Many-core platforms in search for supporting tools

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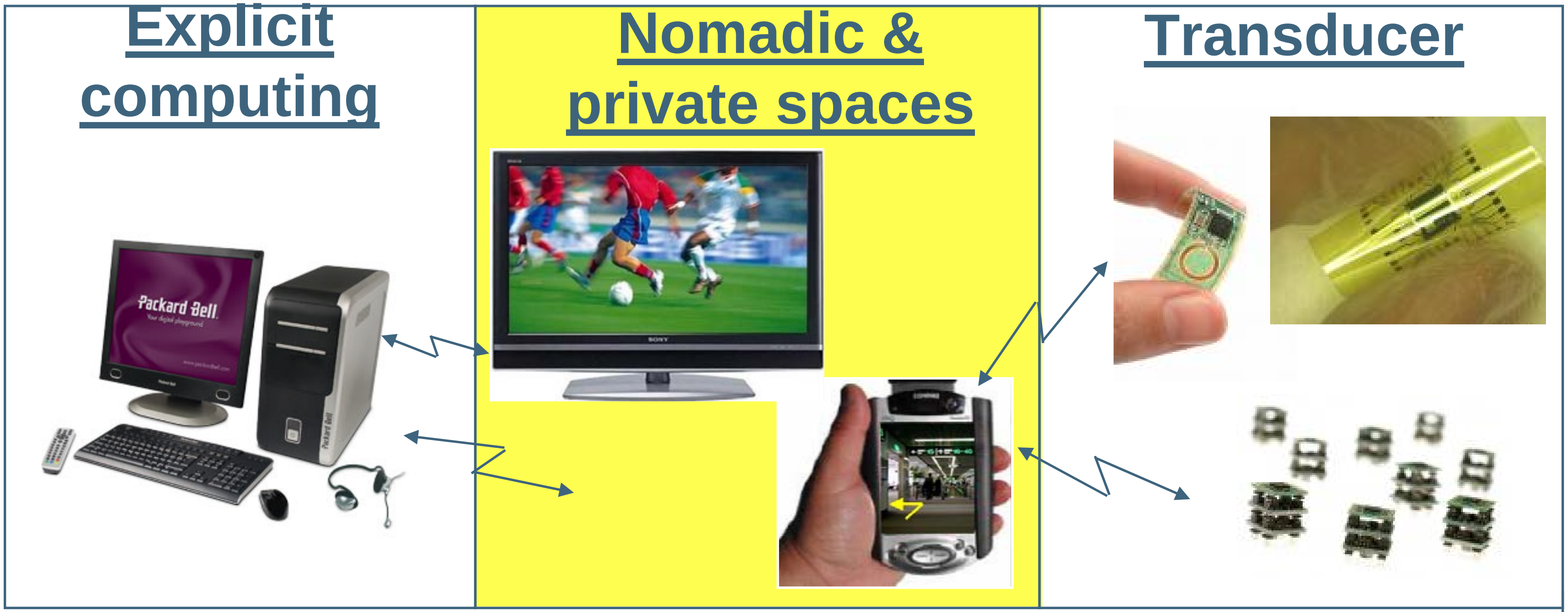
Vision: Multi-core platforms are essential for cheap consumer products and battery operated devices



Explicit computing

Nomadic & private spaces

Transducer

1Tops
100Watt
"Watt" (mains)

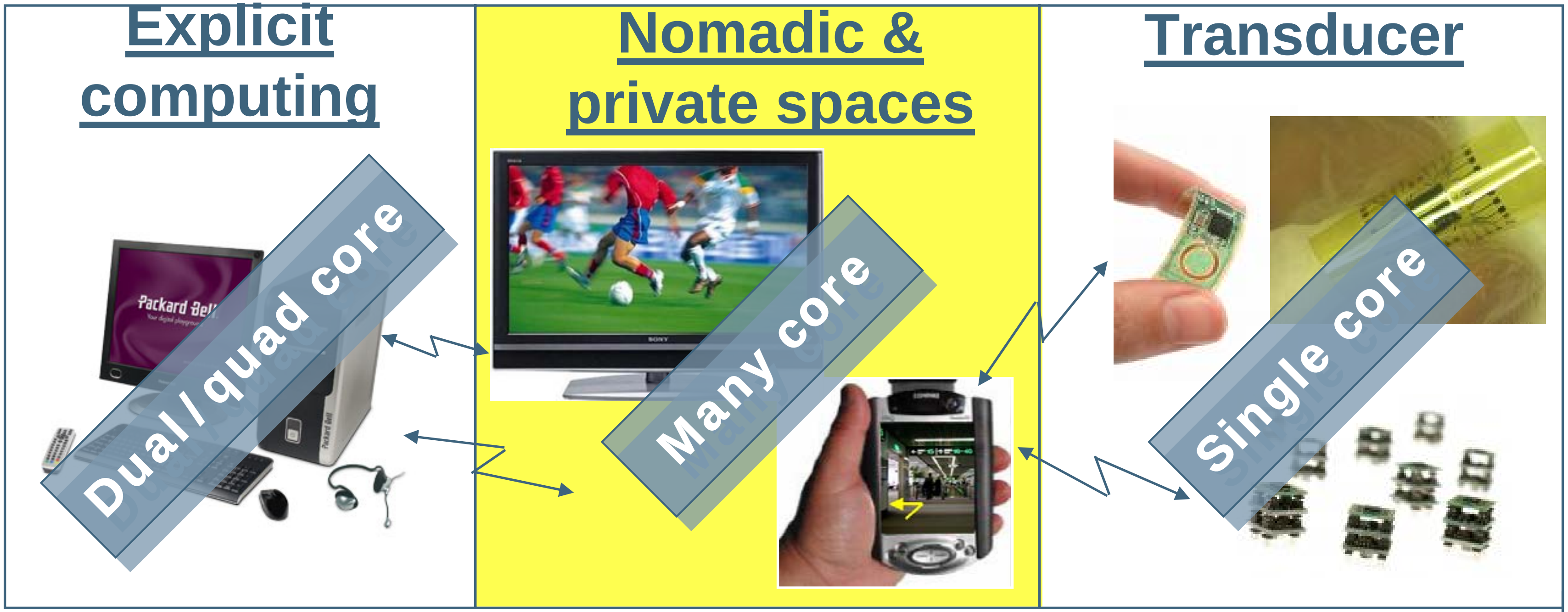
100Gops
1Watt
"Milliwatt" (battery and cheap consumer)

10Gops
100mW
"Microwatt" (ambient)

10Mops
100µW

"More Moore" ← →   ← **"More-than-Moore"** →

Vision: Multi-core platforms are essential for cheap consumer products and battery operated devices



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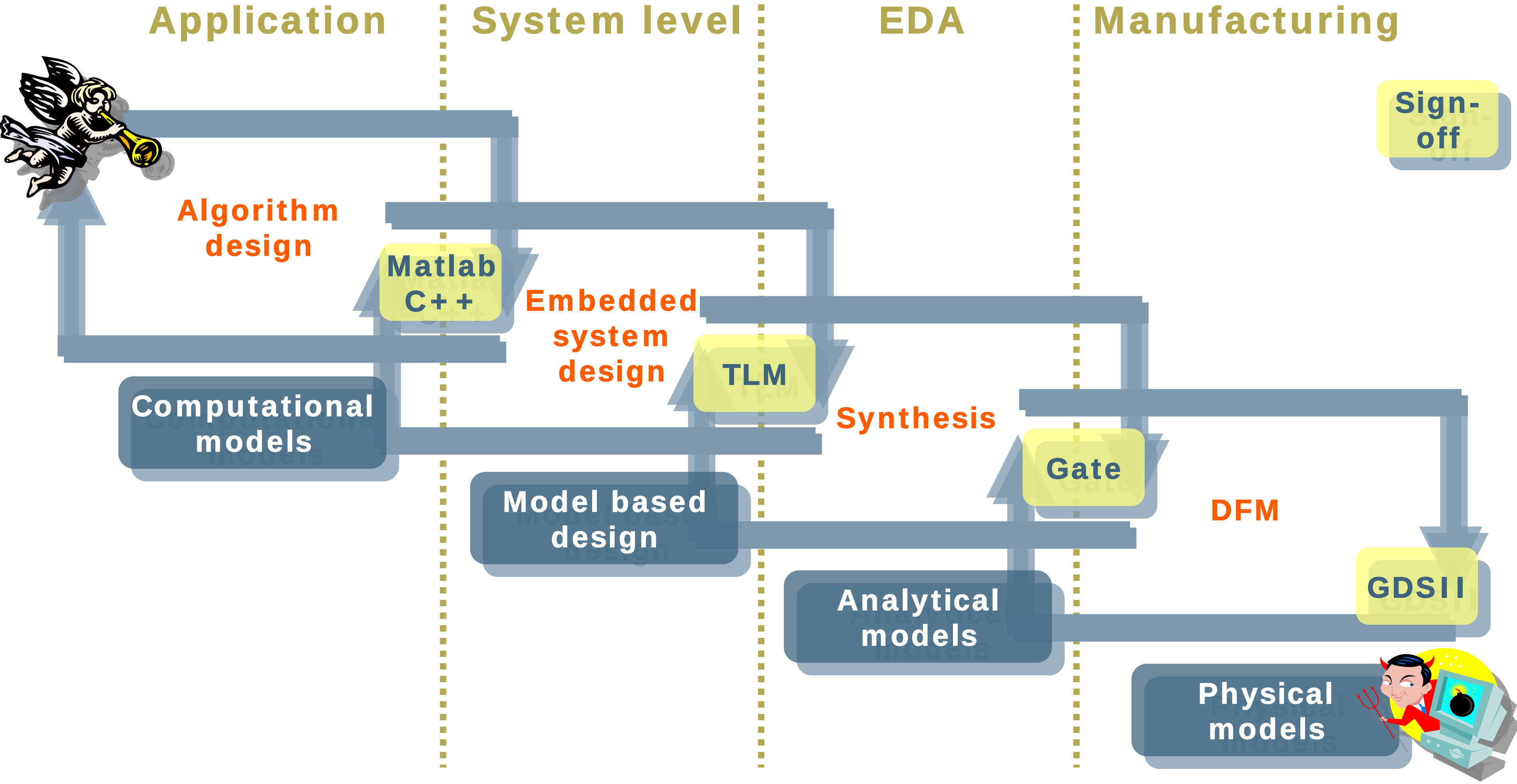
“More Moore”

“More-than-Moore”

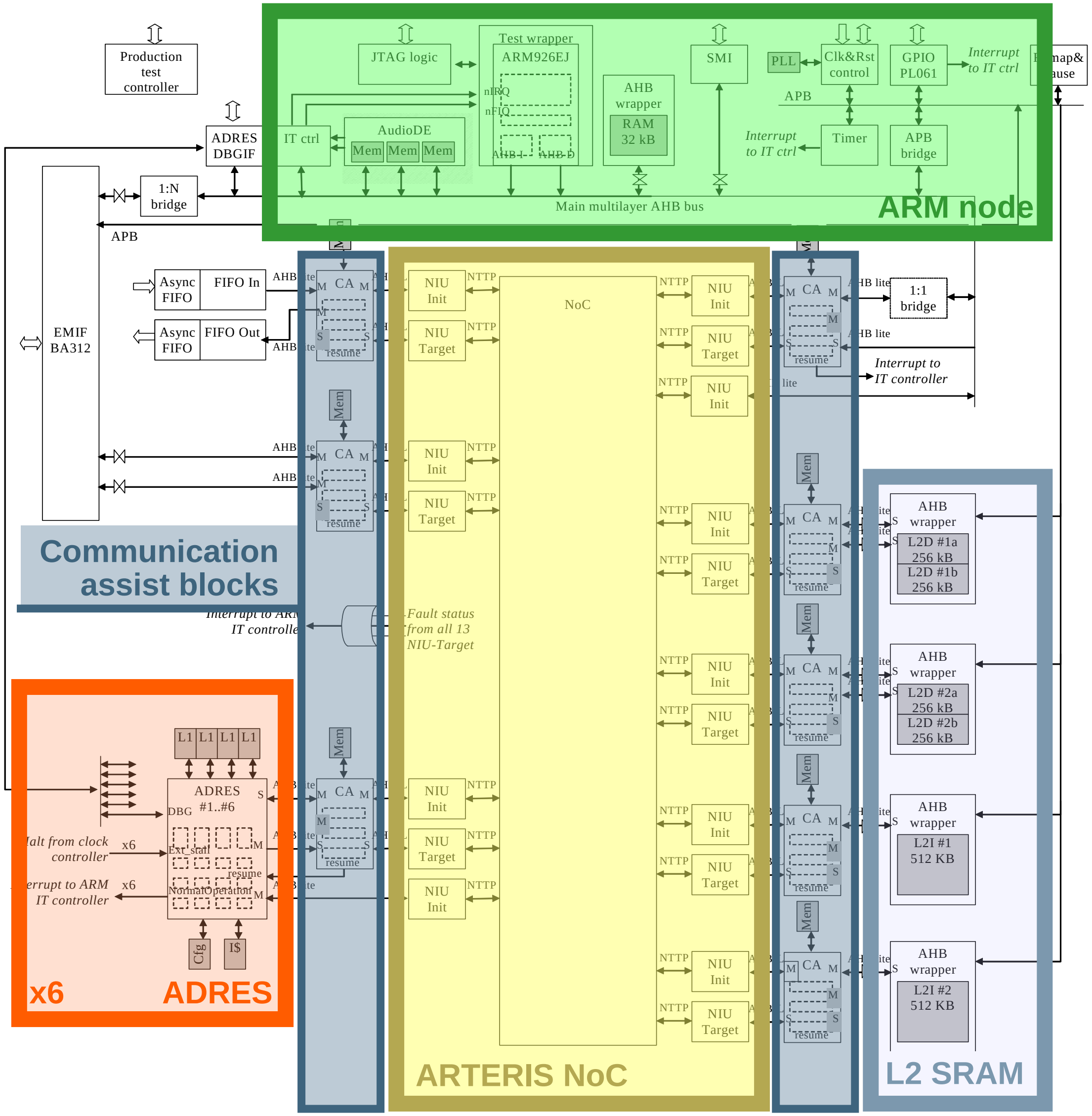
From seventh heaven of service dreams to the hell of physical implementation



Based on: Joachim Kunkel, Synopsys

Example virtual platform for set-top box multimedia codec

- 6 ADRES processors
  - 4x4 array, 3-issue VLIW
  - 32-bit datapath
  - 16 video CODEC specific instructions
  - 8 FUs with multipliers
  - Performance: 300MHz
- 13 Communication assist
  - Performance: 75/150MHz
- ARTERIS NoC
  - Separate instr. and data NoC
  - Bandwidth: 5Gbps@150MHz
- ARM926
  - System control
  - Performance: 75MHz
- L2 memory
  - L2I: 2 banks of 512kB
  - L2D: 4 banks of 256kB
- Voltage islands
  - ADRES processors
  - L2I and L2D banks
- Multiple clock domains
- Specs
  - Area: <60mm2
  - Power: <700mW peak
  - Performance: HDTV AVC encoding @ 30fps



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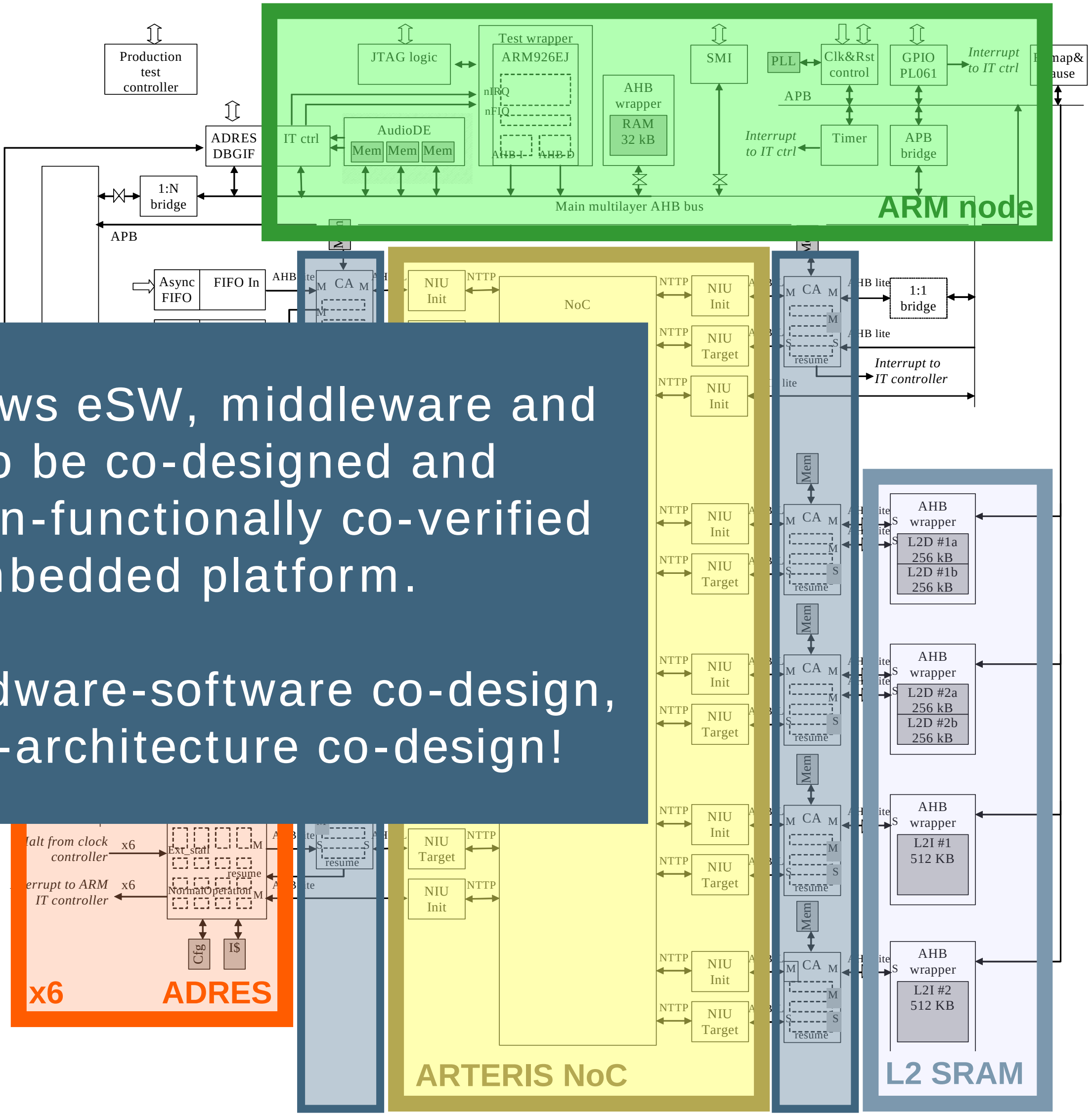
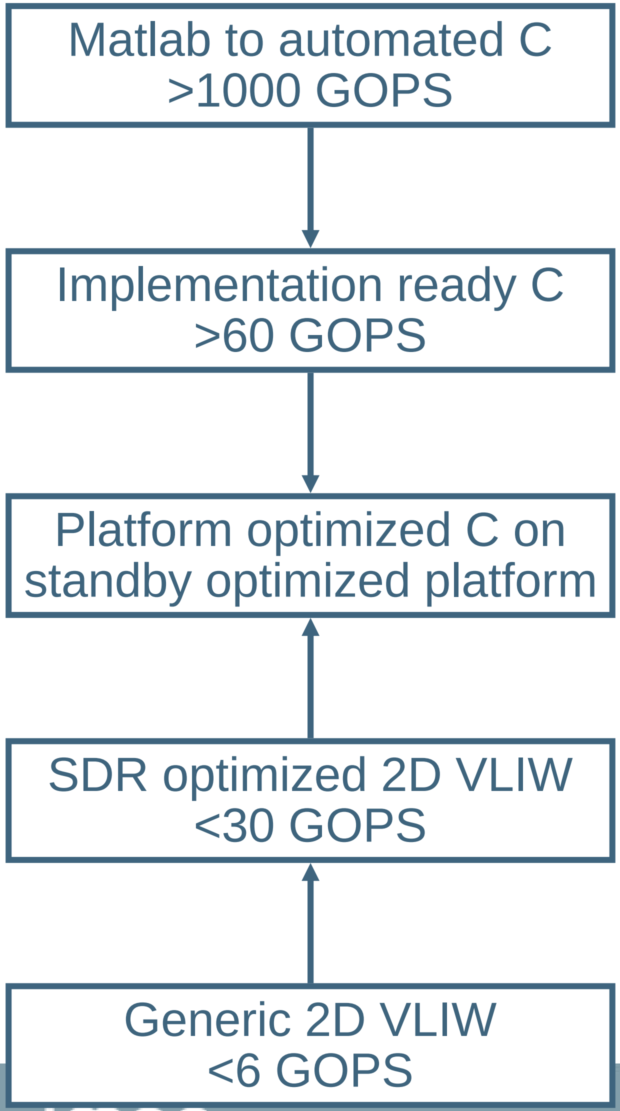


TLM model allows eSW, middleware and firmware to be co-designed and functionally/non-functionally co-verified with embedded platform.

This is NOT hardware-software co-design, but algorithm-architecture co-design!

Algorithm (code)–architecture co-design to bridge huge gaps: Software Defined Radio

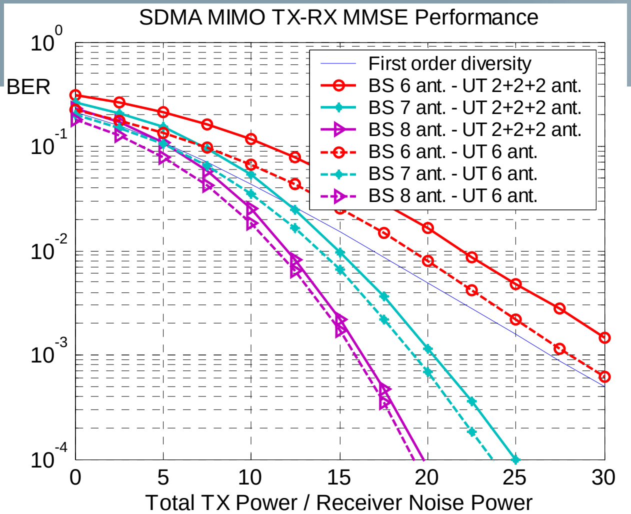

Matlab to automated C
>1000 GOPS

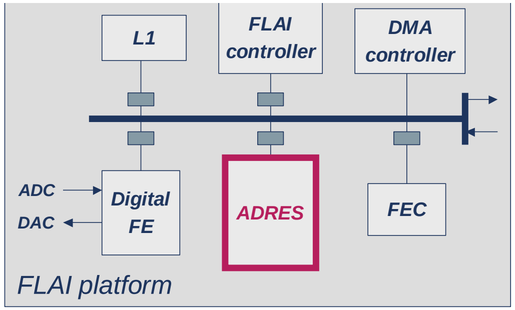
Implementation ready C
>60 GOPS

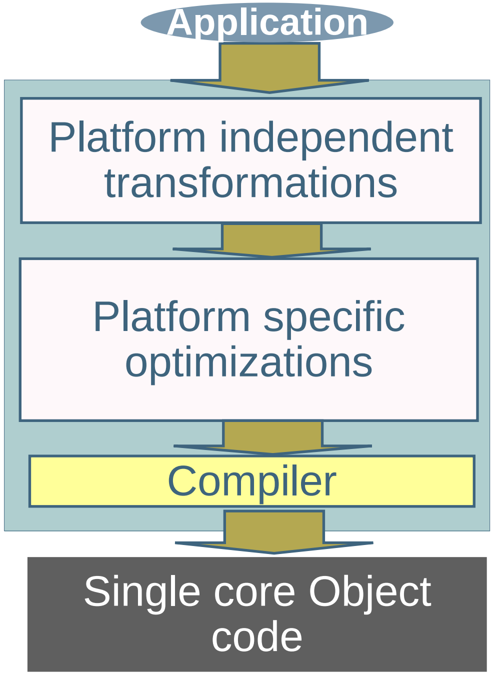
Platform optimized C on standby optimized platform

SDR optimized 2D VLIW
<30 GOPS

Generic 2D VLIW
<6 GOPS


SDMA MIMO TX-RX MMSE Performance



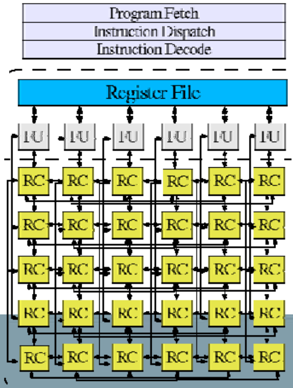

Application

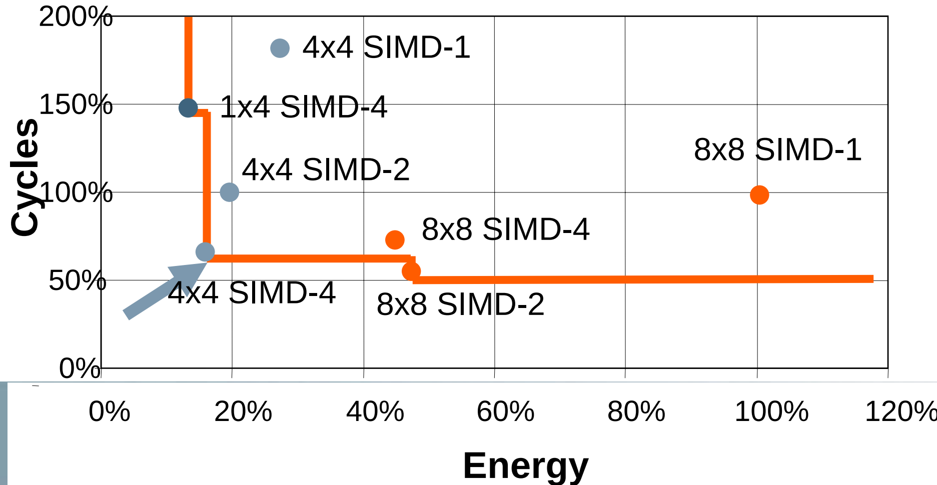
Platform independent transformations

Platform specific optimizations

Compiler

Single core Object code





Platform trends: platforms evolve towards better supporting higher degrees of parallelism to increase power efficiency

Today's multi-core platforms

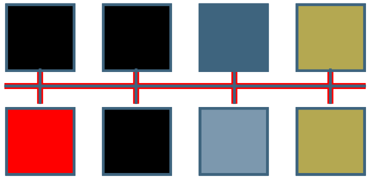
Non-scalable, synchronous bus based interconnect architecture

Limited number of cores (2-8)

One application runs on single core

Single core design flow supports mapping of single application on single processor

Core processors have limited functional (VLIW-8) and data (SIMD-4) parallelism



Next generation many-core platforms

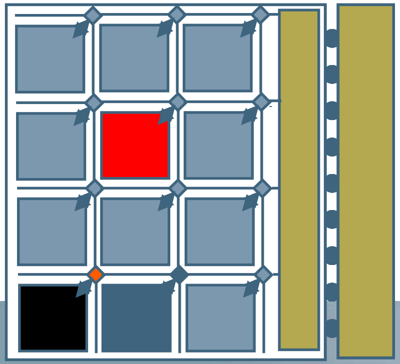
Scalable GALS-NoC based interconnect architecture

Large number of cores (16-100)

One application runs on N cores, depending on run-time load condition

Multi-core design flow supports mapping of multiple applications on heterogeneous multi-core platform

Core processors have high functional (2D VLIW-64) and data (SIMD-1024) parallelism

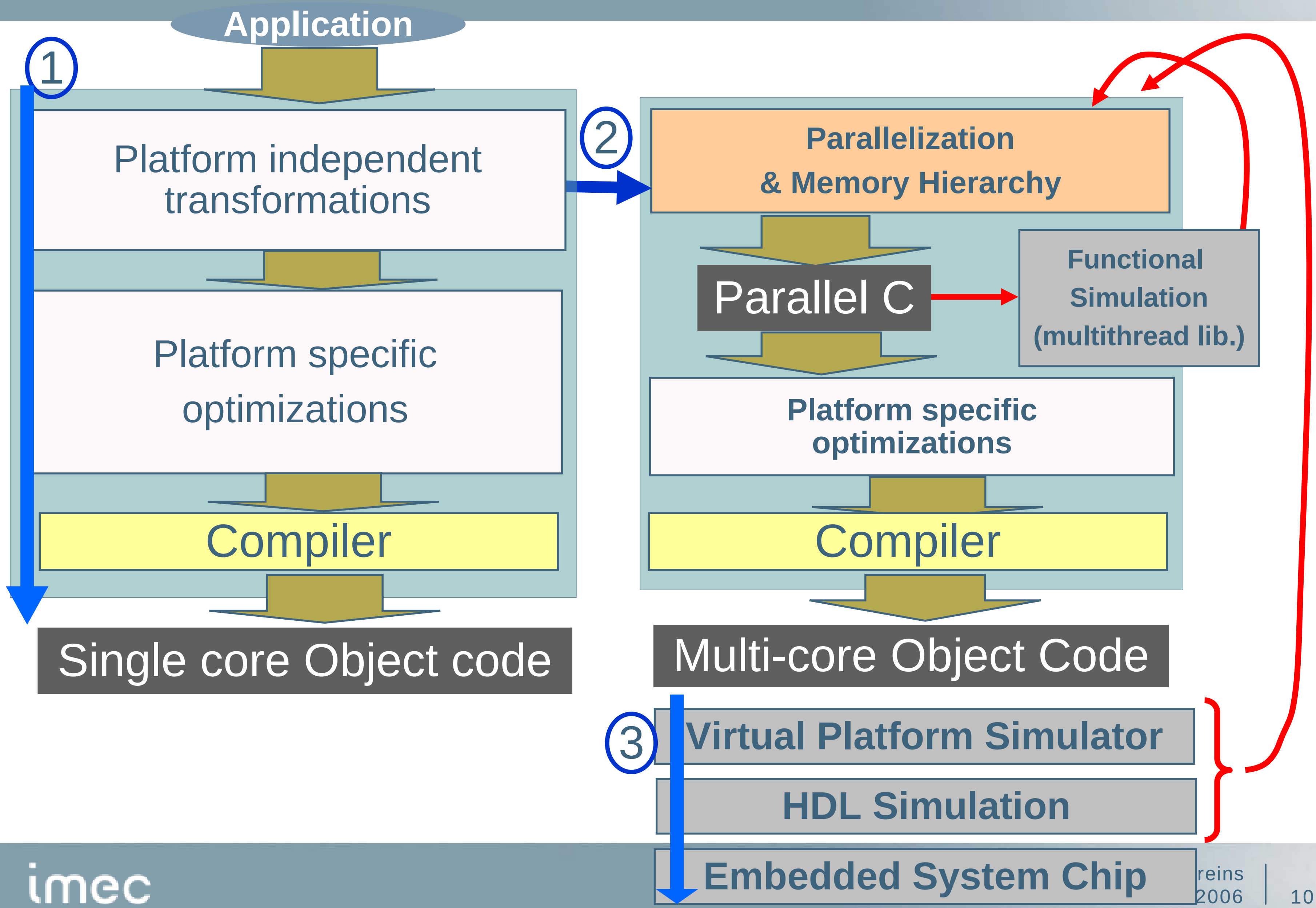


Design Technology trends

- Effective use of advanced processing technology capabilities
  - Dealing with the technology scaling issues so that you get the performance scaling benefit w/o loosing the energy benefit
  - Technology-aware design
- Map 1 application efficiently on one processor
  - Getting the maximal out of emerging processor architectures
  - Compiler and processor technologies
- Map 1 application efficiently on multiple processors
  - Parallelising the application
  - Multi-processor platform mapping
- Mapping of multiple applications on multiple processors
  - Achieving predictability, composability and scalability
  - Multiprocessor platform mapping

Main goal: reduce time-to-market for same power and area budget

Design-Time Flexible Embedded System Design Flow



Application

1

Platform independent transformations

Platform specific optimizations

Compiler

Single core Object code

2

Parallelization & Memory Hierarchy

Parallel C

Functional Simulation (multithread lib.)

Platform specific optimizations

Compiler

Multi-core Object Code

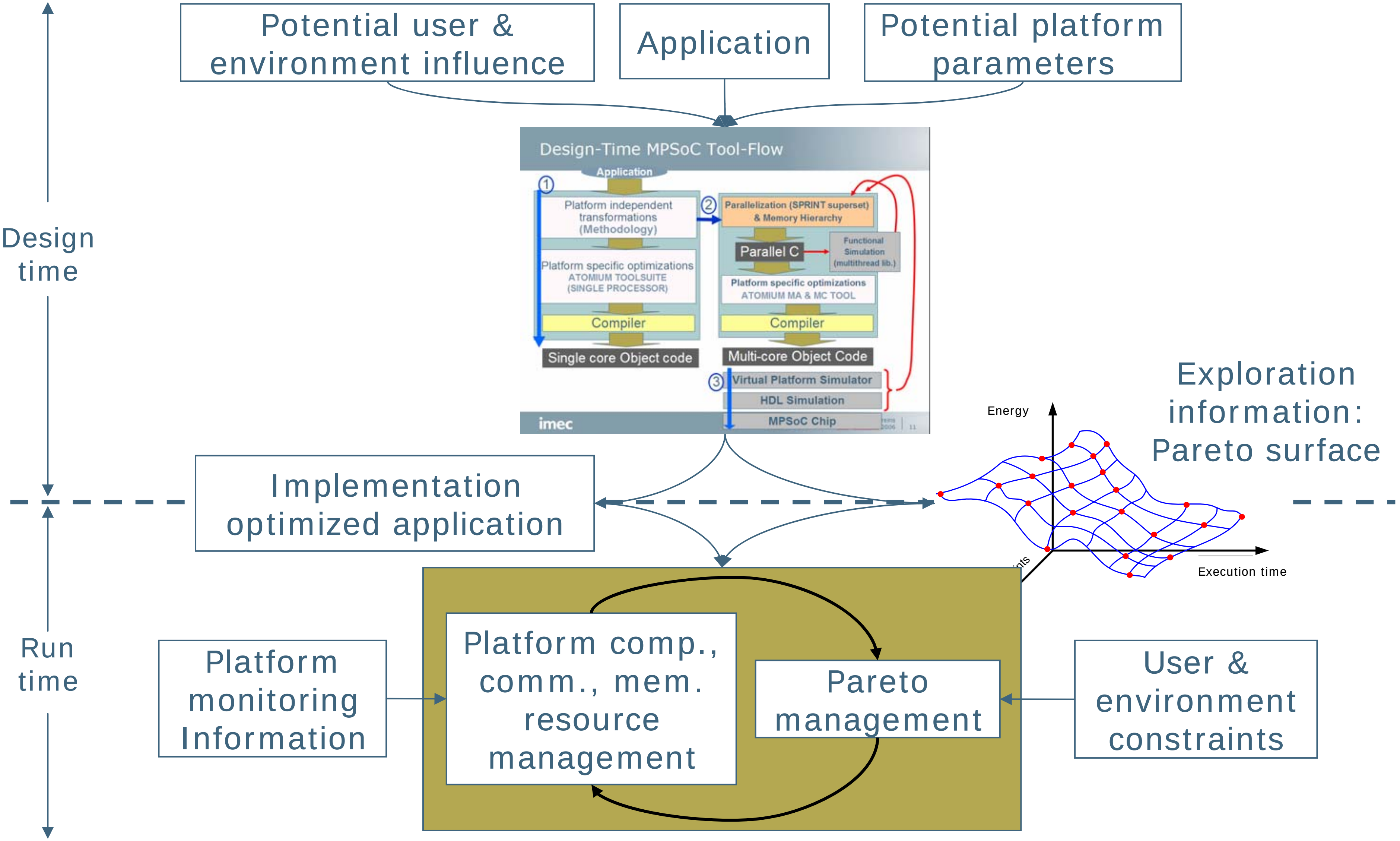
3

Virtual Platform Simulator

HDL Simulation

Embedded System Chip

Composability and scalability require design time analysis and run time control



Design time

Run time

Potential user & environment influence

Application

Potential platform parameters

Design-Time MPSoC Tool-Flow

Application

1 Platform independent transformations (Methodology)

Platform specific optimizations
ATOMIUM TOOLSUITE
(SINGLE PROCESSOR)

Compiler

Single core Object code

2 Parallelization (SPRINT superset) & Memory Hierarchy

Parallel C

Functional Simulation (multithread lib.)

Platform specific optimizations
ATOMIUM MA & MC TOOL

Compiler

Multi-core Object Code

3 Virtual Platform Simulator

HDL Simulation

MPSoC Chip

imec

Implementation optimized application

Exploration information: Pareto surface

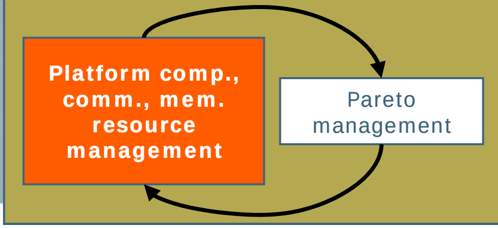
Platform monitoring Information

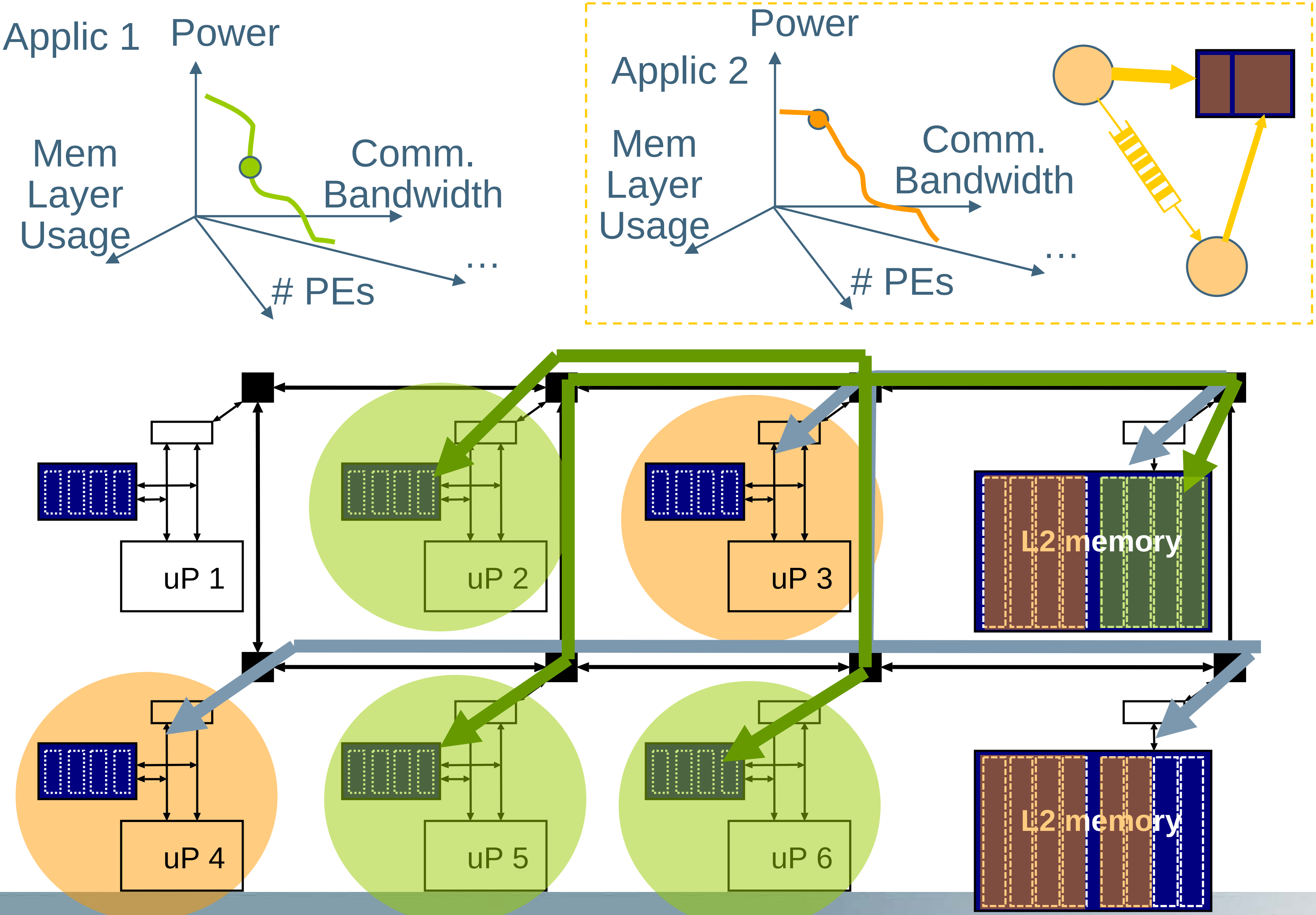
Platform comp., comm., mem. resource management

Pareto management

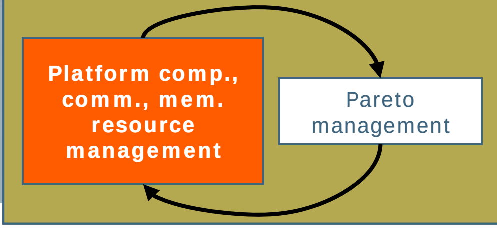
User & environment constraints

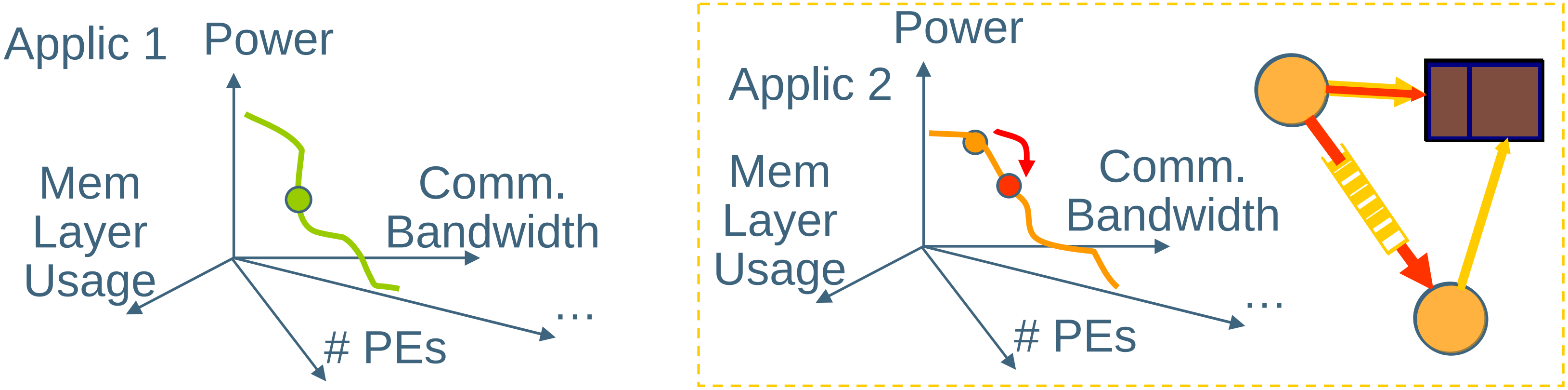
Choosing a Pareto point and assigning resources for 2 applics on same platform

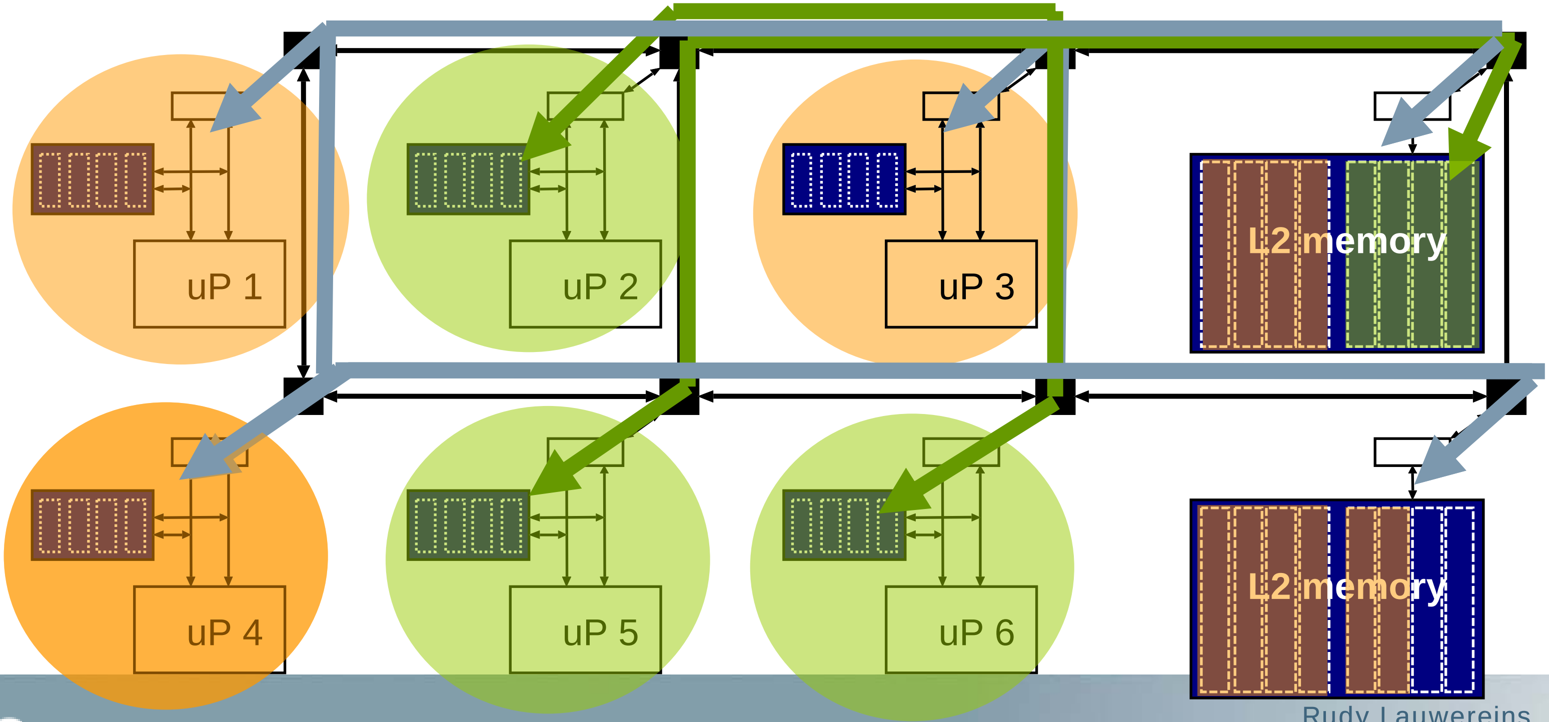




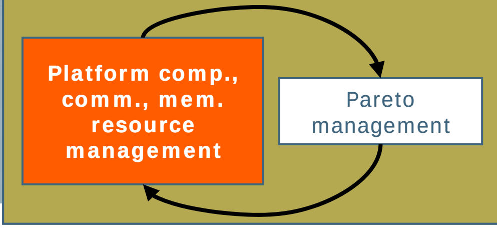
Choosing another Pareto point

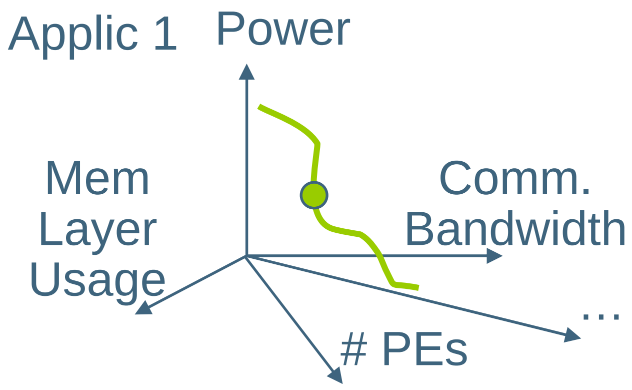


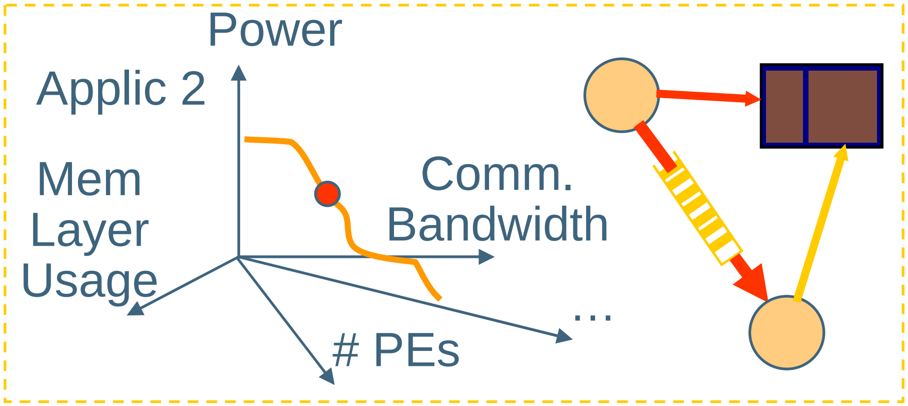


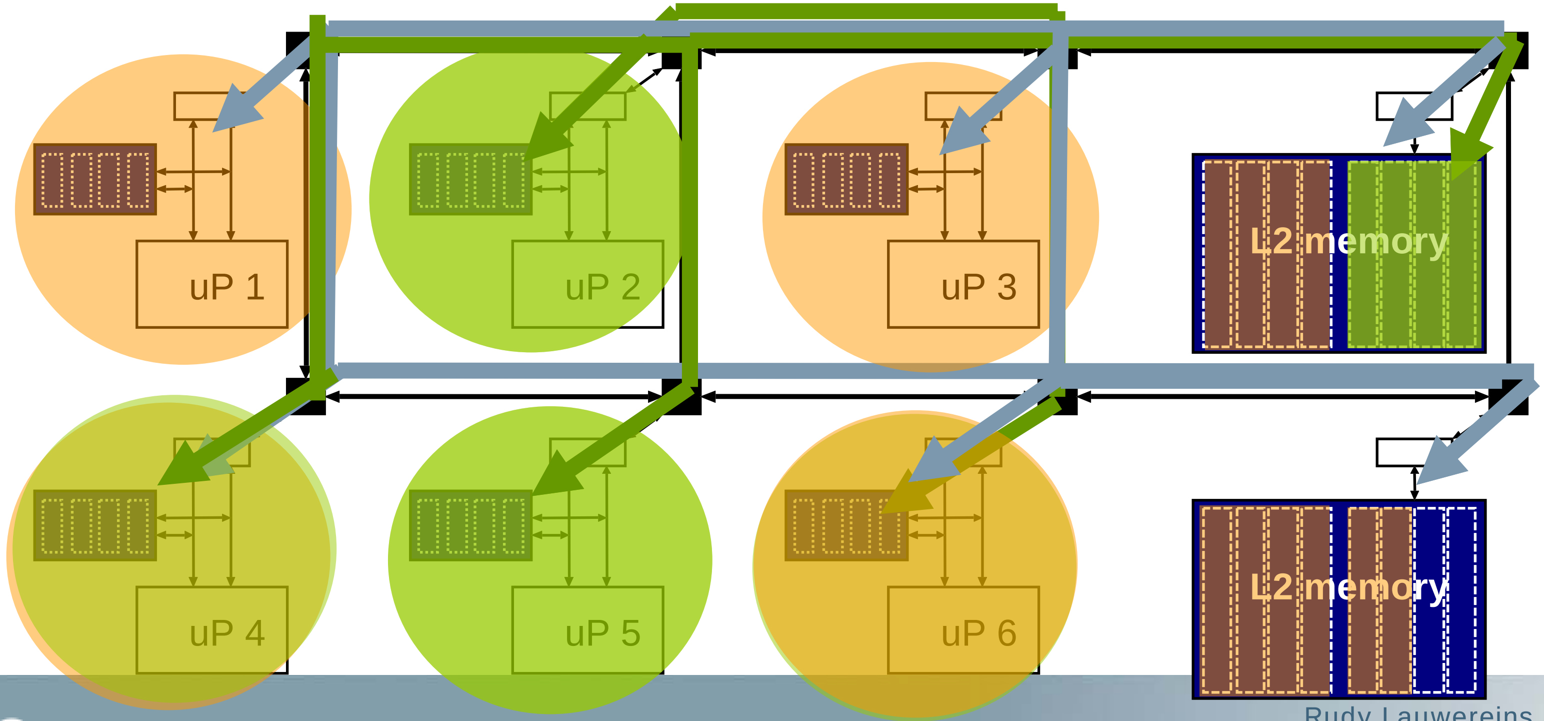


Load balancing









Messages

- Platforms evolve towards supporting higher degrees of parallelism at all levels
- Be aware of the software devil: a multi-core design-time & run-time design flow is in urgent need
- Research in all above is becoming mature and proven in multi-mode radios and multi-format multimedia codecs

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