Fast Decoupling Capacitor Budgeting for Power/Ground Network Using Random Walk Approach

Le Kang, Yici Cai, Yi Zou, Jin Shi,
Xianlong Hong and Sheldon X.-D. Tan

Department of Computer Science and Technology, Tsinghua University, Beijing
Department of Electrical Engineering, University of California, Riverside, CA

Outline

- Introduction of the Optimization of the Power / Ground Network

- Review of Traditional Random Walk Process

- Random Walk based Approach for Decap Allocation

  - Isolation Decap Planting

  - Partition based on Random Walk Process

  - Optimization Flow

  - Refined Leakage Current Modeling for Decaps

- Experimental Results

Outline

Tsinghua University

- Introduction of the Optimization of the Power / Ground Network

- Review of Traditional Random Walk Process

- Random Walk based Approach for Decap Allocation

    - Isolation Decap Planting

    - Partition based on Random Walk Process

    - Optimization Flow

    - Refined Leakage Current Modeling for Decaps

- Experimental Results

Background

- As technology scales down to 90 nanometers and below, signal integrity in the P/G bus is becoming the most insidious issue in high-performance VLSI design

- The improper design of power system can degrade the circuit reliability and cause functional failures due to excessive IR drops, Ldi/dt noise,…

- P/ G Network Optimization has become an intensive research area

Decap Allocation Optimization

- Transient Analysis is used to measure the dynamic noise. Driven by the importance of the analysis, many simulation methods have been proposed to guide the design, such as Conjugate Gradient method, Multi-Grid method, Equivalent Circuit Modeling, Hierarchical Analysis using Macro Modeling

- Dynamic voltage noise may still occur even if the wire sizing is performed.

- Decoupling capacitors addition is a suitable way to reduce dynamic noise.

- However, decap budgeting of the P/G network is a difficult task because of the unbearable run time of the whole chip transient simulation

Related Work

- Nonlinear Program Method [ISPD2002] [ASPDAC2004]
  - Use nonlinear programming and conjugate gradient algorithm to acquire the optimal decap allocation under given constraints
  - Transient analysis should be applied to compute the adjoint network in each step. As shown in previous work, the runtime of an one million node circuit lasts more than 8 hours.
- Partitioning-based Nonlinear Method [DAC2005]
  - Optimize several small circuits instead of the whole circuit.
  - Still carry out the dynamic simulation in each step of the nonlinear programming

The Contribution

- Based on Traditional Random Walk Principle

- Special random walk process is used to find out the partition boundary to plant decaps.

- Trying to improve the design quality at the boundary will improve the time efficiency a lot than trying to find out the optimal solution.

Outline

- Introduction of the Optimization of the Power / Ground Network

- Review of Traditional Random Walk Process

- Random Walk based Approach for Decap Allocation

  - Isolation Decap Planting

  - Partition Based on Random Walk Process

  - Optimization Flow

  - Refined Leakage Current Modeling for Decaps

- Experimental Results

Random Walk Principle

- Traditional Random Walk Principle is a statistical winning process according to Kirchoff law.
  - Brought Out
    - P.G. Doyle and J.L. Snell, "Random Walks and Electric Networks." arXiv:math.PR/0001057
  - Introduced to Power / Ground Network
    - H.-F. Qian, S.R. Nassif. S.S. Sapatnekar, "Random Walks in a Supply Network," In Proceeding of IEEE/ACM Design Automation Conference, pp. 93-98, 2003

Random Walk Principle

- Circuit illustrated right can be written as the formula :

$$V_x \sum g_i - \sum g_i V_i = -I_s$$

- Then we can have, $V_x = \sum \dfrac{g_i}{\sum g_i} V_i - \dfrac{I_s}{\sum g_i}$

- Let the coefficient $P_{x,i} = \dfrac{g_i}{\sum g_i}$ as the probability from x to i, then $\sum p_{x,i} = 1$

- The constant $-\dfrac{I_s}{\sum g_i}$ is the cost at node x

- *The statistical way to solve the random walk process is to play the walking-game several times, and consider the average cost of these walking processes as the voltage of the beginning node*
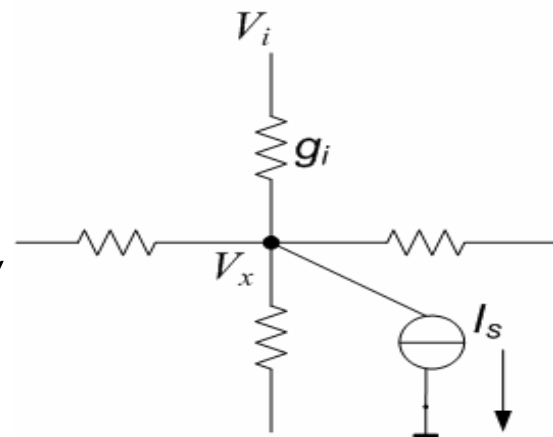
Characteristic

- We have implemented the traditional random walk algorithm. The table below compare it with PCG in terms of speed and accuracy.
  - The random walk method is much faster than PCG approach
  - Also, the max absolute error margin is just about 11 mv

Circuit Size	Run Time		Accuracy			
	PCG (s)	*Random Walk (s)*	*PCG (v)*	*Random walk (v)*	*Absolute Error(mv)*	*Relative Error*
100	0.001	<0.001	1.998032	1.998423	0.391	0.02%
1600	0.021	0.002	1.944538	1.940454	4.084	0.21%
6400	0.146	0.015	1.901242	1.907516	6.274	0.33%
25600	1.224	0.108	1.853241	1.861951	8.710	0.47%
102400	10.816	1.140	1.740406	1.751299	10.893	0.63%

Characteristic

- Random walk algorithm is much faster when solving the specific node.

- Poor Performance

  - Use random walk to calculate the whole circuit with few Vdd pads

- Difficulty

  - Usage for Transient Analysis

    - Voltage variation for decoupling capacitor.

Outline

- Introduction of the Optimization of the Power / Ground Network

- Review of Traditional Random Walk Process

- Random Walk based Approach for Decap Allocation

  - Isolation Decap Planting

  - Partition Based on Random Walk Process

  - Optimization Flow

  - Refined Leakage Current Modeling for Decaps

- Experimental Results

Outline

- Introduction of the Optimization of the Power / Ground Network

- Review of Traditional Random Walk Process

- Random Walk based Approach for Decap Allocation

  - Isolation Decap Planting

  - Partition Based on Random Walk Process

  - Optimization Flow

  - Refined Leakage Current Modeling for Decaps

- Experimental Results

- Due to high via density in M1, the noise current inside local area usually doesn't propagate along with the rail but trends to go up to M2 from the vias.

- If no decaps are planted to provide fast current return path, it will go to up layers until the pad is reached.

- The worst case is the current sources inside the local area turn on simultaneously.

  - find out some boundary nodes that do not consume large dynamic current

  - plant enough decaps to provide fast current return path

- Consider how to partition the whole network later

- Suppose all the boundary nodes are given.

- Then calculate the average current per each node inside the local area according to the piece wise liner (PWL) model.

- Plant a decap at the boundary node with its capacity C_i satisfying equation:

$$\overline{I}_i - \frac{2C_i}{h} \times V_i = 0$$

- We compare the IR drops before and after the planting process on test cases.

  - The maximum dynamic IR drop in the sub-circuit has been reduced obviously
  - Nearly all the nodes' voltage drops have been improved.
  - In other words, even if we only plant decaps at the boundary, the dynamic performance of each sub area can be improved.

TABLE II The Voltage Drop Comparison before/after Using the Isolate Planting Process

Sub area	Total Node Number	Max Vol Drop(mv)	Violation Node Num	Optimized Boundary	
				Max Vol Drop(mv)	Improved Node Num
1	744	203.62	11	30.83	10
5	7492	260.47	46	72.06	46
14	32112	315.71	124	135.19	122

Outline

- **Introduction of the Optimization of the Power / Ground Network**

- **Review of Traditional Random Walk Process**

- **Random Walk based Approach for Decap Allocation**
    - Isolation Decap Planting
    - Partition Based on Random Walk Process
    - Optimization Flow
    - Refined Leakage Current Modeling for Decaps

- **Experimental Results**

Partition Based on Random Walk Process

- The planting decaps at the boundary nodes can improve the dynamic performance of internal nodes.

- Problem
  - How to partition the whole circuit?
  - If unluckily the violation node locates at the boundary??
    - It is hard to optimize

- Modified Random Walk Process

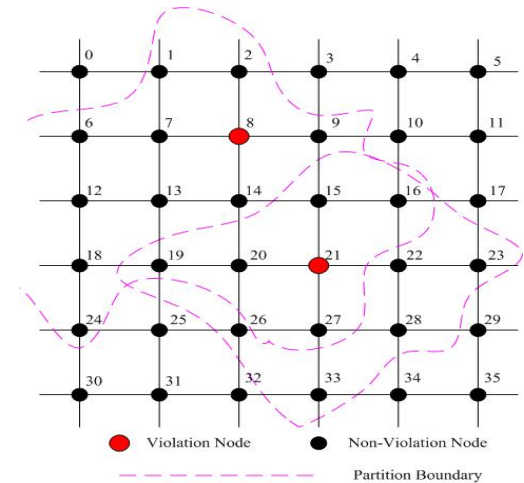# Partition Based on Random Walk Process

- Firstly, we adopt a CG solver based on incomplete cholesky decomposition as the simulation tool to gain the violation nodes

- Then apply modified random walk process.
  - The violation node is considered as the beginning node
  - The probability in the walking process is treated as same as that in traditional random walks
  - The cost of each node is ignored.
  - Our brief target is to achieve the boundary of walking process

- After finishing the walking process from each violation node, the boundary of each violation node is gained.

The Boundary Gained by the Modified Random Walk Process

- As shown, the partitions, acquired by node 8 and 21, are not separated.

- It is essential to merge the partitions that intersect each other and calculate a new boundary.

- Isolation Decap Planting for each sub-circuit

Outline

- Introduction of the Optimization of the Power / Ground Network

- Review of Traditional Random Walk Process

- Random Walk based Approach for Decap Allocation
  - Isolation Decap Planting
  - Partition Based on Random Walk Process
  - Optimization Flow
  - Refined Leakage Current Modeling for Decaps
- Experimental Results

Optimization Flow

- Decaps flow based on Random Walk Process
- 1. Solve the circuit, and identify the violation nodes;
- 2. While (violations) {
- 3. For each violation node {
- 4.   Apply modified random walk process;
- 5.   Form the partition in the walking process}
- 6. Merge the partitions that intersect each other;
- 7. Use isolation decap planting for each partition;
- 8. Update all the decaps and solve the new circuits}
- 9. Optimization Successful.

Outline

- Introduction of the Optimization of the Power / Ground Network

- Review of Traditional Random Walk Process

- Random Walk based Approach for Decap Allocation

  - Isolation Decap Planting

  - Partition Based on Random Walk Process

  - Optimization Flow

  - Refined Leakage Current Modeling for Decaps

- Experimental Results

Leakage Effects

- Over-adding decaps may increase power consumption significantly if leakage effects are considered

  - Jingjing Fu, Zuying Luo, Xianlong Hong, Yici Cai, Sheldon X.-D. Tan, Zhu Pan, "VLSI On-Chip Power/Ground Network Optimization Considering Decap Leakage Currents", 2005.1, The 10th IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC2005)

- The leakage current of the MOS-based decap can be formulated as: $I_{gate} = k \times (\frac{V}{Tox})^2 \times e^{-\alpha \cdot Tox/V} \times w$

  - I_{GATE} is the exponential function of the supply voltage V

Tsinghua University

- The leakage model proposed in 2005, is a linear model, which is a little simplified.

- Our new model contains a time-variant current source, besides a resister, and a capacitor. The current is estimated according to the exponential formula.

- After the circuits are optimized with the simple model, we introduce the newly model to verify the circuits. The results in the table show that the violation nodes still appear. Our refined model is more accurate.
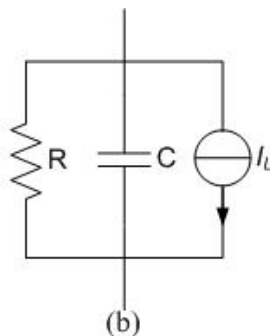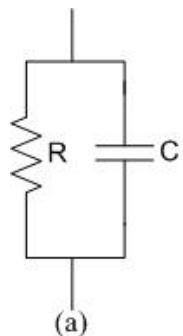

(a)

(b)

TABLE III Violation Node Statistics Comparison to the Simplified Model when our New Model is Considered.

VN = Violation Node

| Circuit Name	Node Num	Eliminated VN Num	VN Num	Newly VN Num Using Our Model
U_cnt100	744	102	0	2
U_cnt500	3741	679	0	9
u05614	32112	3977	0	26

Outline

- Introduction of the Optimization of the Power / Ground Network

- Review of Traditional Random Walk Process

- Random Walk based Approach for Decap Allocation
  - Isolation Decap Planting
  - Partition Based on Random Walk Process
  - Optimization Flow
  - Refined Leakage Current Modeling for Decaps

- Experimental Results

Experimental Results

- We implement our algorithm in C++ programming languages and compare it with the heuristic method and optimal method.

- All test cases are generated according to the real industry standard-cell circuits with pre-placement information in LEF/DEF format.

- Those circuits have complexities ranging from 744 nodes to 1.6 million nodes.

- The optimization results on the 744 node circuit are similar to that using a heuristic method based on the sensitivity
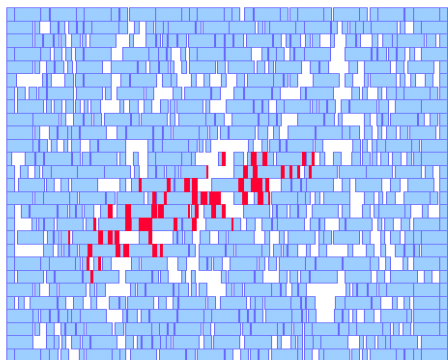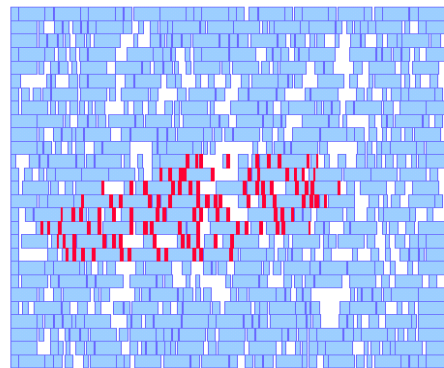
The Proposed Method   Decap Allocation based on Sensitivity

Experimental Results

Experimental Results Compared to Existing Heuristic Budget and Optimal Budget Method

Circuit Name	#Node	#violation	Heuristic Budget		Optimal Budget		Random Walk Based		Speedup On Heuristic	Deviation from Optimal
			Time (s)	Aera of Decap(um^2)	Time (s)	Aera of Decap(um^2)	Time (s)	Aera of Decap(um^2)		
u_cnt100	744	96	37.34	7182.58	117.08	6779.66	7.81	7190.24	4.8	6.06%
u_cnt500	3741	665	223.59	44938.03	961.42	42372.17	33.14	45072.39	6.7	6.37%
U05614	32112	3682	2812.04	176975.84	8709.37	169491.63	370.96	178290.51	7.6	5.19%
U19649	112392	10755	11834.1	728931.47	39257.62	677966.08	958.63	721091.26	12.3	6.36%
U28070	1618026	612132	28596.4	8922309.20	NA	NA	1606.54	9142708.72	17.8	NA

Our proposed method is usually 10 times faster than the sensitivity method, and the deviation from the optimal area is about 6%.

Experimental Results

- Use the two-stage optimization method to consider decap leakage in P/G
  - Optimize the dynamic voltage noise assuming all decaps are leakage free
  - Perform the wire sizing strategy to compensate the IR drops caused by leakage
- Compare routing resource between the simplified leakage model and our newly proposed accurate model.
  - The routing resource of our newly leakage model only has 1% deviation
  - But our proposed model makes the optimization process more practical.

TABLE V
Optimization Result Comparison between Two Leakage Models
using the Two-Stage Method

Circuit Name	#Node	Added Decap without Leakage (um^2)	Ratio of Routing Resources Increases	
			Simplified Model	Our Accurate Model
u_cnt100	744	7190.24	1.85%	1.88%
u_cnt500	3741	45072.39	5.83%	5.86%
u05614	32112	178290.51	3.00%	3.25%
u19649	112392	721091.26	4.91%	5.14%

Conclusion

- Fast decap optimization method based on the idea of using random walk approach

    - Find out the partitions using the modified random walk process, and then add decaps on these boundary of partitions. A refined leakage current model for decap is considered.

    - The experimental results on the test cases demonstrate that the proposed method based on random walk process saves much run time and is also very efficient compared with the other method.

That is all!

- Thank you for listening!