A Current-based Method for Short Circuit Power Calculation Under Noisy Input Waveforms

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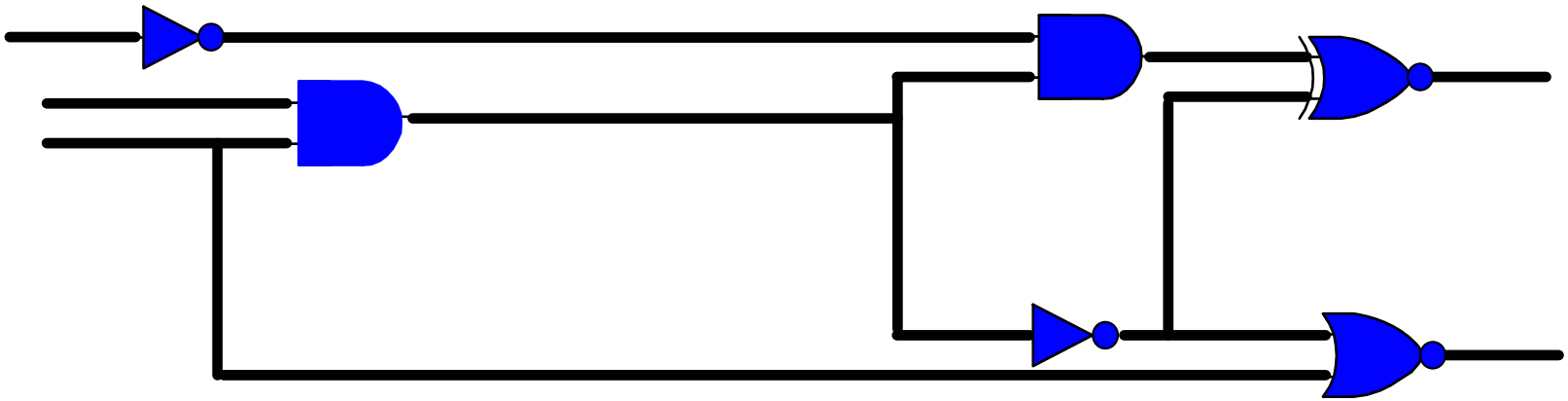
Outline

- **Motivation**
- **Introduction**
- **Current Source Modeling**
- **A Current-based Short-circuit Power Calculator**
- **Experimental Results**
- **Conclusion**

Power Analysis

- **A digital CMOS circuit is a collection of CMOS gates:**

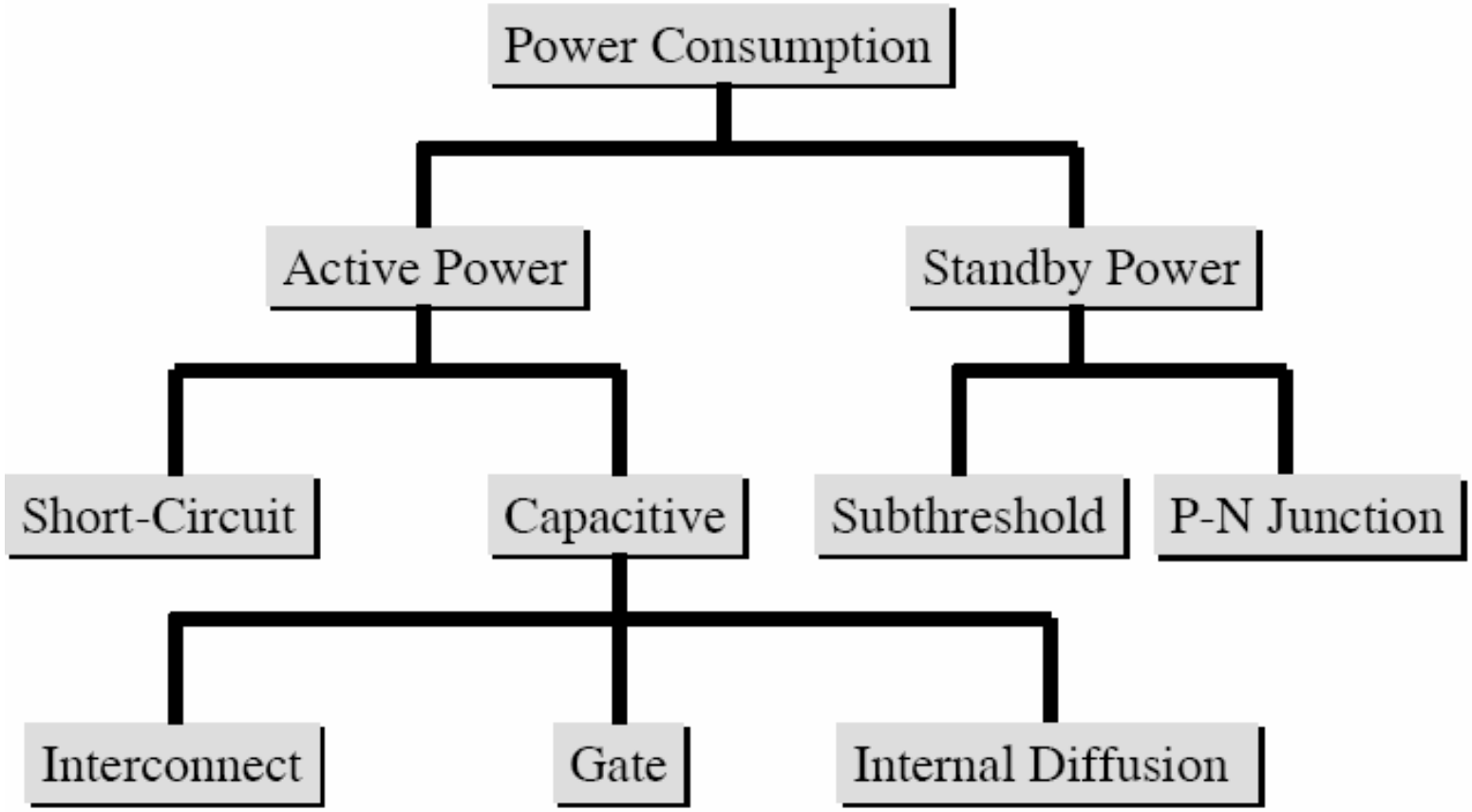


- **Accurate power estimation is a critical step in the analysis and design of such circuits**

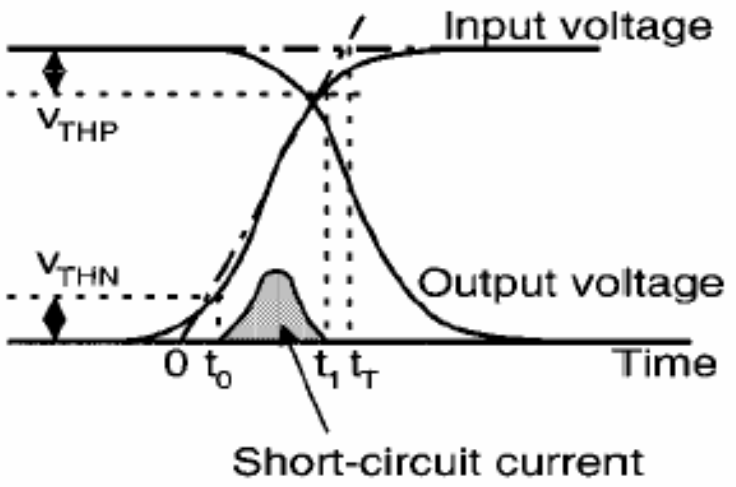
Power Analysis Challenges

- **Input pattern dependency:**
  - **Knowledge of a “typical” or “expected” input stream**
    - **E.g., Signal probability, switching activity, spatio-temporal correlation**
    - **Addressed by various statistical and/or probabilistic power estimation techniques**
- **Variability in the shape of the input signal waveform**
  - **Due to different sources of noise, such as crosstalk noise and DC drop on supply lines and /or process variation**

Sources of Power Consumption in CMOS



Short Circuit Power Calculation



- **Short circuit current:**
  - **Due to current the flows from the Vdd rail to ground during an output transition**
  - **Depends on the duration of time that transistors in the pull-up and pull-down sections of a CMOS logic cell operate in each region of the transistor operation**
  - **Depends on both input and output voltage waveforms**
- **How to measure short circuit current and energy dissipation?**

Prior Work

- **Closed-form analytical expressions based on simple device models:**
  - **H. Veendrick (1984), based on the Shichman–Hodges model**
  - **S. Vemuri et al. (1994) and K. Nose et al. (2000) based on the alpha-power model**
  - **L. Rossello et al. (2002) based on a charge-based device model called MM9**
  - **Lack of accuracy due to use of simple device models and assumptions made regarding the device operation during signal transitions**
- **Pre-characterization:**
  - **Dartu et al. (1996), based on input signal transition time and capacitive output load**
- **Generalized device equations and table lookup based computations**
  - **Acar et al. (2003), quadrilateral model of short circuit current waveform**
- **All these techniques assume a ramp signal as the input**

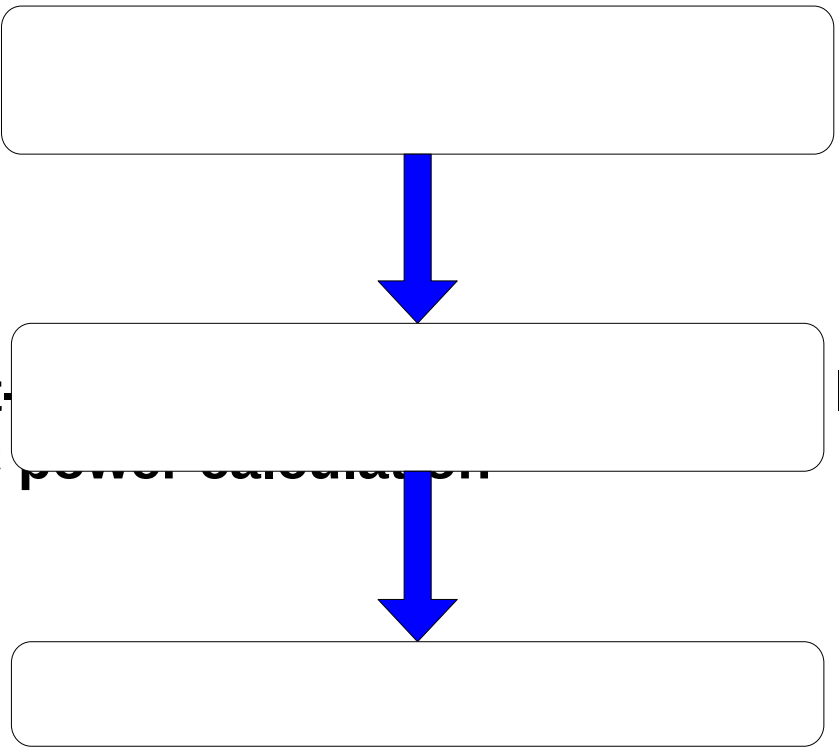
Short Circuit Power Calculation Flow

- **Problem statement:**

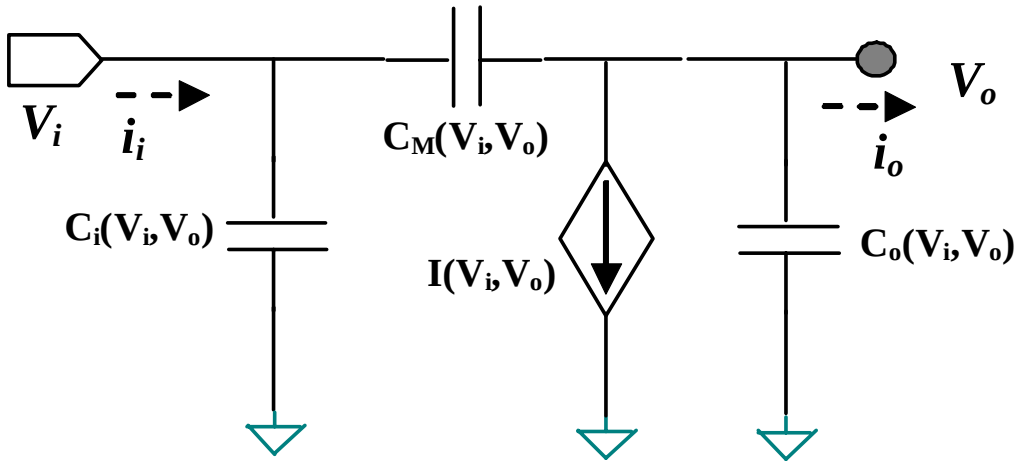
  Develop a short circuit power calculator capable of handling noisy inputs (including glitches) with arbitrary shapes

- **Solution:**

  Utilize Current- **logic cells for the purpose of SC**



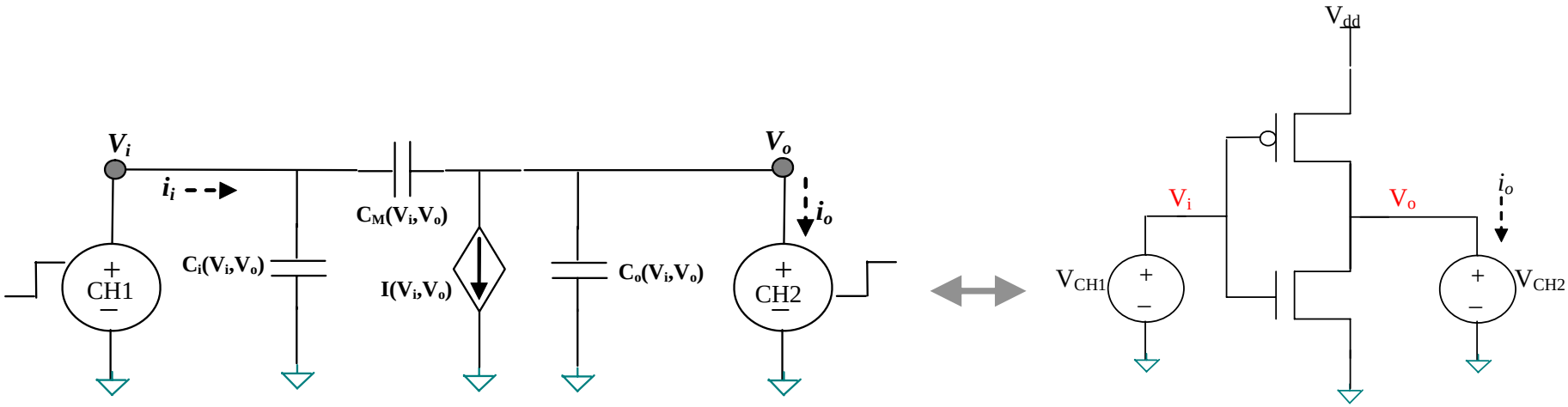
Our Current Source Model (Fatemi et al. DAC 06)



$$i_o + C_o \frac{\Delta V_o}{\Delta t} + I(V_i, V_o) + C_M \frac{\Delta V_o}{\Delta t} - C_M \frac{\Delta V_i}{\Delta t} = 0$$

- **The non-linear behavior of the logic cell:**
  - **2-D lookup table to store $I(V_i,V_o)$**
- **Parasitic effects in the logic cell:**
  - **2-D lookup tables to store $C_i(V_i,V_o)$, $C_M(V_i,V_o)$, and $C_o(V_i,V_o)$**
- **Series of SPICE simulations to pre-characterize various elements of the CSM model**

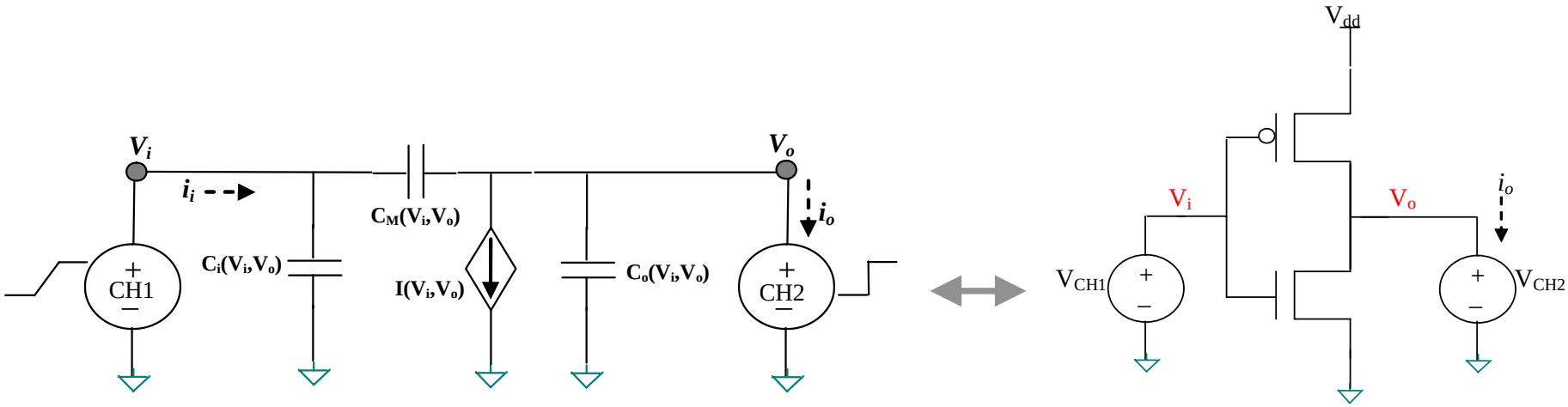
CSM Pre-characterization: Current Source



$$i_o + C_o \frac{\Delta V_o}{\Delta t} + I(V_i, V_o) + C_M \frac{\Delta V_o}{\Delta t} - C_M \frac{\Delta V_i}{\Delta t} = 0$$

- $I(V_i,V_o)$:
  - Apply DC voltage sources V_{CH1} and V_{CH2} to the input and output
  - Measure i_o (the current going trough V_{CH2}) in SPICE and fill the entry $I(V_{CH1},V_{CH2})$ of the table
  - Sweep the DC voltage sources

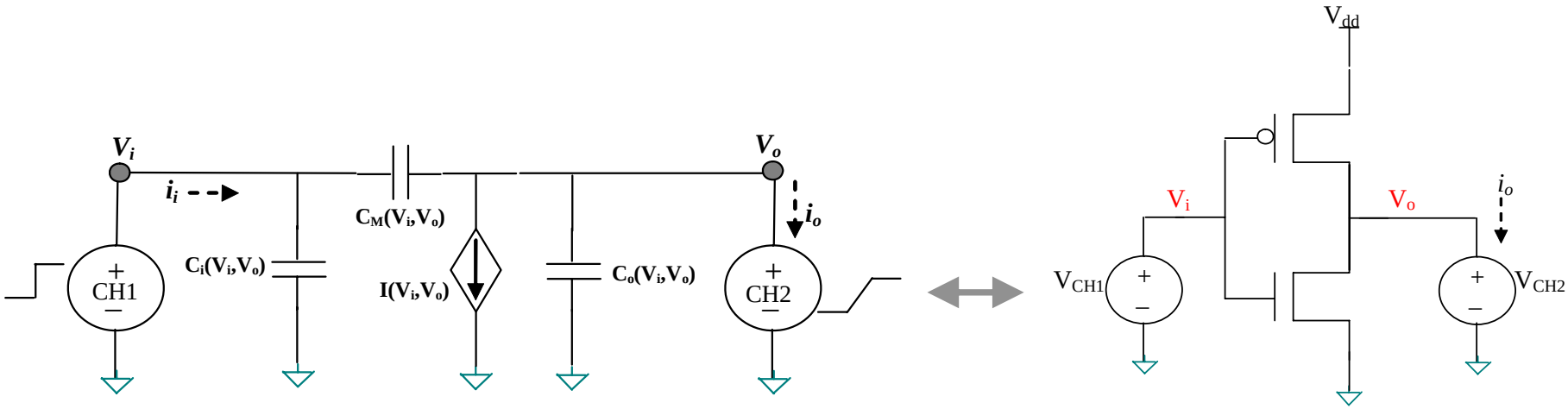
CSM Pre-characterization: Parasitics (C_M)



$$i_o + C_o \frac{\Delta V_o}{\Delta t} + I(V_i, V_o) + C_M \frac{\Delta V_o}{\Delta t} - C_M \frac{\Delta V_i}{\Delta t} = 0$$

- $C_M(V_i,V_o)$
  - Apply a ramp voltage source to input and a DC source to output
  - Measure i_o in SPICE for different voltage values at the input
  - Calculate C_M from the KCL eqn and fill out one column of the table
  - Sweep the DC voltage source at the output

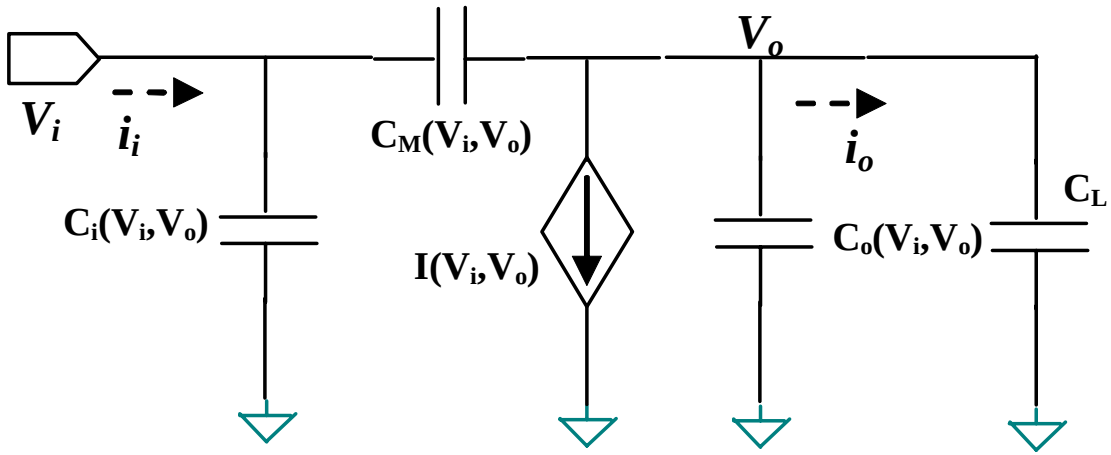
CSM Pre-characterization: Parasitics (C_o)



$$i_o + C_o \frac{\Delta V_o}{\Delta t} + I(V_i, V_o) + C_M \frac{\Delta V_o}{\Delta t} - C_M \frac{\Delta V_i}{\Delta t} = 0$$

- $C_o(V_i, V_o)$
  - Apply a DC source to input and a ramp voltage source to output
  - Measure i_o in SPICE for different voltage values at the output
  - Calculate C_o from the KCL eqn and fill out one row of the table
  - Sweep the DC voltage source at the input

Voltage Calculation Using CSM

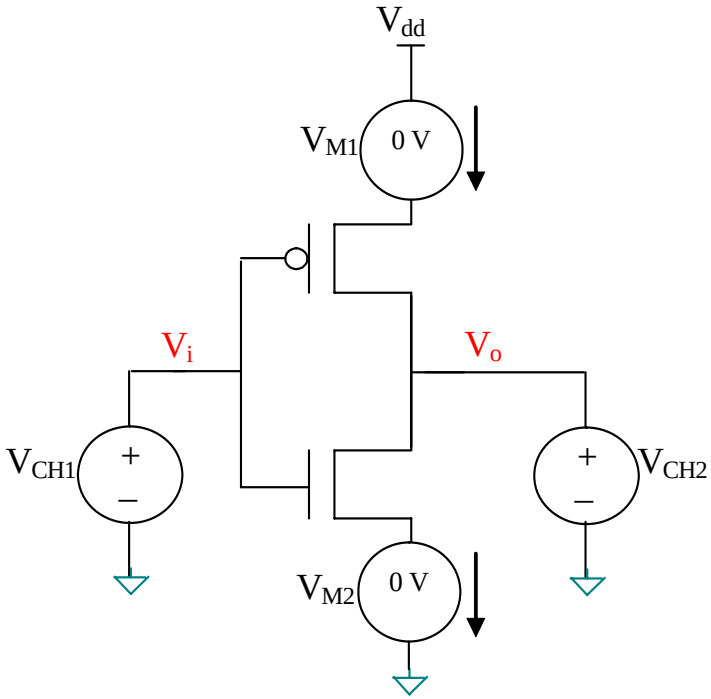


$$C_L \frac{\Delta V_o}{\Delta t} + C_o \frac{\Delta V_o}{\Delta t} + I(V_i, V_o) + C_M \frac{\Delta V_o}{\Delta t} - C_M \frac{\Delta V_i}{\Delta t} = 0$$

$V_o(t_{k+1})$: Calculated based on $V_o(t_k)$ and $V_i(t_k)$, $V_i(t_{k+1})$ and the current source and parasitic capacitance values

$$V_o(t_{k+1}) = V_o(t_k) + \frac{1}{C_L + C_o + C_M} \cdot \left\{ C_M \cdot \left(V_i(t_{k+1}) - V_i(t_k) \right) - I\left(V_i(t_{k+1}), V_o(t_k) \right) \cdot \Delta t \right\}$$

Short Circuit Current Pre-characterization



- $I_{sc}(V_{CH1}, V_{CH2}) = Min\ \{I(V_{M1}), I(V_{M2})\}$
- A new 2-D lookup table is created to store the $I_{sc}(V_{CH1}, V_{CH2})$ values
- Complexity of the CSM does not increase by the SCC pre-characterization

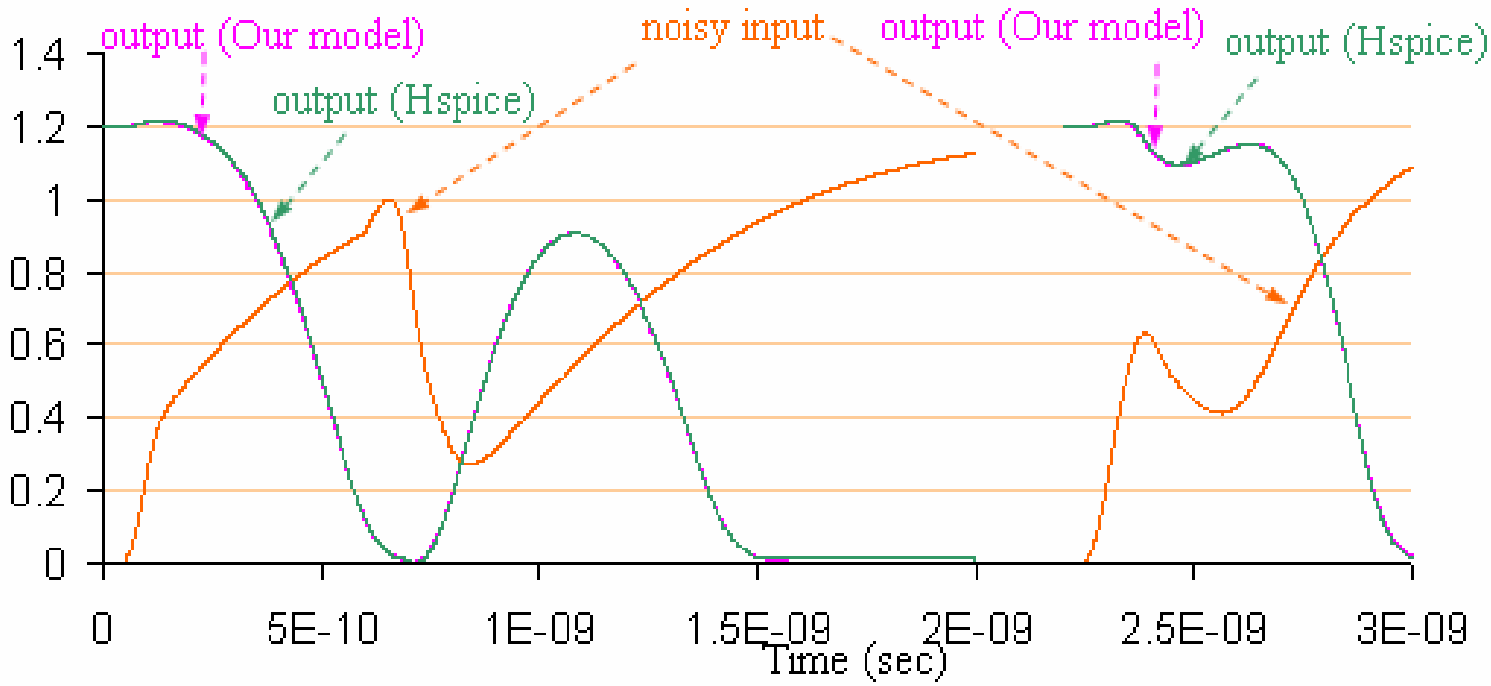
CSM-based Short Circuit Power Calculator (CSPC)

- **Step 1: Construct the output voltage waveform from on the noisy input waveform by using our CSM-based calculator**

- **Step 2: At each time instance, read the corresponding short circuit current from the look up table and thus construct the exact short circuit (SC) current waveform**

- **Step 3: Report the short circuit energy dissipation associated with the input-output transition as the area under the SC current waveform**

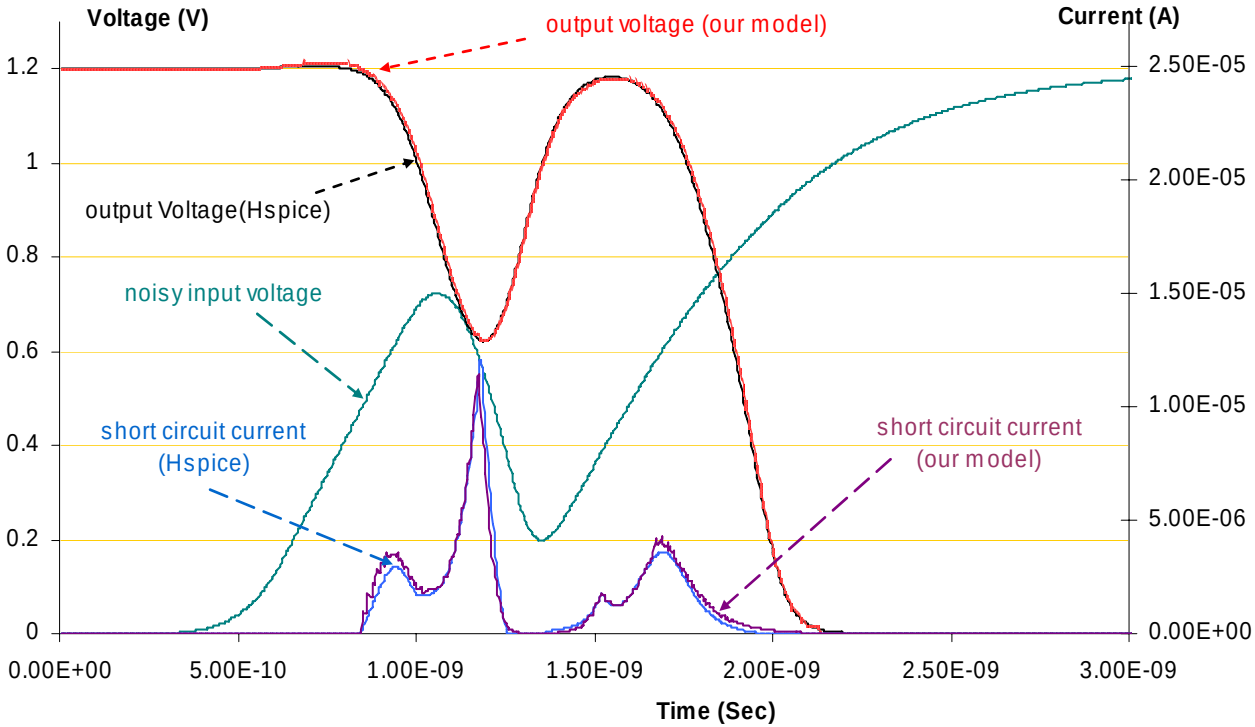
Experimental Results: CSM-based Technique



- **Logic cell: Minimum sized inverter in a 130nm CMOS cell library**
- **HSPICE and our CSM-based calculator results for some (crosstalk-induced) noisy input waveforms**

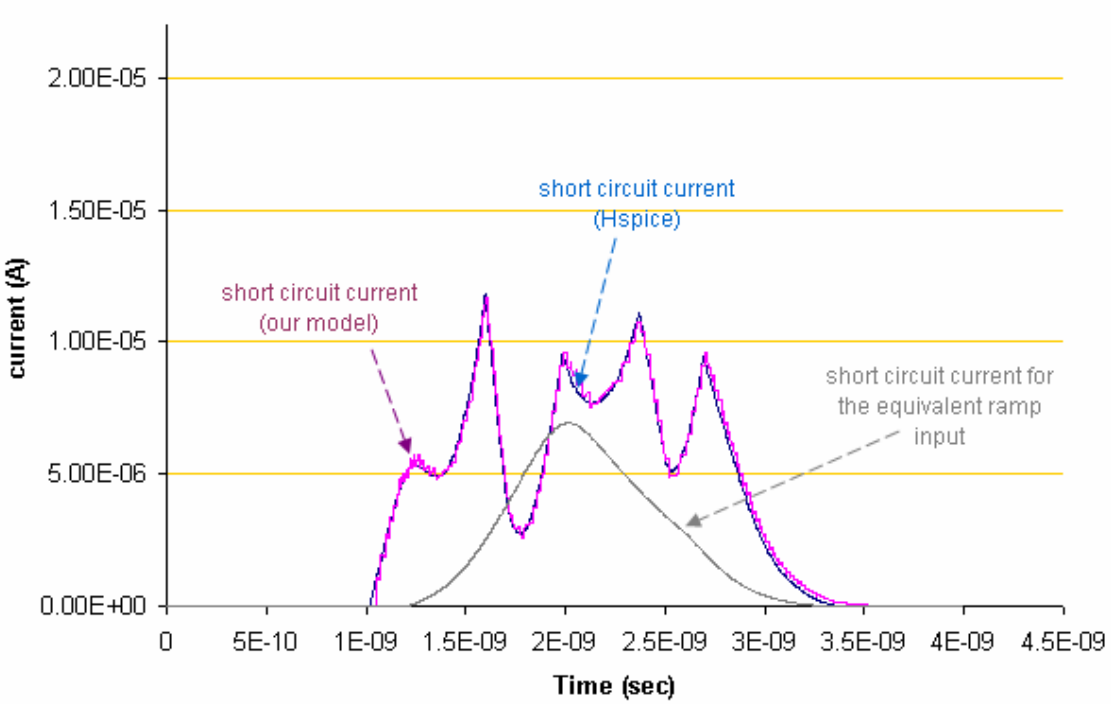
Experimental Results – Accuracy of CSPC

- **Noisy waveform given to a minimum sized inverter with a FO4 loading in our 130nm cell library**
- **Switching energy consumption per transition is 8.89fJ**
- **SC energy dissipation is 2.68fJ (2.78fJ) per Hspice (CSPC)**
- ***E_{sc}/E_{sw}* ratio of 30.1%**



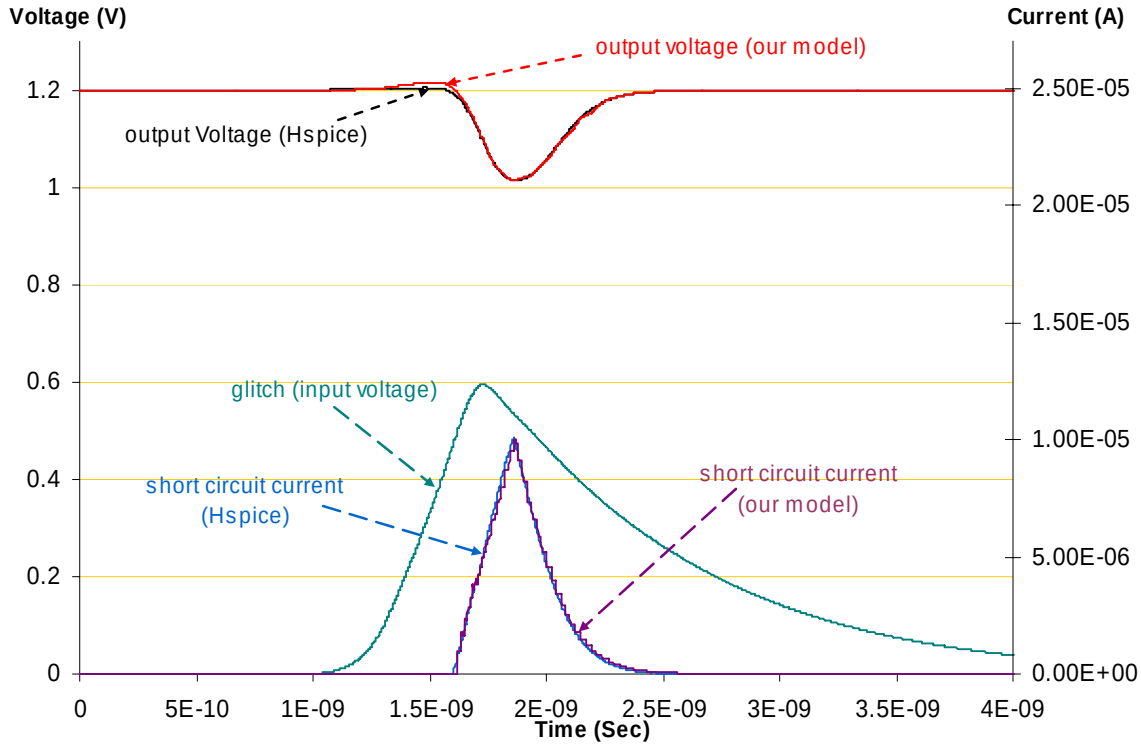
Comparison with Previous Techniques

- **Saturated ramp approximation of input waveform and use of pre-characterized lookup tables $E_{sc}(t_{in},C_L)$**
  - **SC energy dissipation reported by ramp approximation is 7.1fJ**
  - **45.9% error w.r.t. to Hspice short circuit energy report of 15.45fJ**
  - **SC energy dissipation reported by CSPC is 15.61J (1% error)**
  - **Shape of the input waveform should not be ignored**

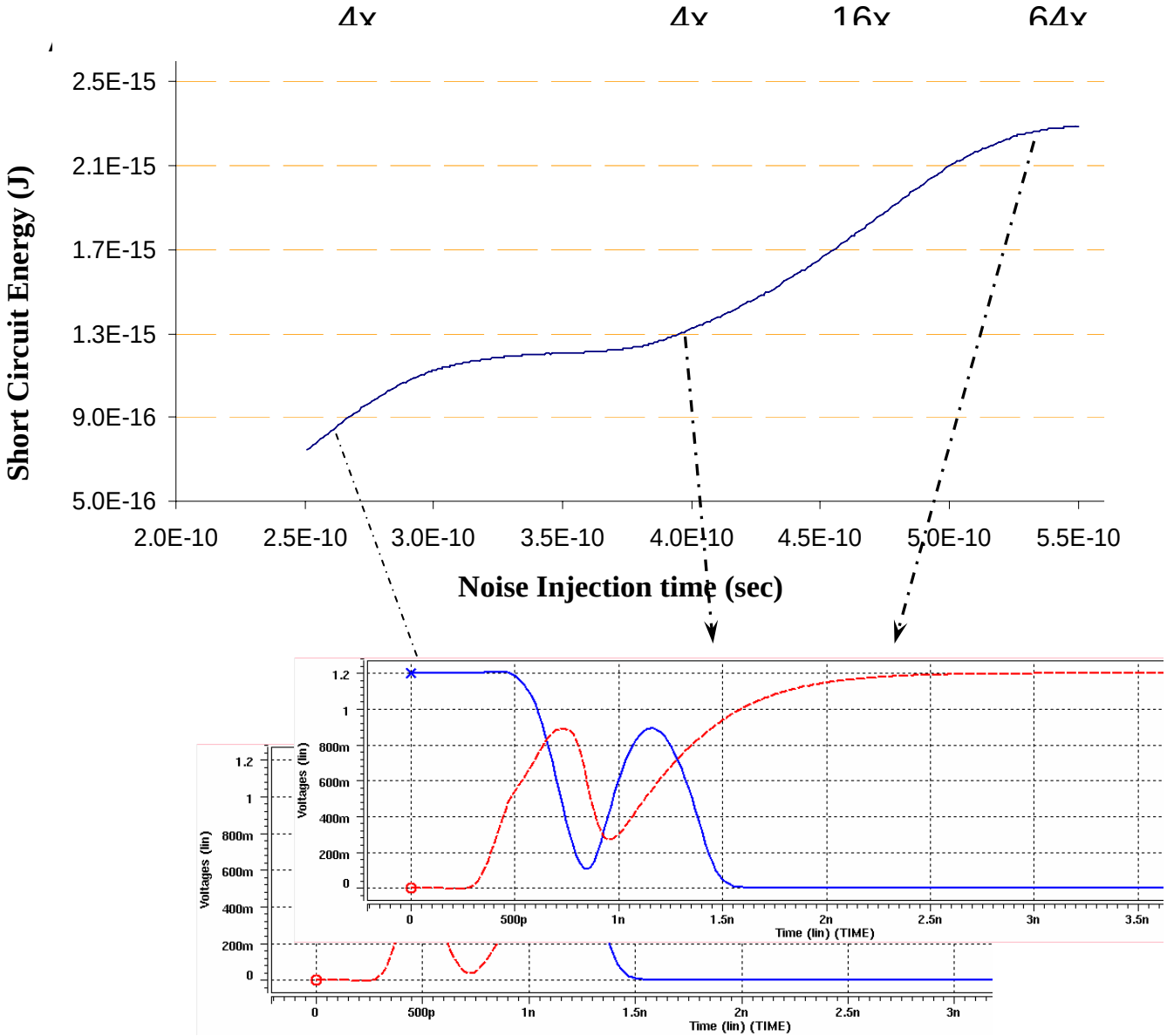


Experimental Results – Glitches

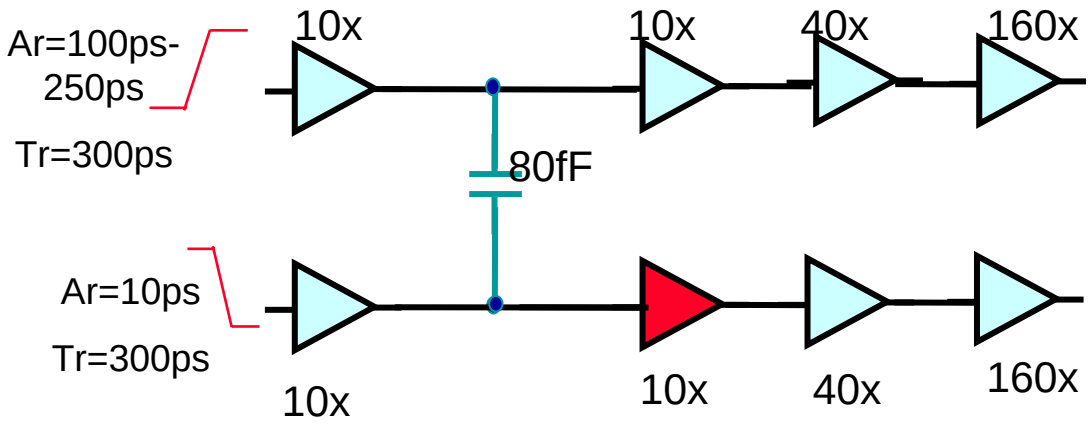
- **Glitches are typically ignored by the timing analysis or a validation tools**
  - **However, the corresponding SC energy dissipation may not be negligible (3.5fJ for the example shown below)**



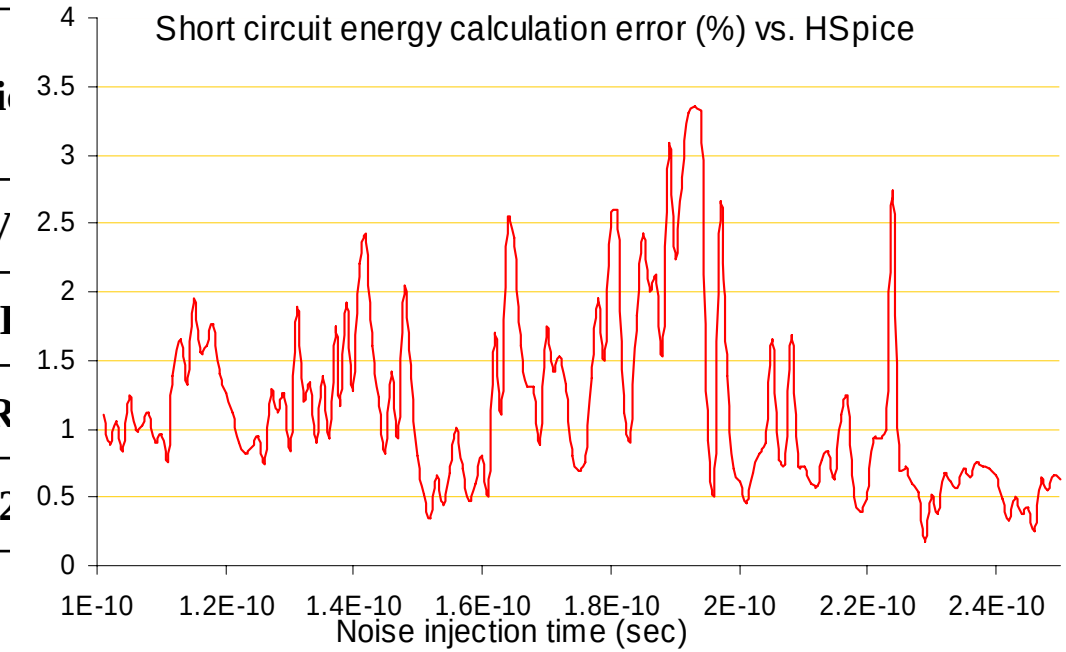
Short Circuit Energy in the Presence of Crosstalk



Accuracy and Runtime of CSPC



Logi		untime peedup
INV		2940
NANI		6120
XOR		15800
AOI2		6750



Conclusion

- **Short circuit energy dissipation increases in the presence of noise such as capacitive crosstalk**
- **Previous short circuit calculation methods are not capable of handling noisy input waveforms**
- **We utilize our CSM-based waveform calculator for the purpose of short circuit current calculation**
  - **The output voltage waveform constructed by the CSM-based calculator is used to estimate the short circuit current and hence the corresponding energy dissipation**
  - **Our model is also capable of calculating the short circuit energy consumption of the glitches.**
- **Hpsice-based experimental results prove the high accuracy of our technique**