On Increasing Signal Integrity with Minimal Decap Insertion in Area-Array SoC Floorplan Design

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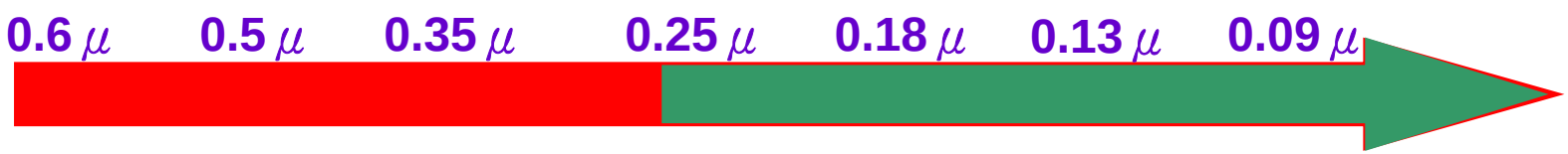
Outline

- Introduction
- Power Delivery and Signal Integrity Issue in Area-Array Design
- Power Supply Noise Aware Floorplanning
- Noise-driven Decap Planning with Minimum Area Insertion
- Experimental Results
- Conclusions

Introduction



IC Design

…… Signal Integrity ……

Signal Net

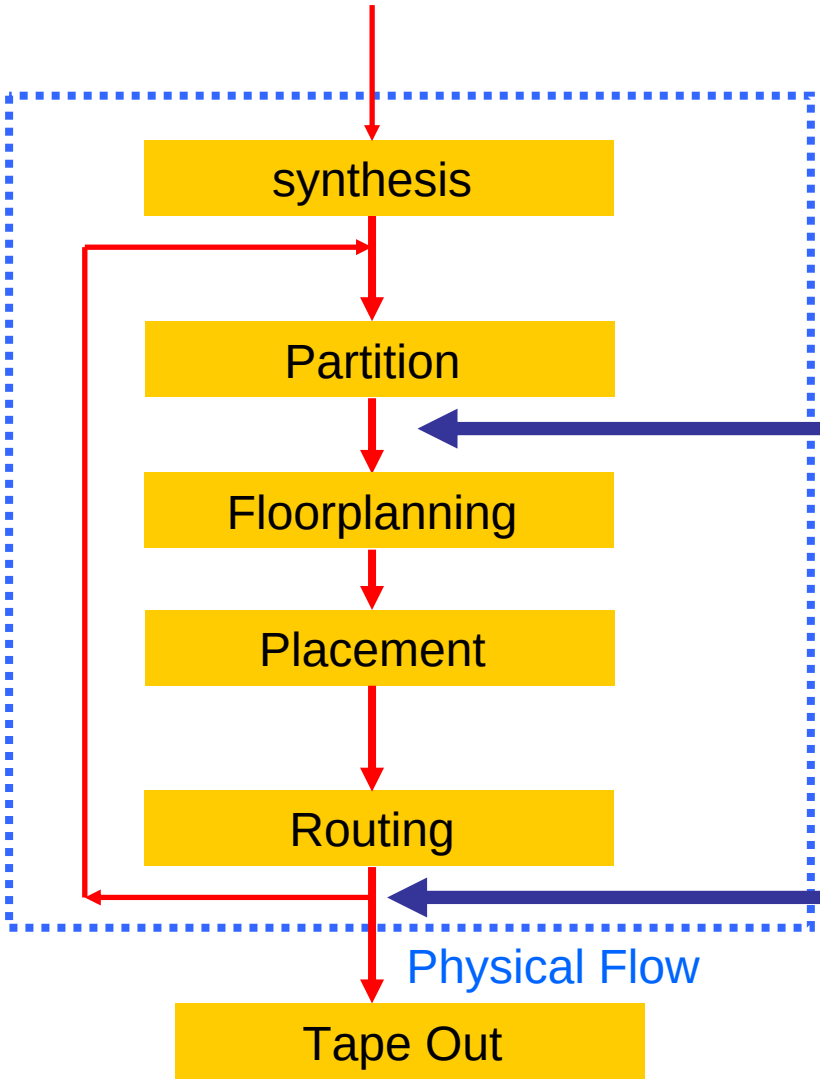
……

Power/Ground Net

IR Drop, $L\frac{di}{dt}$ Noise

Power Supply Noise

Decap Insertion in Physical Synthesis Flow



Modern Design Flow

Decap insertion step

Traditional Design Flow

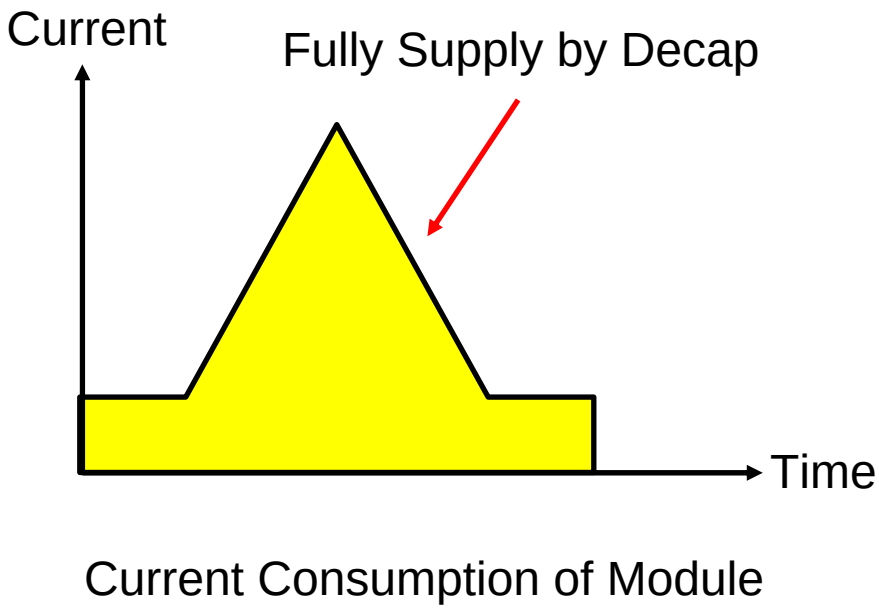
Decap insertion step

Recent Works on Decap Insertion Method

- S. Zhao et al., “Decoupling Capacitance Allocation and Its Application to Power-Supply Noise-Aware Floorplan”. In *TCAD,* pages 81–92, 2002.
- J.T. Yan et al, “Decoupling capacitance allocation in noise-aware floorplanning based on DBL representation”. In ISCAS, pages 23–26, 2005.
- C.Y. Yeh et al, “Timing-aware power noise reduction in layout”. In *DAC*, pages 627–634, 2005.

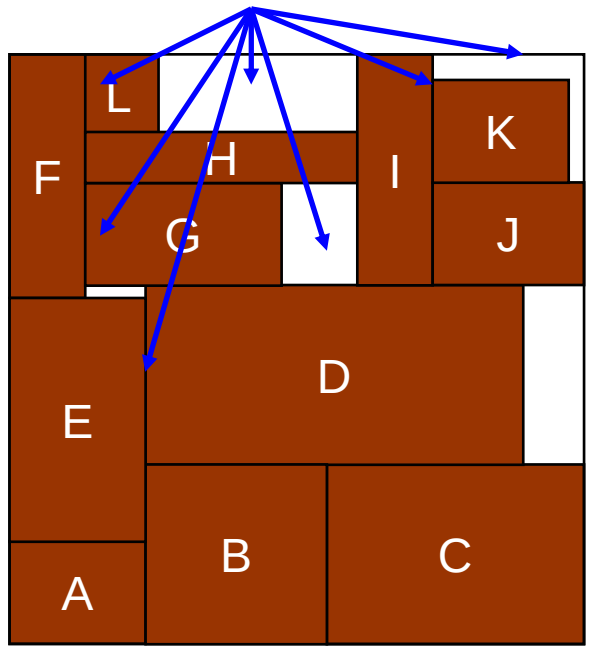
Motivation

- In previous works
  - Decap budget is overly estimated
  - Floorplan space is not fully used



Current Consumption of Module

Many available space can be used in one floorplan



Problem Formulation

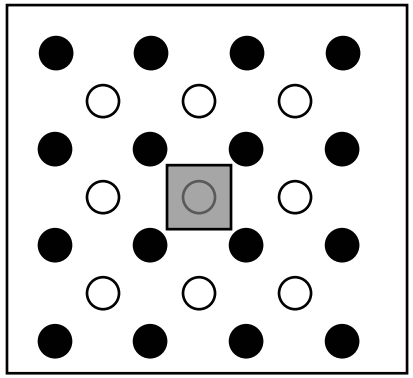
Input :

Given a set of blocks and the noise constraint for each block

Output :

Obtain the optimal block location and insert minimum decaps into floorplan result to satisfy its required constraint with minimal extra extensive area

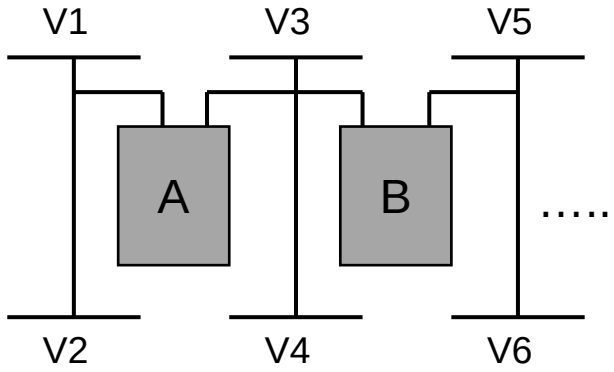
Power Delivery Model and Noise Estimation



● : Power and Gnd bump

○ : Signal bump (area array pad)

▭ : Module



$$V_{noise}^{(k)} = \sum_{P_j \in T^k} i_j R_{P_{jk}} + L_{P_{jk}} \frac{di_j}{dt} \quad .....(1)$$

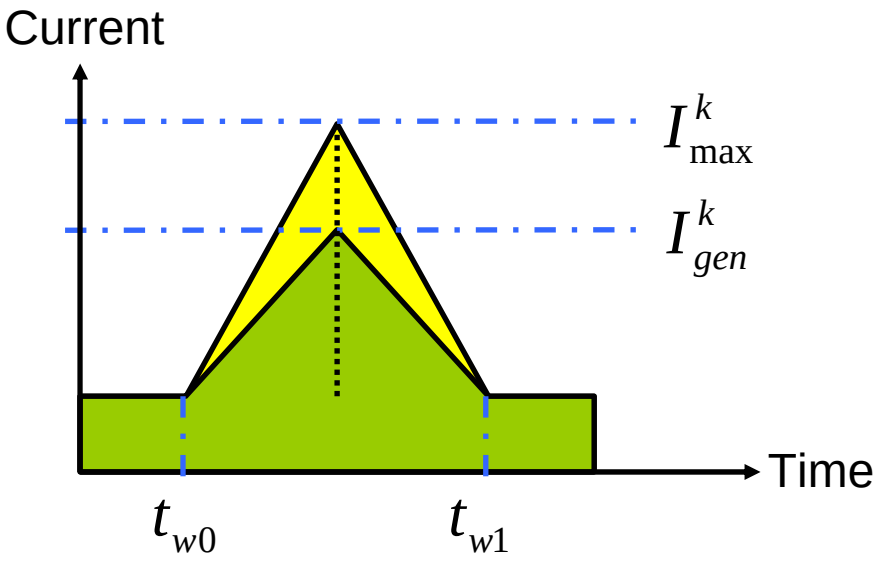
$V_{noise}^{(k)}$: power supply noise at module k

R : resistance

P_{jk} : path from node j to node k

i : current

Decap Budget Computation



I^k_{max} : maximum switching current of module k

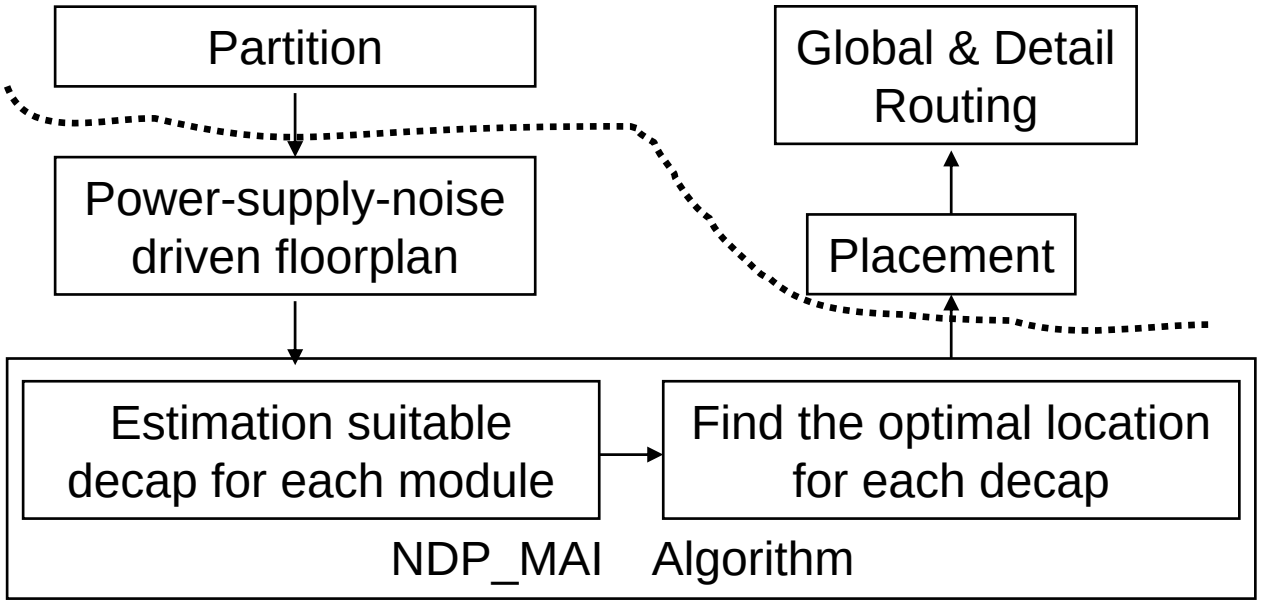
I^k_{gen} : general switching current of module k

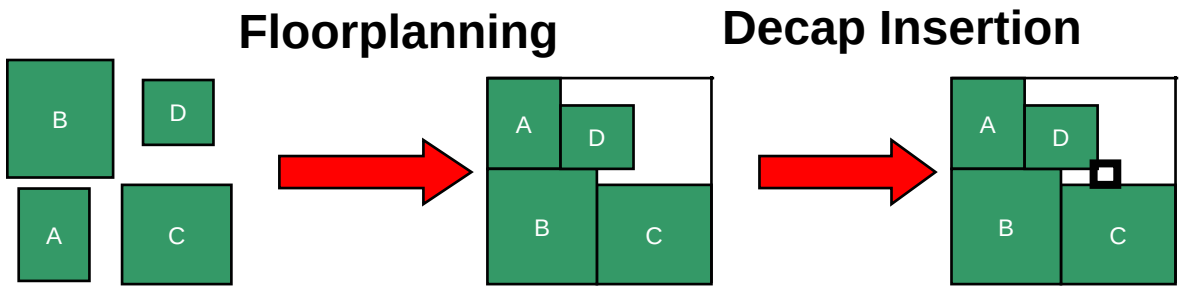
$$Q^k = \int_{t_{w0}}^{t_{w1}} I^k_{max}(t)dt - \int_{t_{w0}}^{t_{w1}} I^k_{gen}(t)dt \ldots\ldots\ldots (2)$$

Method	Decap	Drop V.
Initial	0pF	2.44V
[15]	112pF	2.471V
Eq(2)	96pF	2.46V

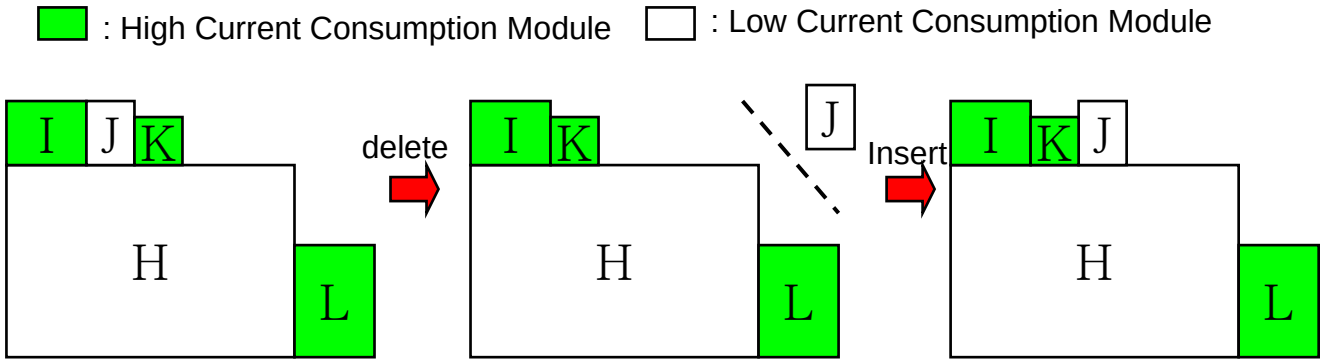
[15]:S.Zhao, K. Roy and C.K. Koh. “Decoupling Capacitance Allocation and Its Application to Power-Supply Noise-Aware Floorplan” TCAD pp. 81-92, Jan. 2002

Minimal Decap Allocation in Power Supply Noise Aware Floorplanning

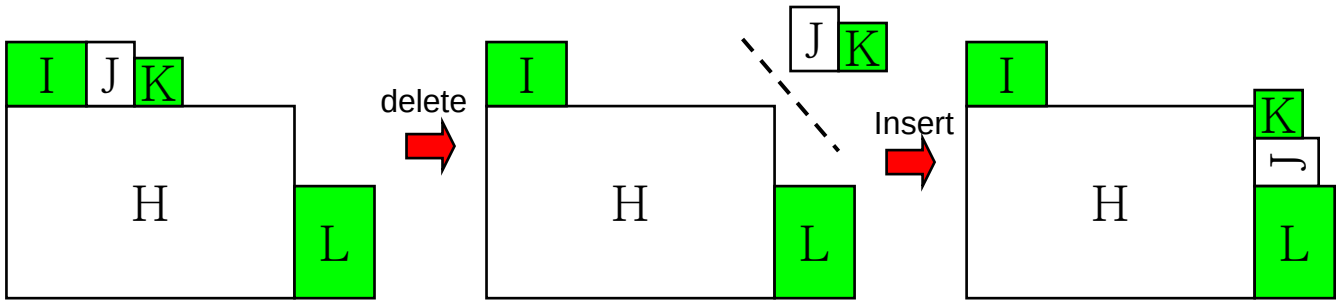




O-Tree Based Power Supply Noise Aware Floorplan



(A) Using the traditional operation to change a floorplan

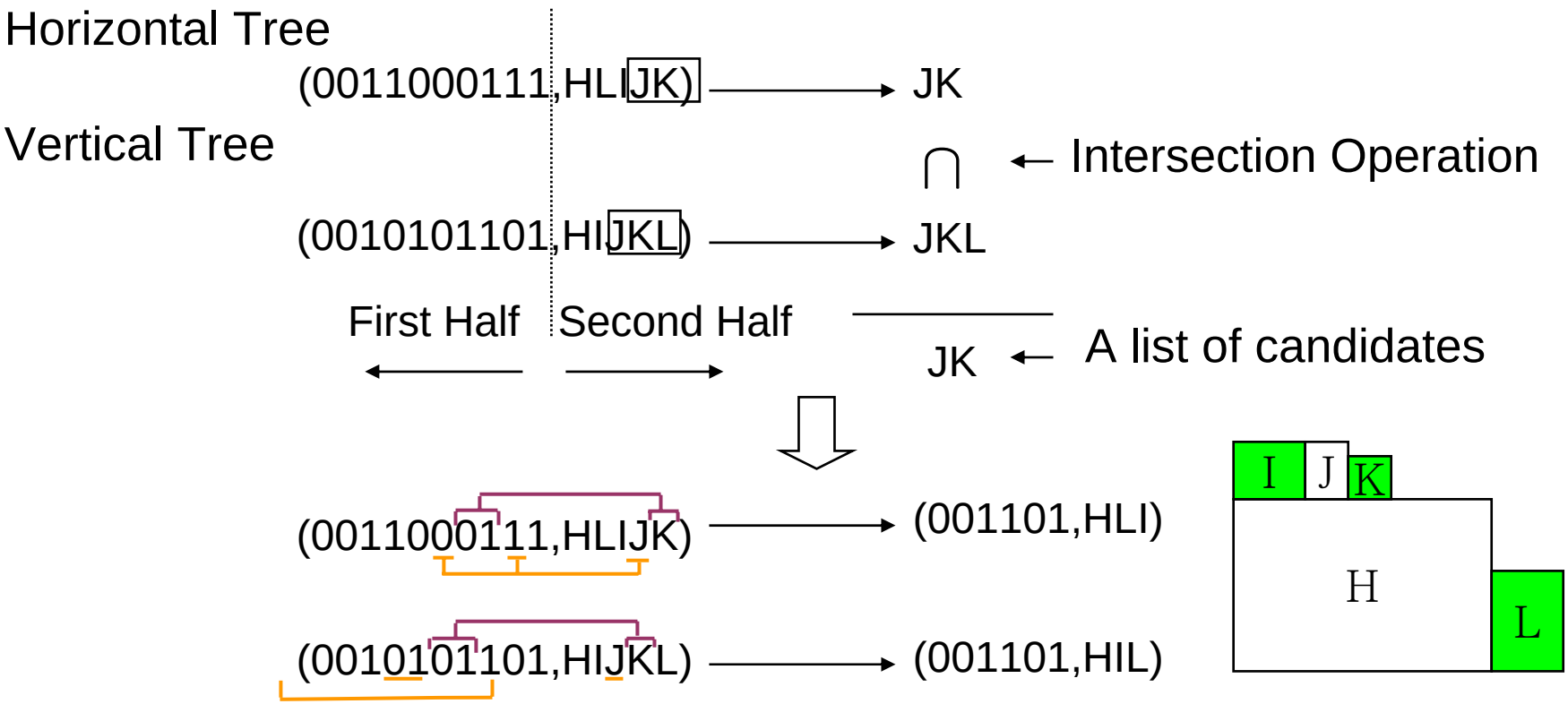


(B) Using the new operation to change a floorplan

O-tree Advantage

Type of repreaentation		1 to 1	P-admissible	Adjacent relationship
List	SP	Yes	Yes	Bad
Graph-based	B*-tree	No	No	Middle
	TCG	Yes	Yes	Middle
	DBL	Yes	Yes	Middle
List – Graph-based	O-tree	No	No	Best
	CBL	No	No	Middle
	SCP	Yes	Yes	Middle

Delete Operation (1/2)



Delete Operation (2/2)

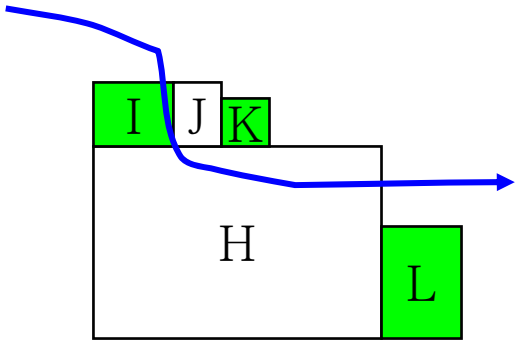
Delete Block J

(0011000111,HLIJK)

∩

(0010101101,HIJKL)

JK



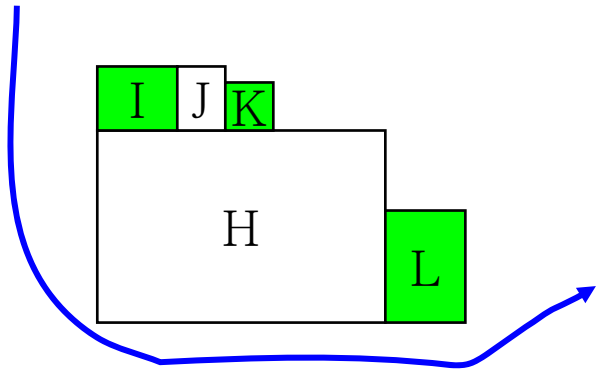
Delete Block H

(0011000111,HLIJK)

∩

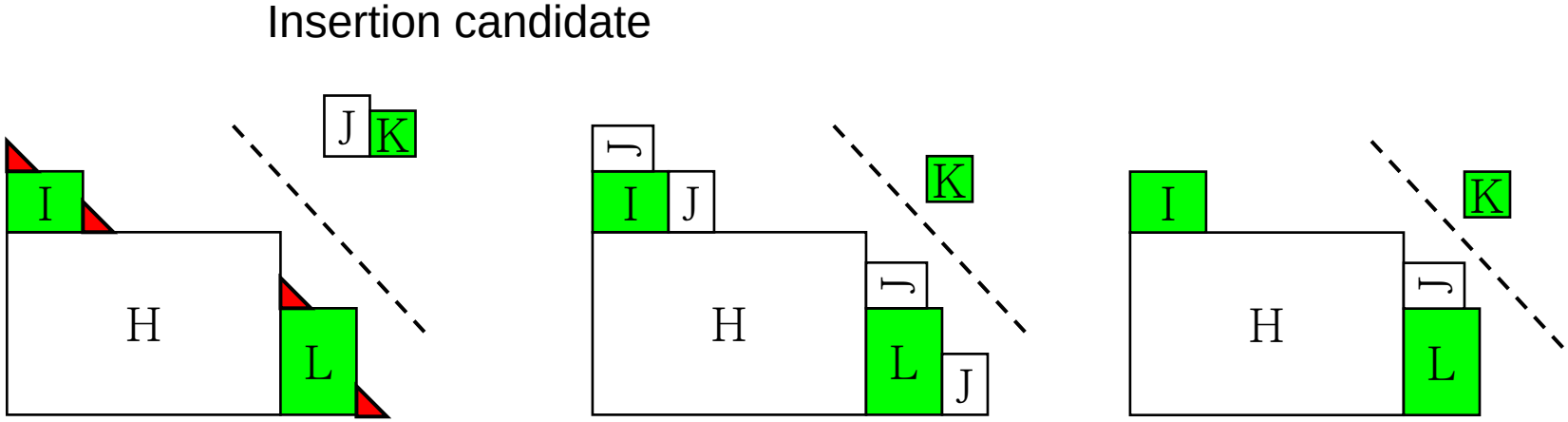
(0010101101,HIJKL)

HLIJK



Insert Operation

: the possible insertion location in this floorplan



(A) Find all possible location (B) Compute cost (C) Choose optimal location

$$C_a = D_1(A_{new} - A_{original}) + D_2(I_a + I_b + I_c) \quad \text{.....} \quad (3)$$

C_a : cost function of module insertion

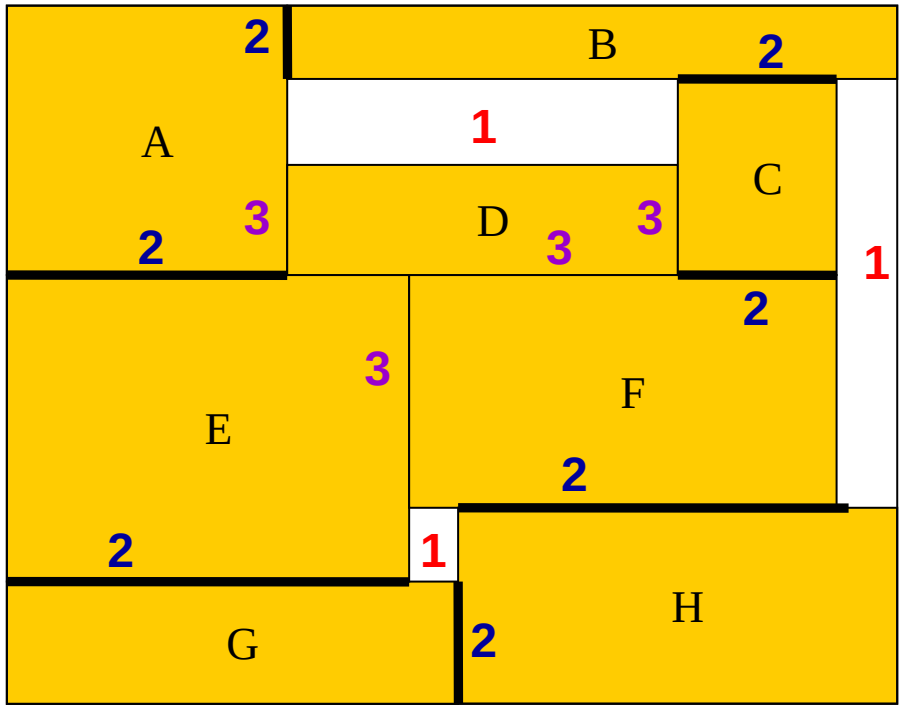
Noise-Driven Decap Planning with Minimal Area Insertion

Space on Floorplan

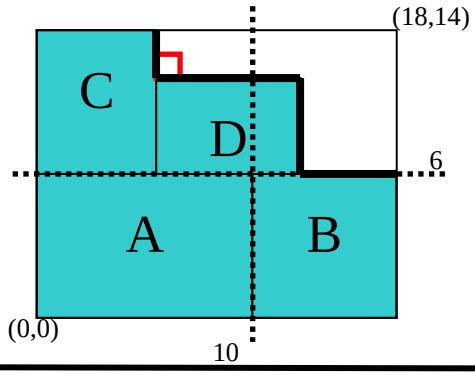
(1) : Empty Space : can not used by any block

(2) : Extensive Space : between any pair adjacent blocks in longest path block list

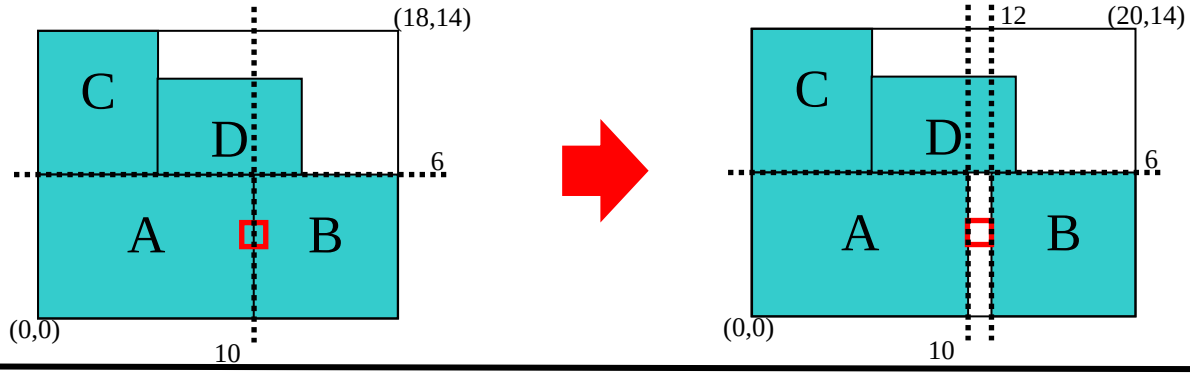
(3) : Available Space : besides the empty space and the extensive space



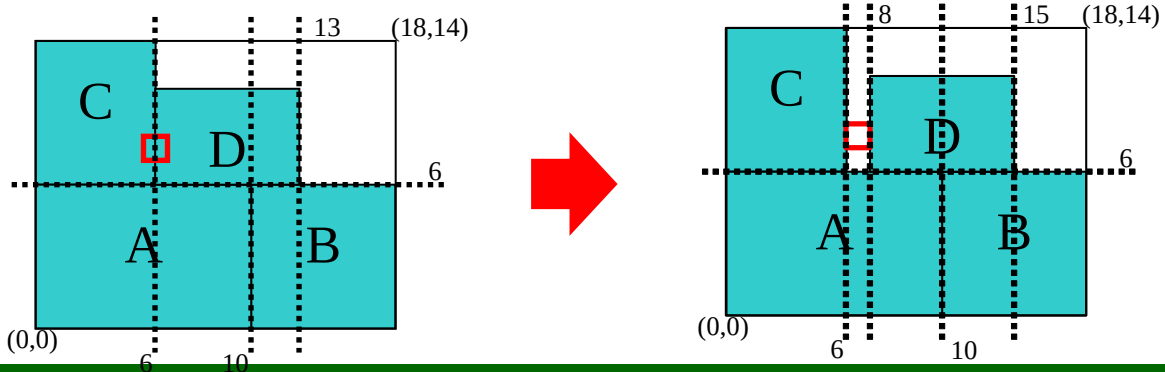
The Effect of Decap Insertion



(1) : Empty Space
Priority Value : 1



(2) : Extensive Space
Priority Value : 3



(3) : Available Space
Priority Value : 2

NDP_MAI Algorithm

Step 1 : Find one non-planned module, i

Step 2 : If (I^i_{gen} >= $I^i_{\max}$) do nothing for this module;
goto Step 1

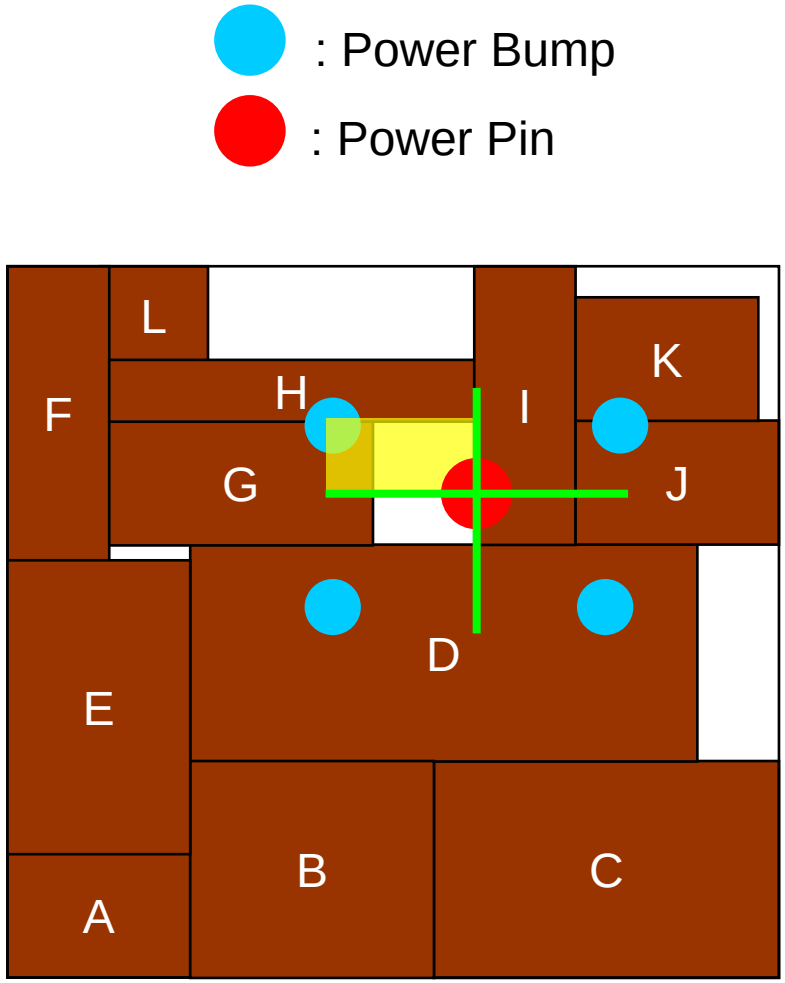
Step 3 : Compute Require Decap Size

Step 4 : Decap cut apart into four small decap

Step 5 : Find the feasible region of the decap;

Step 6 : Fix all dead space and the channel space

Step 7 : Compute cost for each space and choose minimum cost



Experimental Results – Effective Decap Budget

Circuit	Ours	[15] (greedy)	[15] (iterative)	Improved Ratio
apte	7.01	16.32	13.46	47%
hp	1.65	3.41	2.75	40%
xerox	3.09	6.96	5.71	46%
ami33	0.08	0.31	0.27	70%
ami49	3.61	10.7	9.08	60%

[15]:S.Zhao, K. Roy and C.K. Koh. “Decoupling Capacitance Allocation and Its Application to Power-Supply Noise-Aware Floorplan” TCAD pp. 81-92, Jan. 2002

Experimental Results – Area Increase

Circuit	Pre Area(μm^2)	Post Area(μm^2)	Area Increase (μm^2)	[15]Area Increase (μm^2)	[12]Area Increase (μm^2)
apte	47761324	47780360	19036	469916	35400
hp	9940140	10097780	157640	317503	67000
xerox	20630210	20705216	75006	269374	144000
ami33	1241440	1245266	3824	390	11000
ami49	37504880	37659870	154990	218000	217000

Maximum current consumption = 1.05~1.2 * average current consumption

[12]:J.T Yan, K.P Lin and Y.H. Chen . “Decoupling capacitance allocation in noise-aware floorplanning based on DBL representation”, ISCAS pp. 23-26, May. 2005

[15]:S.Zhao, K. Roy and C.K. Koh. “Decoupling Capacitance Allocation and Its Application to Power-Supply Noise-Aware Floorplan” TCAD pp. 81-92, Jan. 2002

Conclusion

- We have improved noise estimation model and obtained less decap area
- We adopt strong adjacent module relation O-tree representation for floorplannin and modify the primary operations *Delete* and *Insert* so that they be used in our framework
- Minimal Decap Insertion and blocks and decaps legalization are performed in our work

Thanks for Your Attention !