Fast Flip-Chip Pin-Out Designation Respin by Pin-Block Design and Floorplanning for Package-Board Codesign

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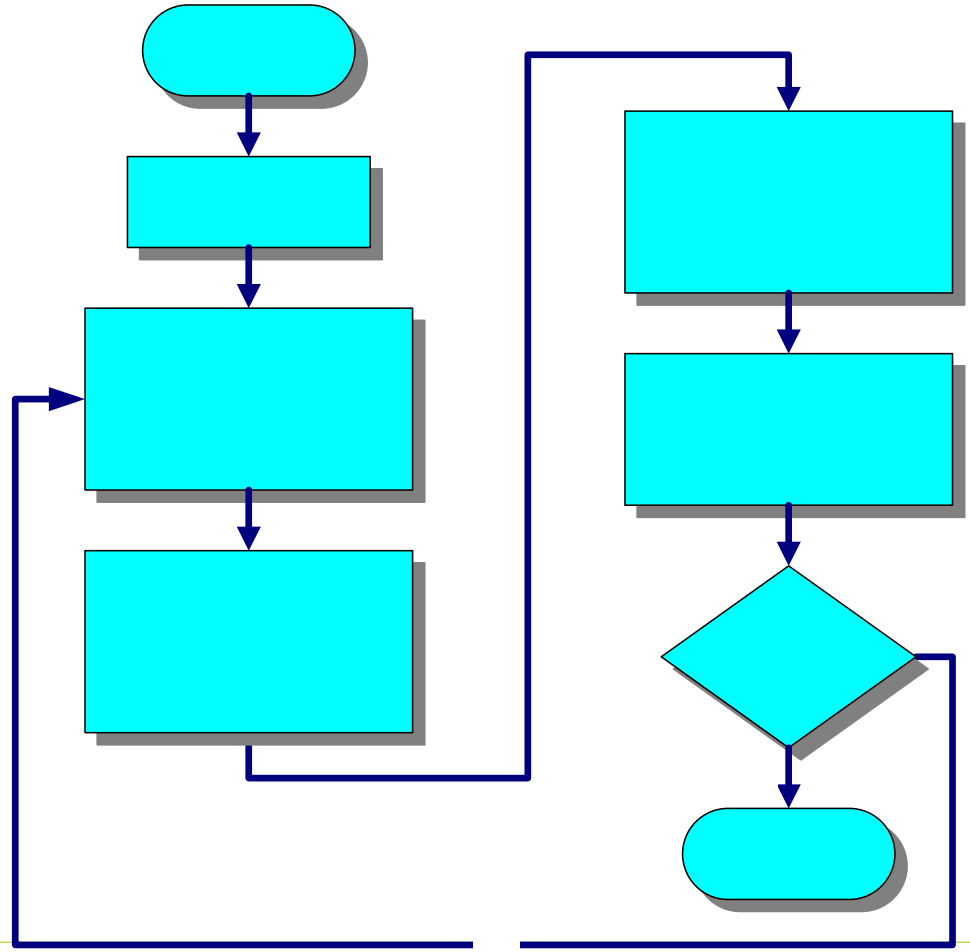
Outline

- Introduction and Motivation
- Proposed design flow
- Constraints and Considerations
- Pin-Block Design and Floorplanning
- Experimental Results
- Conclusion

Introduction—

Conventional Design Flow of Chip-Package-Board Codesign



Motivation

- To speed up turn around time of chip-package-board codesign
- To account for practical experience and techniques in automatically designing interface
- To optimize package size

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- **Proposed design flow**
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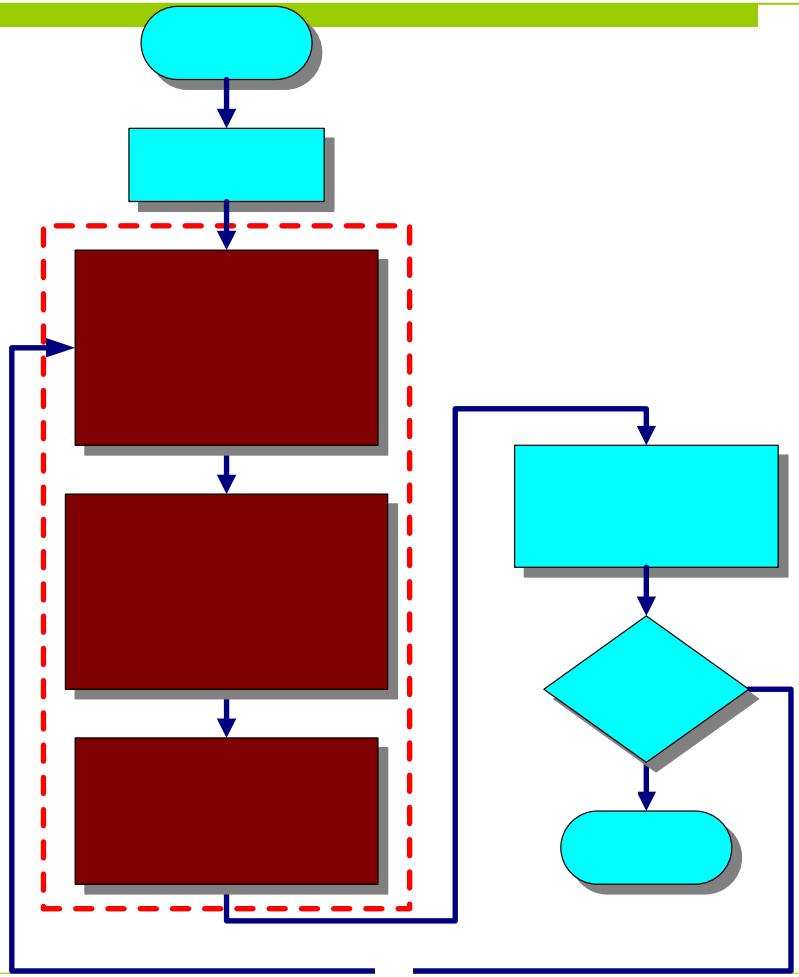
Proposed Design Flow

(Chip-Package-Board Codesign)



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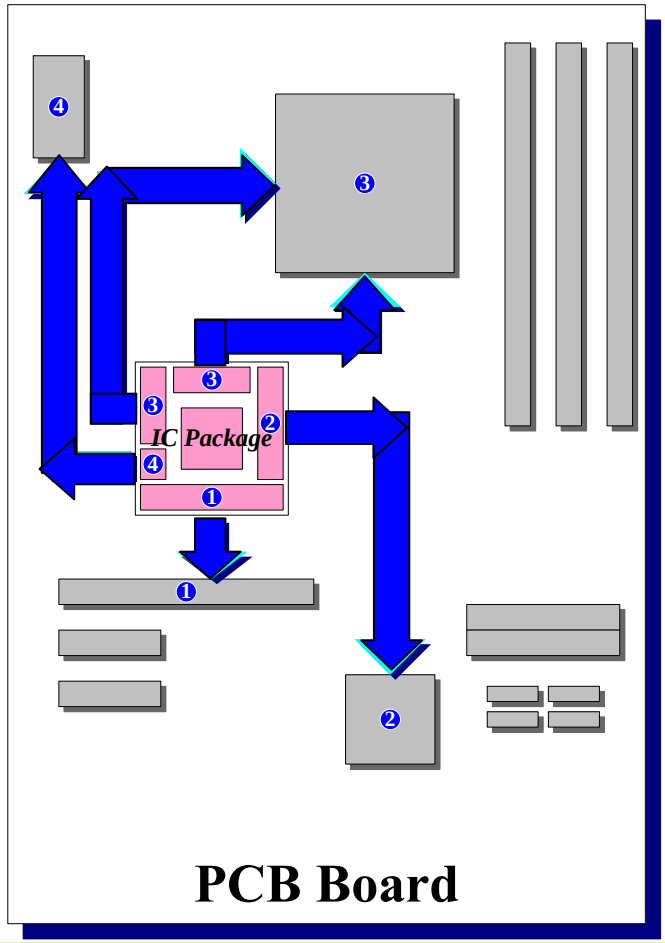
Constraints and Considerations (1/5)

- **A general layout of PCB board.**

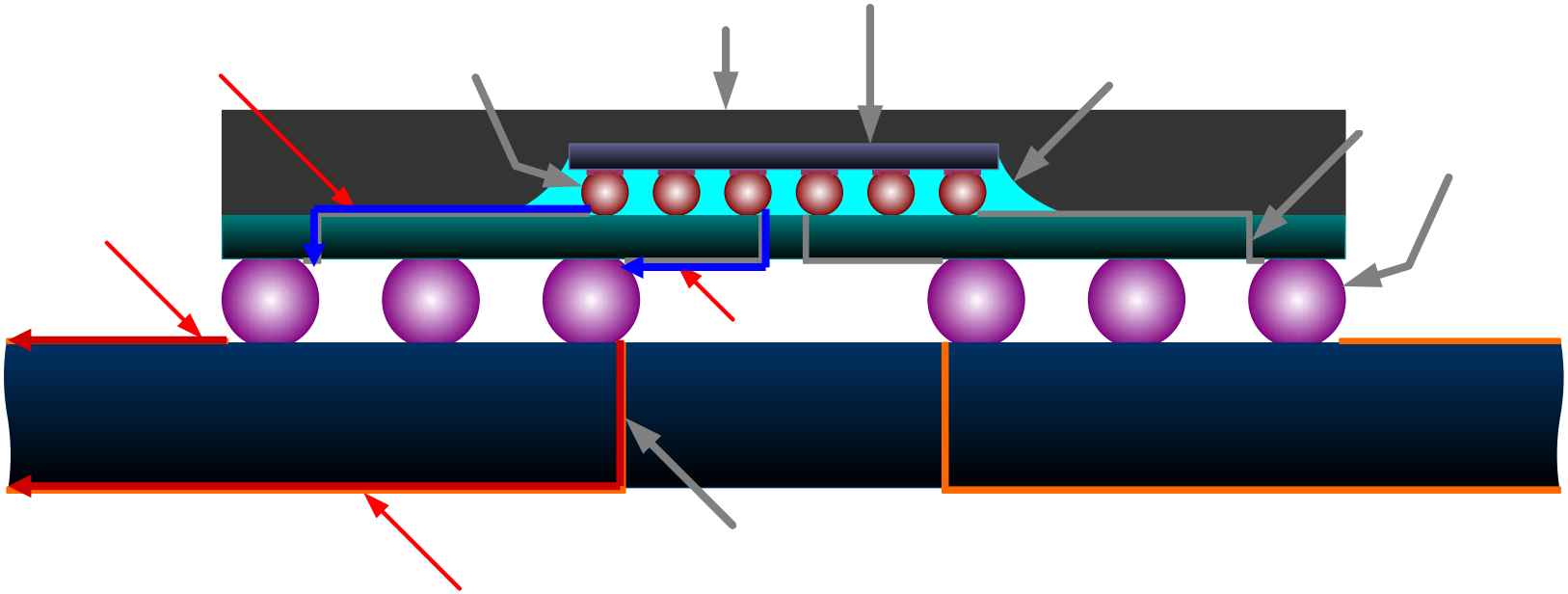
$$V_{SSN} = NL_{tot}\frac{dI}{dt}$$

$$\begin{pmatrix} V_{SSN}: \textit{Simultaneous Switching Noise} \\ N: \textit{Number of drivers switching} \\ L_{tot}: \textit{Equivalent inductance in current loop} \end{pmatrix}$$



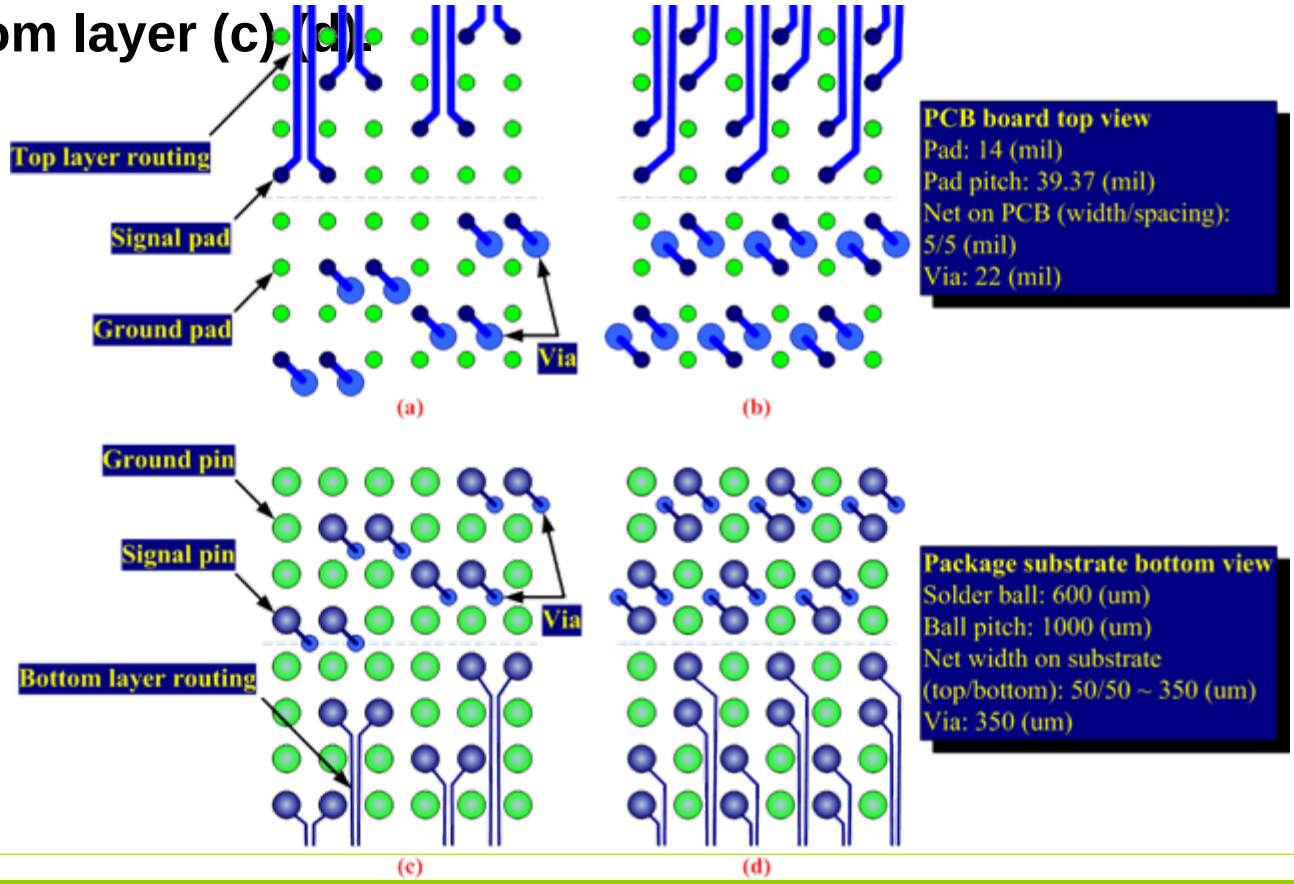
Constraints and Considerations (2/5)

- Die-Package-PCB cross-section view



Constraints and Considerations (3/5)

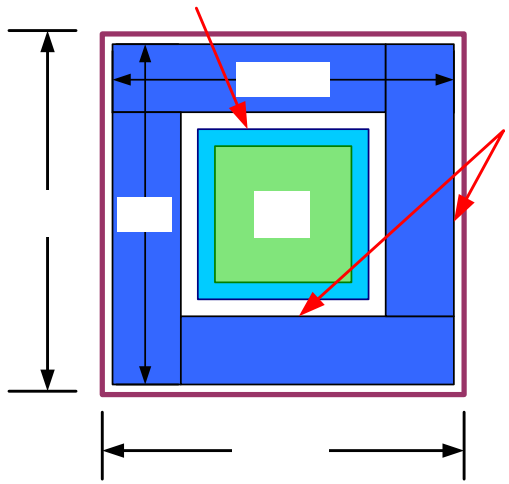
- The routing pattern on PCB top layer (a) (b) and package bottom layer (c) (d).



Constraints and Considerations (4/5)

- **The row number of signal-pin with different package size.**
  - ✓ **(ball pitch=1.0mm, net width=5 mil, net spacing = 5 mil, for four layer PCB board).**

Package size (mm) (Width x Height)	Pin number (Row x Column)	Row number of outer-pin (power-pin, ground-pin and signal-pin)		Row number of outer-pin (signal-pin only)	
		Max.	Avg.	Max.	Avg.
37.5 x 37.5	36 x 36	9	8	7	6
35 x 35	34 x 34	9	8	7	6
31 x 31	30 x 30	9	8	7	6
27 x 27	26 x 26	9	8	7	6
...	...	9	8	7	6



(Top View)

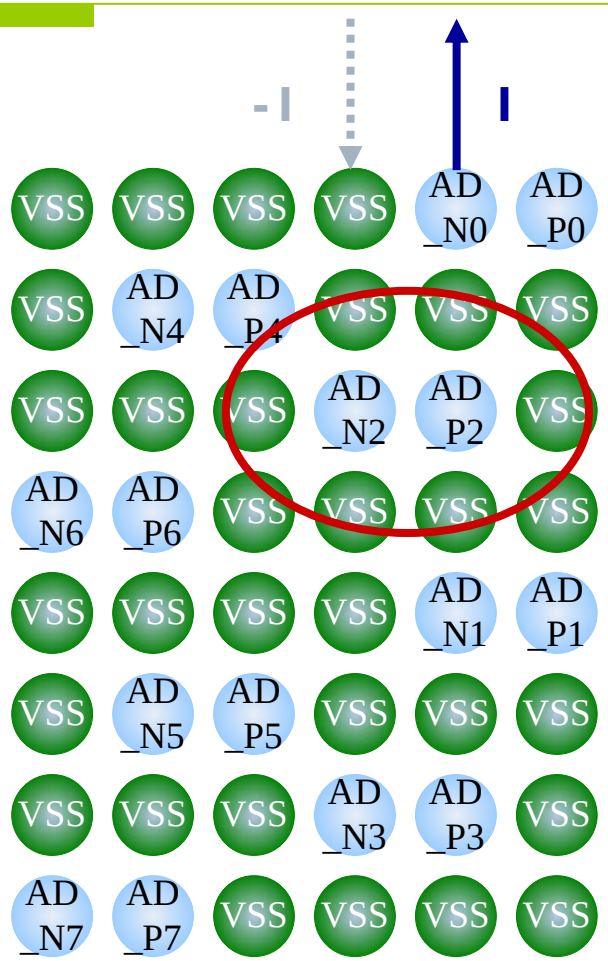
Constraints and Considerations (5/5)

- Return path pin
- Shielding pin

$$I_{noise,C_m} = C_m \frac{dV_{driver}}{dt}$$

I_{noise,C_m} : *Noise induced by mutual capacitor*

C_m : *Mutual capactance*



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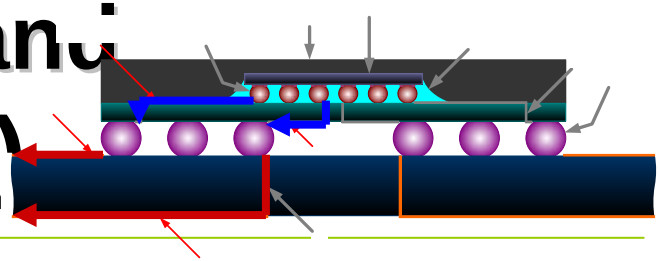
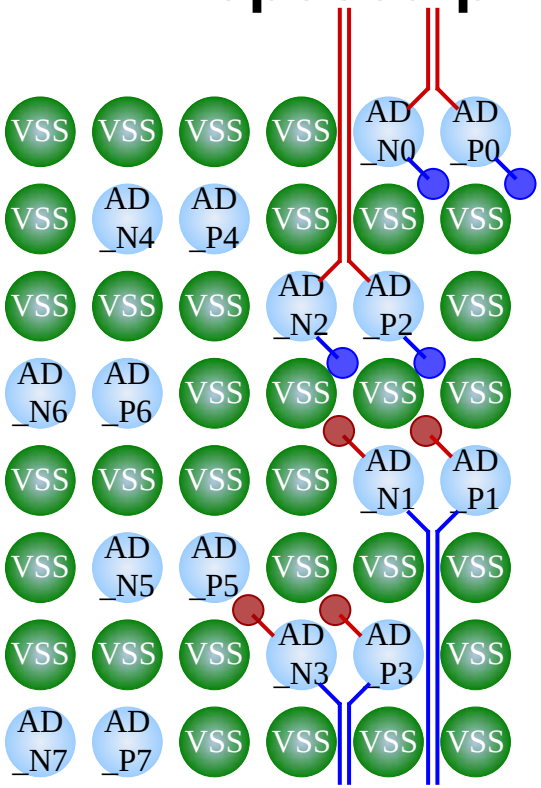
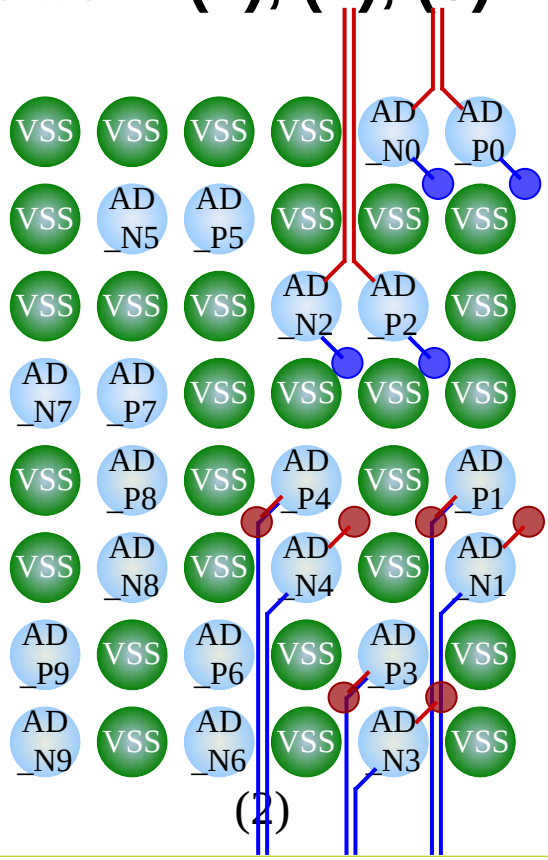
Pin-Block Design and Floorplanning (1/6)



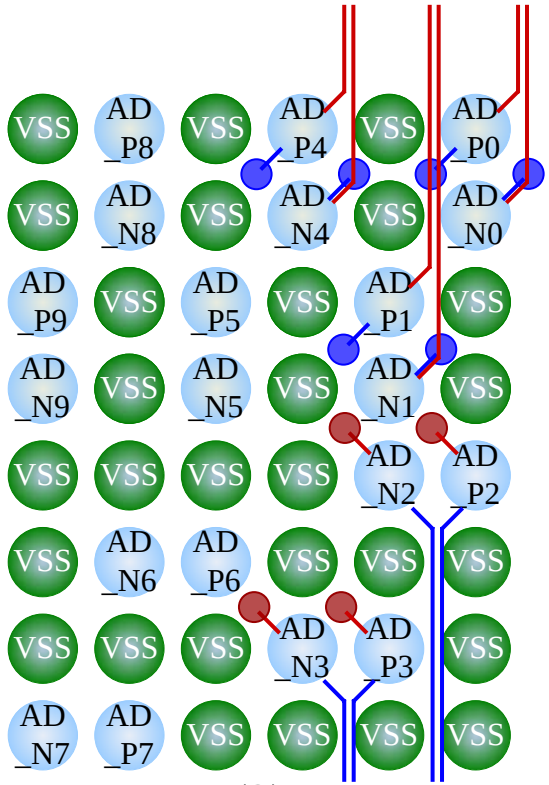
- Proposed pin pattern (1), (2), (3)



(1)

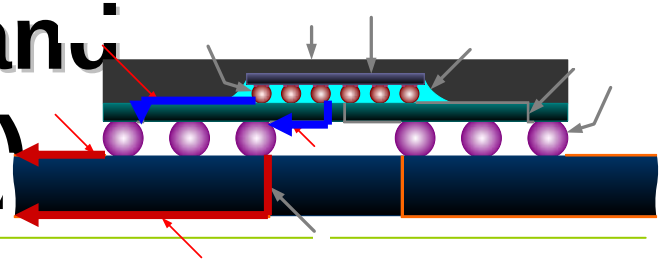


(2)

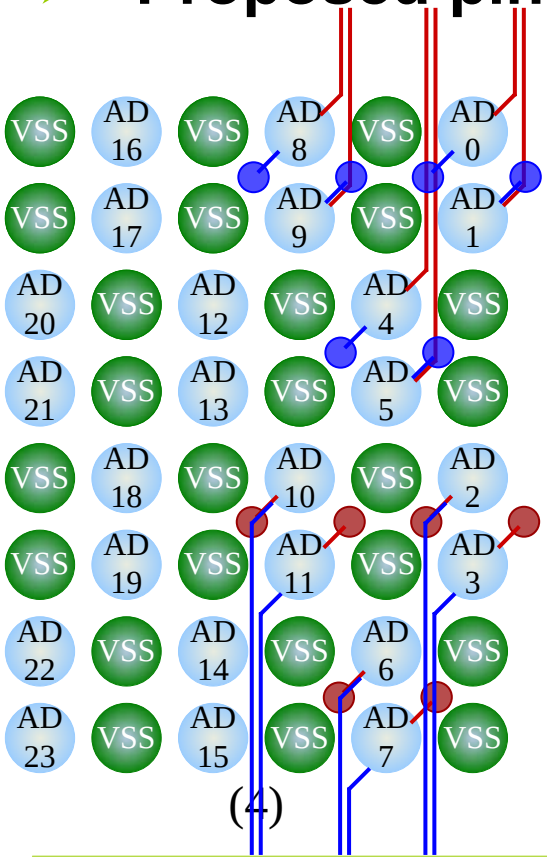


(3)

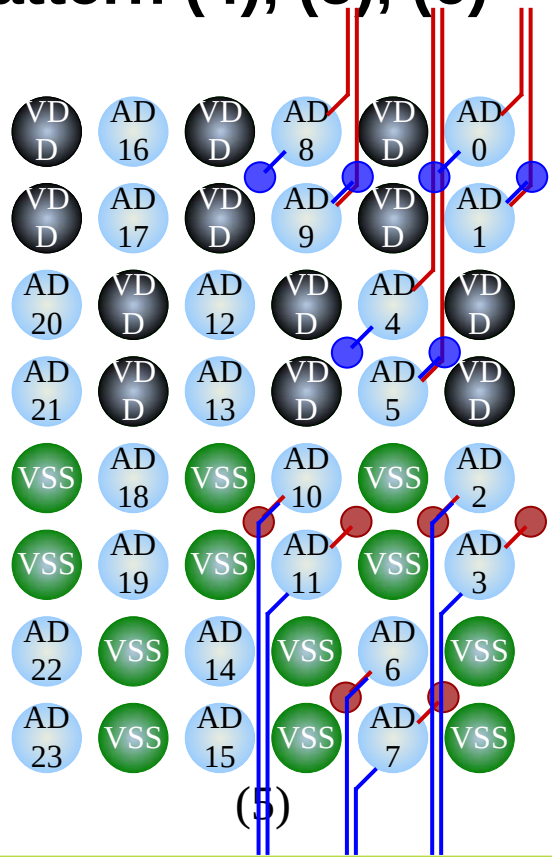
Pin-Block Design and Floorplanning (2/6)



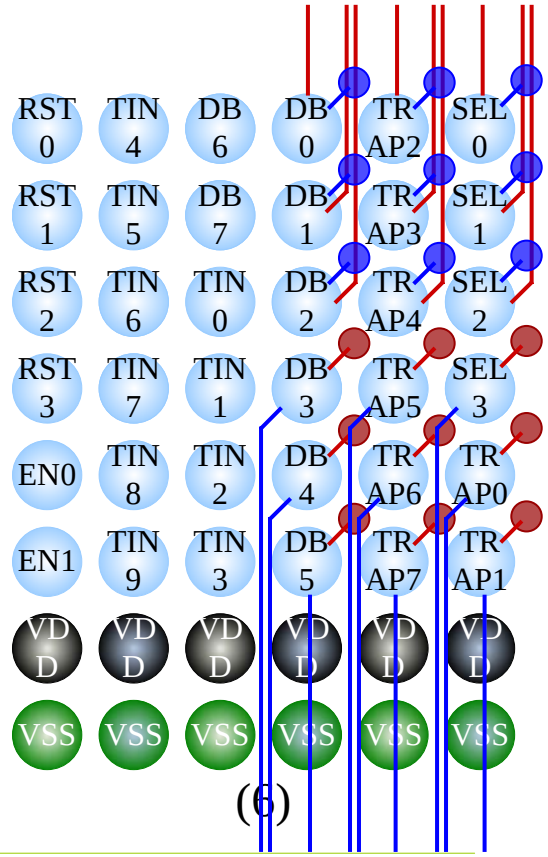
- Proposed pin pattern (4), (5), (6)



(4)



(5)



(6)

Pin-Block Design and Floorplanning (3/6)

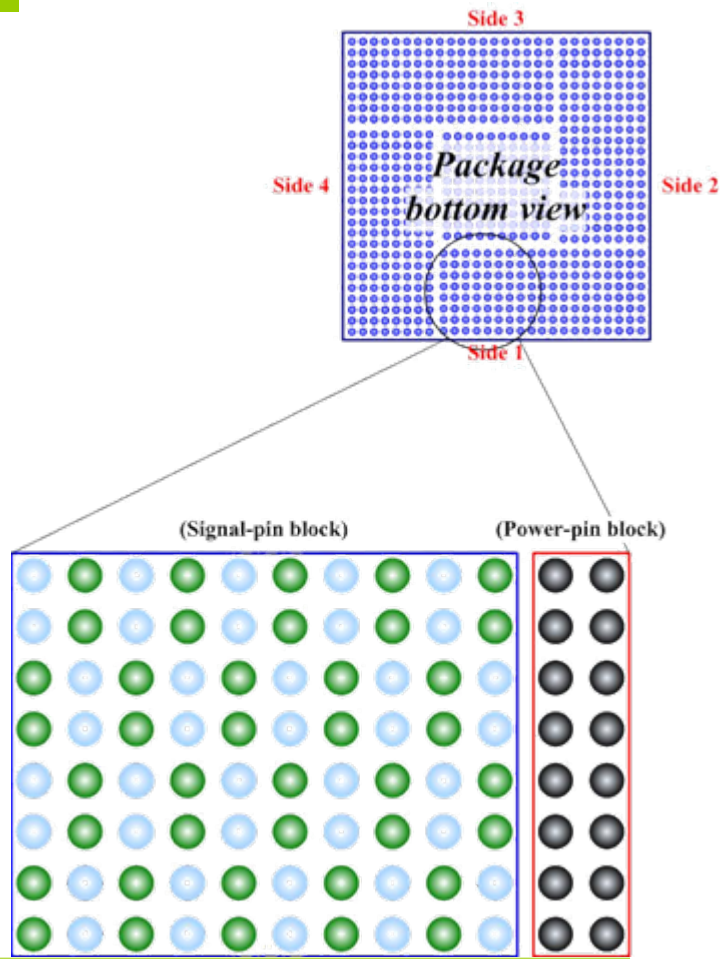
- **Characteristics of signal-pin patterns.**
  - ✓ **Applications, pin-designation efficiency, pin-to-pin crosstalk immunity, net balance, ..., etc.**

	Application	Signal-pin NO.	Pin-to-pin crosstalk immunity	Net balance				Signal shielding on package substrate (Power/Ground)		Power delivary aware	Pin-designation efficiency
				PCB board		Package substrate					
				Top layer	Bottom layer	Top layer	Bottom layer	Top layer	Bottom layer		
Pattern (1)	Differential signal	16	Excellent	Good	Good	Good	Good	Ground	Ground	Without	Not good
Pattern (2)	Differencial signal / Single-ended signal	20	Good	Good	Good	Good	Not good	Ground	Ground	Without	Average
Pattern (3)	Differencial signal / Single-ended signal	20	Good	Not good	Good	Good	Good	Ground	Ground	Without	Average
Pattern (4)	Differencial signal / Single-ended signal	24	Excellent	Not good	Good	Good	Not good	Ground	Ground	Without	Good
Pattern (5)	Differencial signal / Single-ended signal	24	Excellent	Not good	Good	Good	Not good	Power	Ground	With	Good
Pattern (6)	Single-ended signal	36	Not good	Not good	Not good	Not good	Not good	None	None	With	Excellent

Pin-Block Design and Floorplanning (4/6)

- An example of pin configuration chart and pin block.

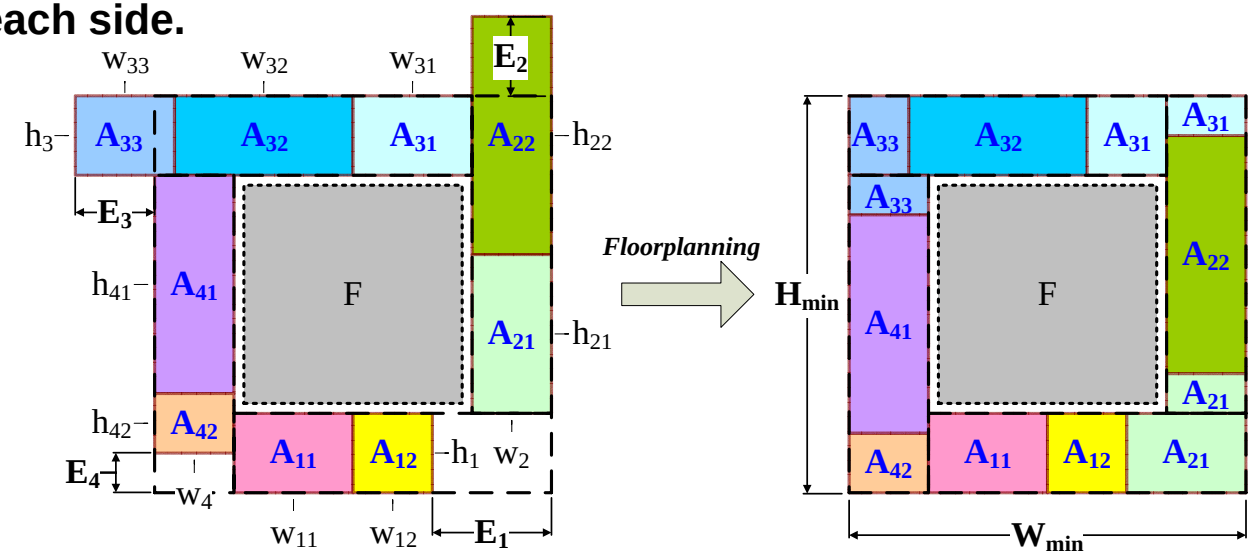
Signal-pin name	I/O buffer type	I/O width (um)	I/O height (um)	Selected signal-pin pattern	Group	Side	Order	Power-pin name	Power-pin NO.
AD_P[0:7]	AIO1XH0J	40	500	1	1	1	1	VDDA	10
AD_N[0:7]	AIO1XH0J	40	500	1	1	1	1	VDDA	10
…	…	…	…	…	…	…	…	…	…
AD[0:15]	BIO1XH0J	30	350	3	2	1	2	VDDB	8
…	…	…	…	…	…	…	…	…	…
TEST_IN[0:6]	CIO1XH0J	25	400	4	3	2	1	VDDC	5
TEST_OUT[0:6]	CIO1XH0J	25	400	4	3	2	1	VDDC	5
TRAP[0:6]	CIO1XH1J	25	400	4	3	2	1	VDDC	5
…	…	…	…	…	…	…	…	…	…



Pin-Block Design and Floorplanning (5/6)

Package size optimization

- E1 to E4 represent the width (height) of the excess or empty area in each side.



$$E \begin{cases} > 0, & \textit{Excess} \\ = 0, & \textit{Exact} \\ < 0, & \textit{Empty} \end{cases}$$

(Side, Order)

A_{11}: (1, 1)	A_{12}: (1, 2)	
A_{21}: (2, 1)	A_{22}: (2, 2)	
A_{31}: (3, 1)	A_{32}: (3, 2)	A_{33}: (3, 3)
A_{41}: (4, 1)	A_{42}: (4, 2)	

Pin-Block Design and Floorplanning (6/6)

- **Problem formulation— to minimize package size**

Minimize

$$f = \sum_{j=1,3}(\sum_i w_{ji} + E_j)h_j + \sum_{j=2,4}(\sum_i h_{ji} + E_j)w_j + F$$

subject to

$$W = w_4 + \sum_i w_{1i} + E_1 = w_2 + \sum_i w_{3i} + E_3 \quad (1)$$

$$H = h_1 + \sum_i h_{2i} + E_2 = h_3 + \sum_i h_{4i} + E_4 \quad (2)$$

$$W = H \quad (3)$$

$$E_1 + E_2 + E_3 + E_4 \geq 0 \quad (4)$$

$$F \geq c \quad (5)$$

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Experimental Results (1/3)

TABLE I

TWO INDUSTRIAL BENCHMARKS USED IN THIS PAPER.

	Signal bus	Pin num	Group	Selected signal-pin pattern	Side	Order	Power-pin number
Case 1	Bus#1	66	1	2	1	1	32
	Bus#2	27	2	3	2	1	8
	Bus#3	37	3	4	2	2	24
	Bus#4	39	4	1	3	1	N/A
	Bus#5	42	5	1	4	1	24
	Bus#6	58	6	4	4	2	24
Case 2	Bus#1	66	1	2	1	1	24
	Bus#2	27	2	3	2	1	8
	Bus#3	95	3	2	2	2	N/A
	Bus#4	100	4	2	3	1	8
	Bus#5	42	5	4	4	1	16
	Bus#6	16	6	4	4	2	7

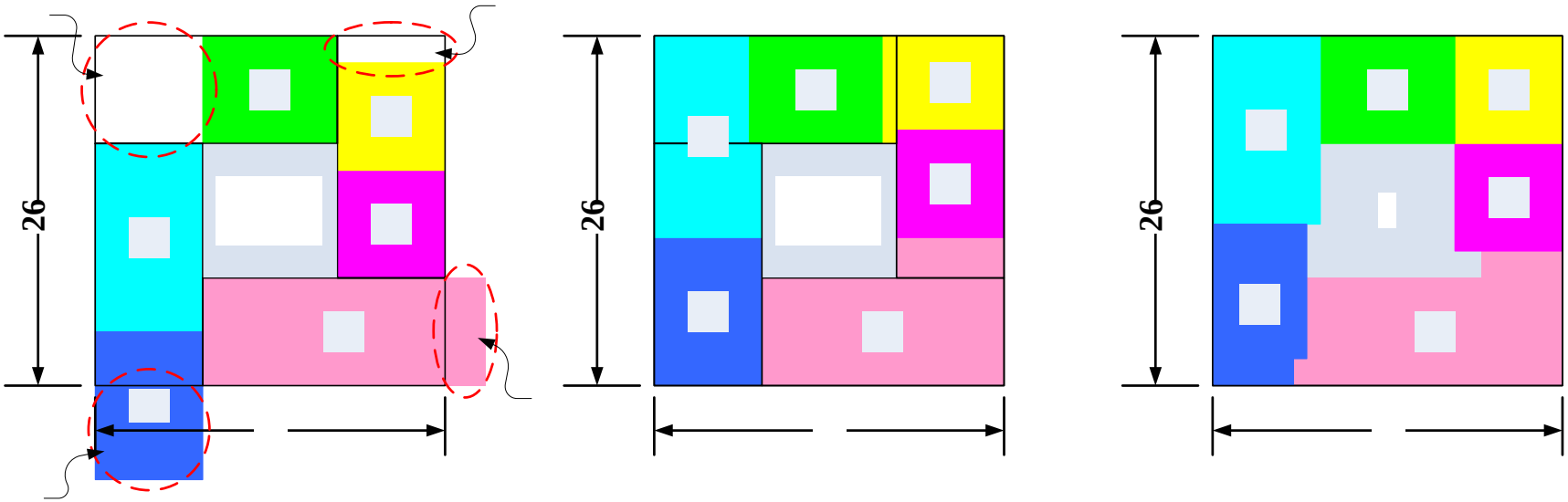
TABLE II

THE EXPERIMENTAL RESULTS OF CASE 1 AND CASE 2.

	E_1	E_2	E_3	E_4	$\sum_i E_i$	Central p/g pins (F=rowxcol)	Eval min package (WxH)
Case 1	-3	2	8	-7	0	10x10	26x26
Case 2	3	-9	-3	12	3	14x14	31x31

Experimental Results (2/3)

- **Case (I):**
  - ✓ **(b) Automated pin-out designation.**
  - ✓ **(c) Manual pin-out designation.**



Experimental Results (3/3)

- **Case (II):**
  - ✓ **(e) Automated pin-out designation.**
  - ✓ **(f) Manual pin-out designation.**

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Conclusion

- We have designed six signal-pin patterns (template) for pin block construction in package design.
- We have proposed a near optimal approach to minimize package size.
- We automate this pin-out designation process for package-board codesign.

Thanks for your attention