# A Technique to Reduce Current and Average Power Dissipation in Scan Designs by Limited Capture

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# Purpose

- Reducing excessive switching activity of deterministic test patterns generated by any ATPG
  - Reduce peak current during capture and shift cycles to safe level
  - Reduce also average power
- Low hardware overhead
- No performance degradation
- No decrease in fault coverage
- Minimizing test sequence length
  - Use highly compacted test patterns

# Outline

- Introduction
- Outline of Proposed Scheme
- Reducing Power during Shift Cycles
- Reducing Power during Capture Cycles
- Procedure to Determine Capture Groups
- Experimental Results
- Conclusions and Future Research

# Introduction

- Significantly higher switching activity during scan testing causes two main problems
  - High power (heat) dissipation -> damages CUT or hurts reliability of chips
    - Elevates CUT temperature during test application
    - Power dissipation during scan shift cycles dominates
  - High Instantaneous current flow capture cycles -> results in unnecessary loss of yield
    - $Vdrop = IR + Ldi/dt$
    - Increases delay and even flips flip-flop states

# Introduction

- Most previous publications focus on reducing power dissipation (scan shift cycles)
- Previous publications that reduce peak current
  - Sequential capture [Rosinger et al. TCAD 04], [Lee et. al. ATS 04], [Saxena et al. ITC 01]
    - Partition scan chains into sub scan-chains and clock only one sub scan-chain in each phase in sequence
    - Capture violation should be resolved
  - Don't care utilization by ATPG [Wen et al. VTS 05]
    - Assigns don't cares existing in test cubes to minimize peak current during capture cycles
    - Needs a separate technique to reduce scan shift power

# Outline of Proposed Scheme

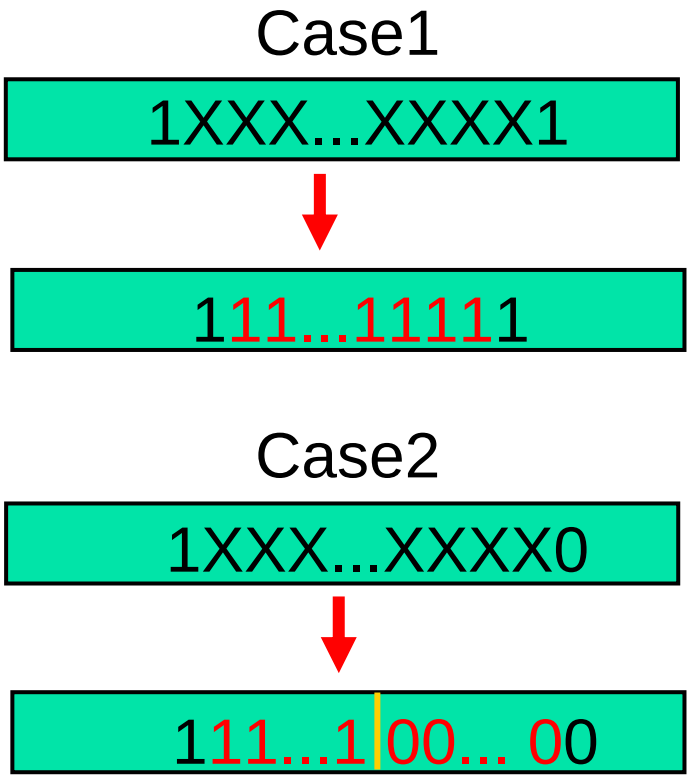
- Reducing switching activity during capture cycles does not reduce switching activity during shift cycles and vice versa
- Different methods used to reduce power during shift cycles and current during capture cycles
  - Shift cycles
    - Utilize don’t cares existing in test patterns
    - Adjacent don’t care bits are assigned same values
  - Capture cycles
    - Capture only selected scan chains
    - Scan chains that are not selected continue shifting

# Outline of Proposed Scheme

- Simply modifies existing test patterns to reduce switching activity without generating test patterns
  - Handle test patterns generated by any ATPG tool
  - No special (dedicated) ATPG tool required
- Minimally intrusive to existing design
  - No need to modify existing scan structure (partitioning into scan sub-chains are not required)
  - No need for special clock trees
  - Multiple scan enable signals and a small register are only addition

# Reducing Power during Shift Cycles

- Don’t care are assigned to reduce power during shift cycles [Wang & Gupta DAC 97]




don’t cares are flanked by the same binary values

fill don’t cares with the same binary value

don’t cares are flanked by opposite binary values

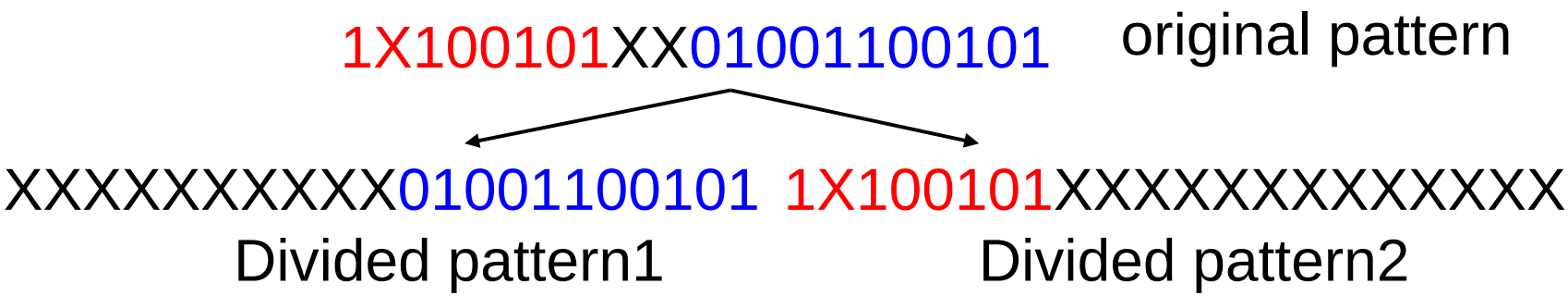
randomly choose 1/0 boundary

# Reducing Power during Shift Cycles

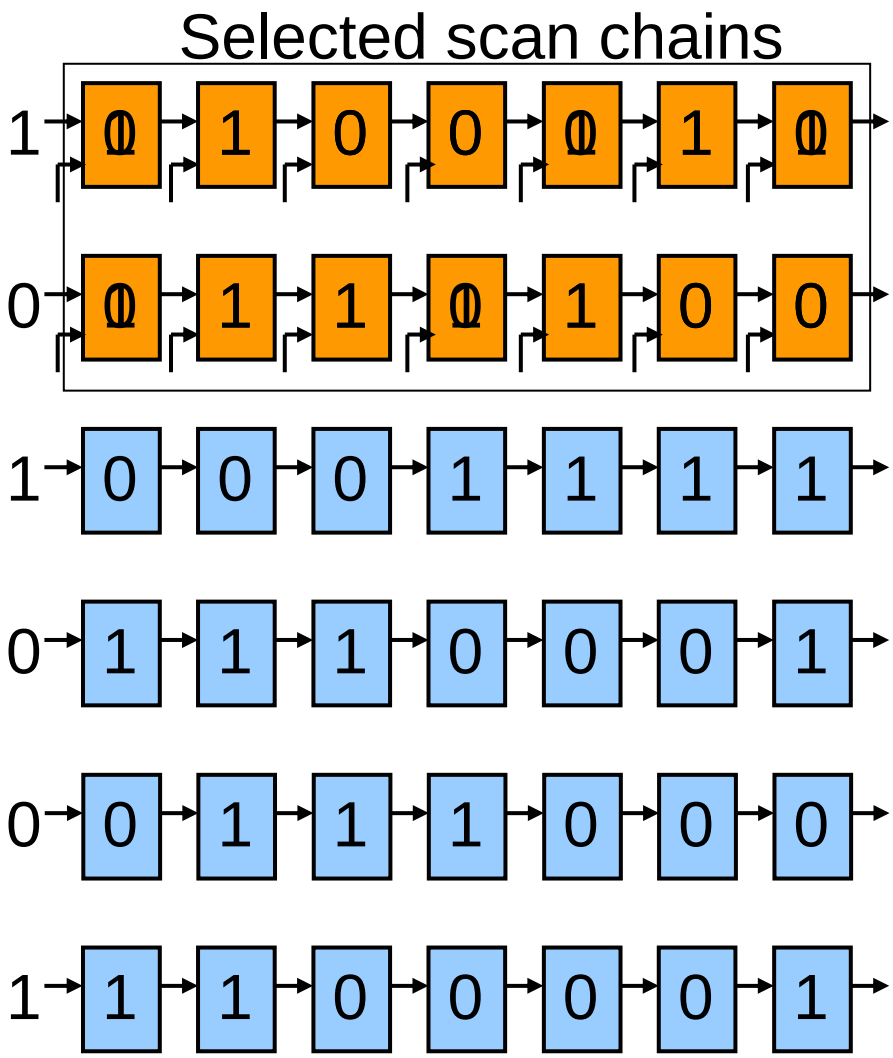
- Need many don't cares (X's) to achieve enough power reduction during shift cycles
  - Overspecified bits are relaxed [Wang et al. ITC 05]
- If highly compacted test set used, some patterns do not have enough don't cares even after relaxations
  - Static compaction merges several compatible test patterns into one test pattern
    - Increase specified bits (decrease X's)
  - Reverse compaction can increase X's at the expense of larger test data volume and longer test application time

# Reducing Power during Shift Cycles

- Reverse compaction
  - Partition a densely specified test pattern into multiple test patterns that have enough don't cares
  - Overlaps between specified bits of new patterns should be minimized
  - Specified bits should be evenly divided into new patterns
  - All faults that are detected by original patterns should be detected by the divided patterns



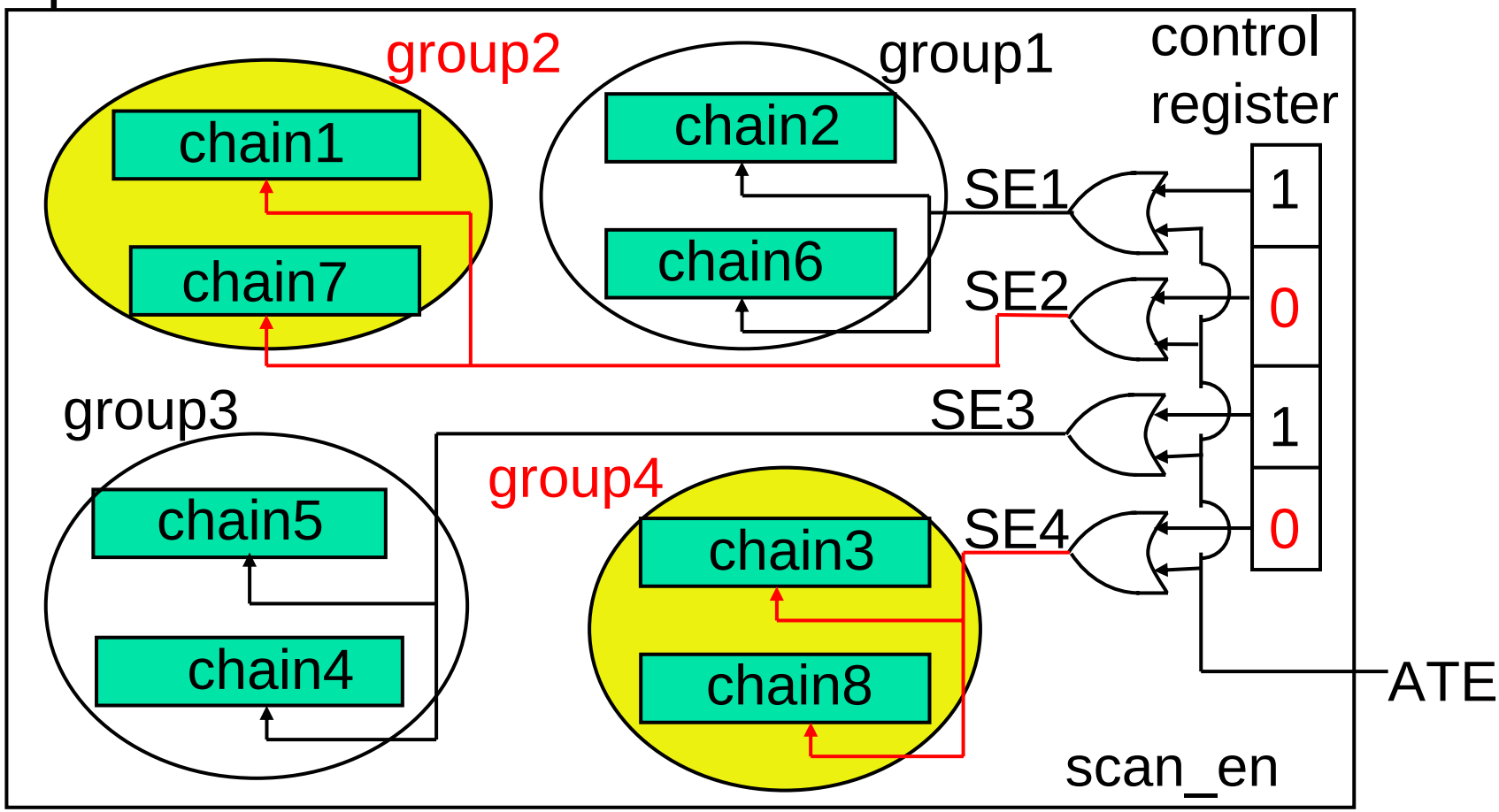
# Reducing Power during Capture Cycles




- In each capture cycle, only selected scan chains capture
  - Other scan chains continue shifting test patterns that are modified to reduce transitions
  - Since only 2 scan chains capture, overall switching activity is reduced
  - Only 2 scan chains shift out responses and other scan chains scan out test patterns that cause fewer transitions

# Reducing Power during Capture Cycles

Proposed scan architecture



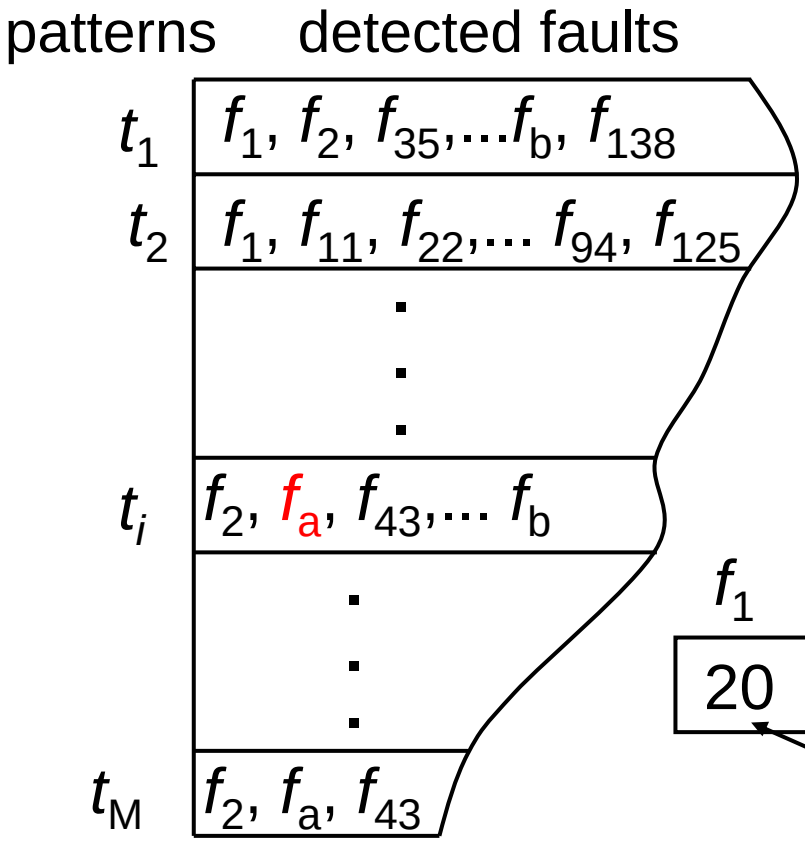

Only group2 and group4 capture responses

# Reducing Power during Capture Cycles

- Determine control register value (groups to capture) for each pattern
  - If there are *G* groups and maximum *C* groups can capture safely, *C* bits in the control register are set to 0
  - There are $\binom{G}{C}$ different combinations to choose
- Since only $C < G$ groups capture responses
  - Fault coverage may decrease
  - But, carefully selecting *C* capture groups can minimize or eliminate decrease in fault coverage

# Procedure to Determine Capture Groups

- Computed detection counts (# of patterns that detect each fault by *n*-detection fault simulation




single detection faults

if $f_a$ is single detection fault of pattern $t_i$, then scan chains that capture $f_a$ should be selected (included in capture group for $t_i$) in $C$

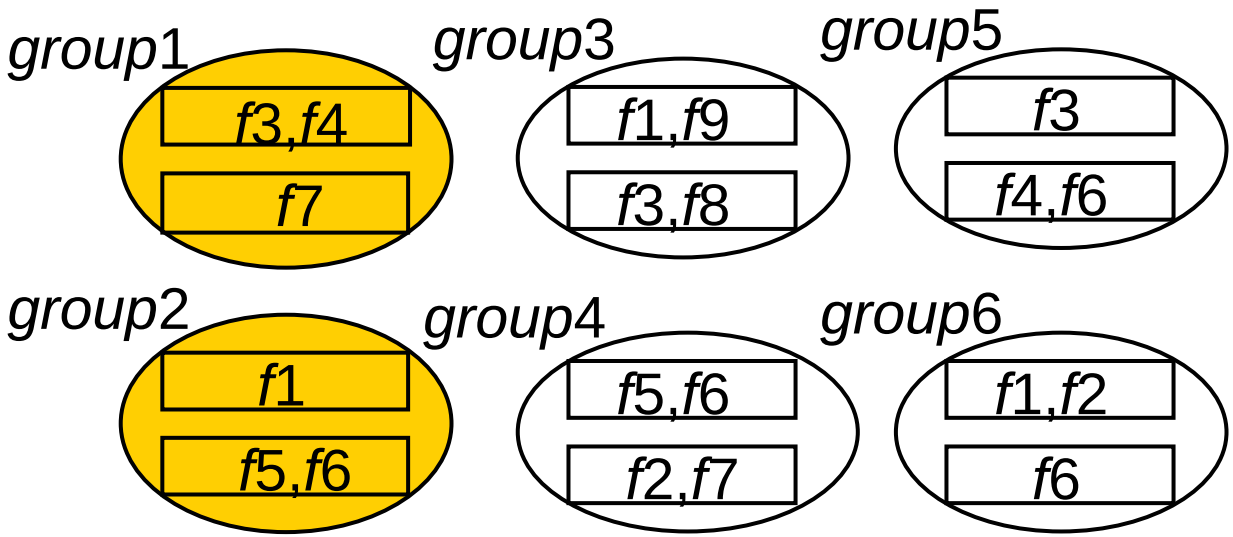
detection count table

| $f_1$ | $f_2$ | ... | $f_a$ | ... | $f_b$ | ... | $f_N$ |
|---|---|---|---|---|---|---|---|
| 20 | 15 | ... | 1 | ... | 2 | ... | 1 |

many other patterns detect

# Procedure to Determine Capture Groups

- Tries to find *C*(=2) capture groups that detect all single detection faults of the test pattern
  - None-single detection faults can be detected by other patterns



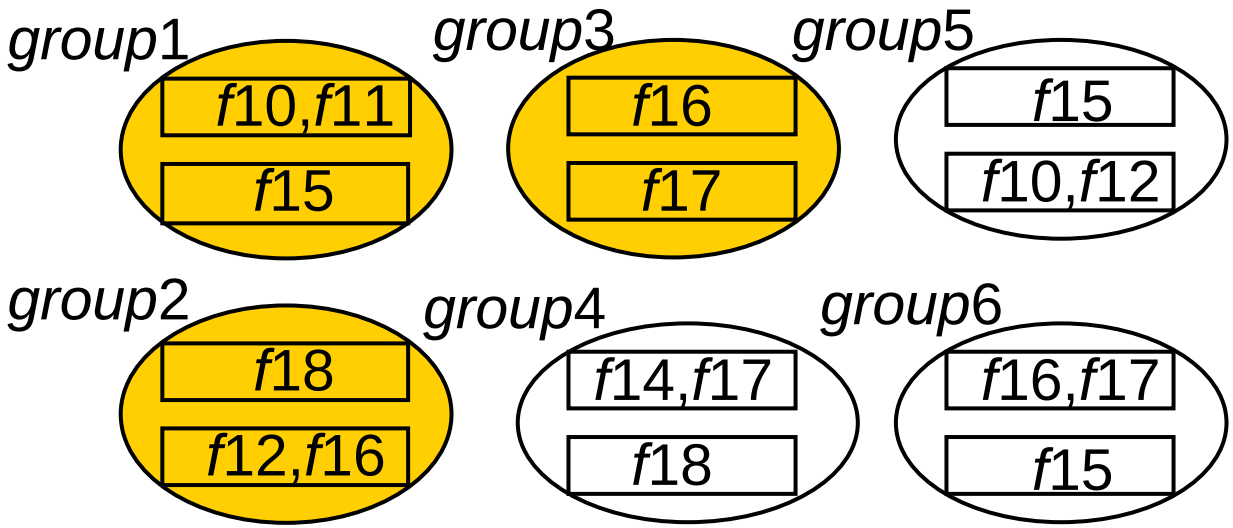

Capturing group1 & group2 can detect all single detection faults of pattern *ta*

*Fa*={*f*1, *f*2, *f*3, *f*4, *f*5, *f*6, *f*7, *f*8, *f*9}

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $dc_j$ | 1 | 3 | 1 | 2 | 1 | 2 | 1 | 7 | 3 |

# Procedure to Determine Capture Groups

- Detecting all single detection faults by capturing *C* groups is not possible for some test patterns
  - Select more than *C* groups to detect all single detection faults if it does not exceeds peak current limit




No *C* groups can detect all single detection faults, but detecting one more can do

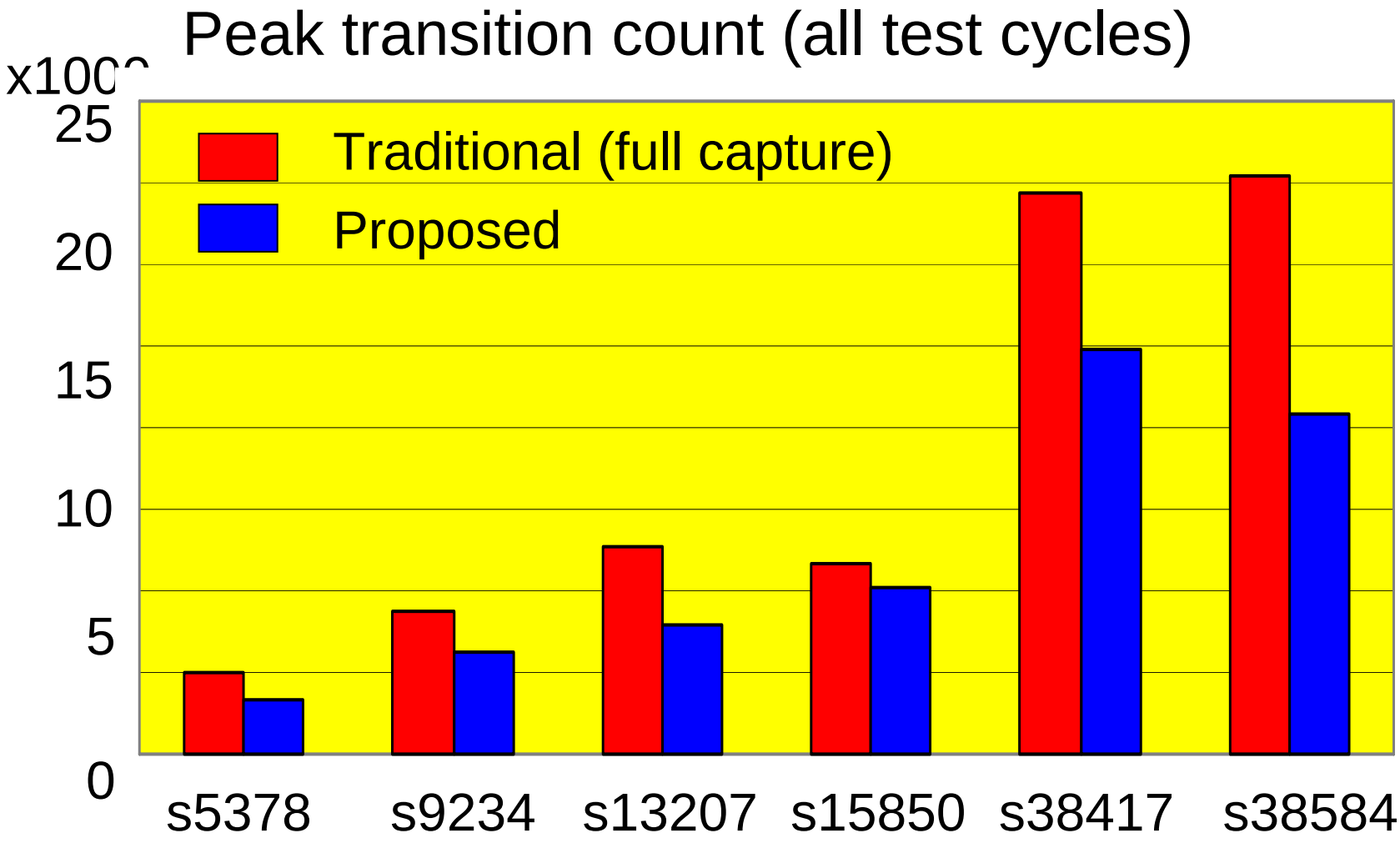
*Fa*={*f*10, *f*11, *f*12, *f*13, *f*14, *f*15, *f*16, *f*17, *f*18}

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $dc_j$ | 1 | | 3 | | 1 | 2 | 1 | 7 | 3 |

# Procedure to Determine Capture Groups

- If capturing more than *C* groups exceeds peak limit
  - Select 2*C* groups
  - Apply the same pattern twice and capture different *C* groups in each application
- If selecting 2*C* groups still cannot detect all single detection faults
  - Select more than 2*C* groups to detect all single detection faults and see if it exceeds current limit
  - If it exceeds peak current, select 3*C* groups
  - Apply the pattern 3 times capturing different *C* groups in each application

# Experimental Results



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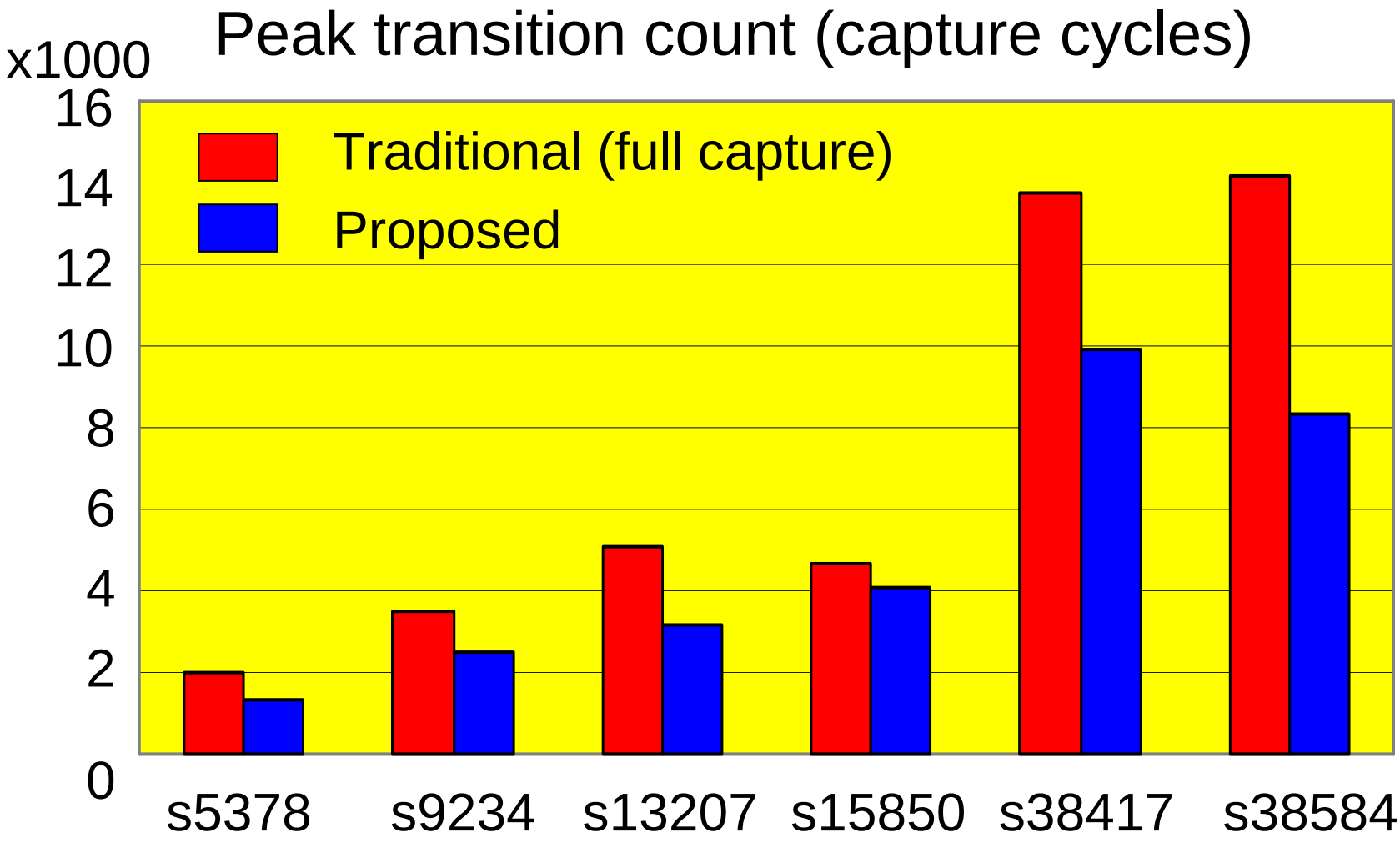

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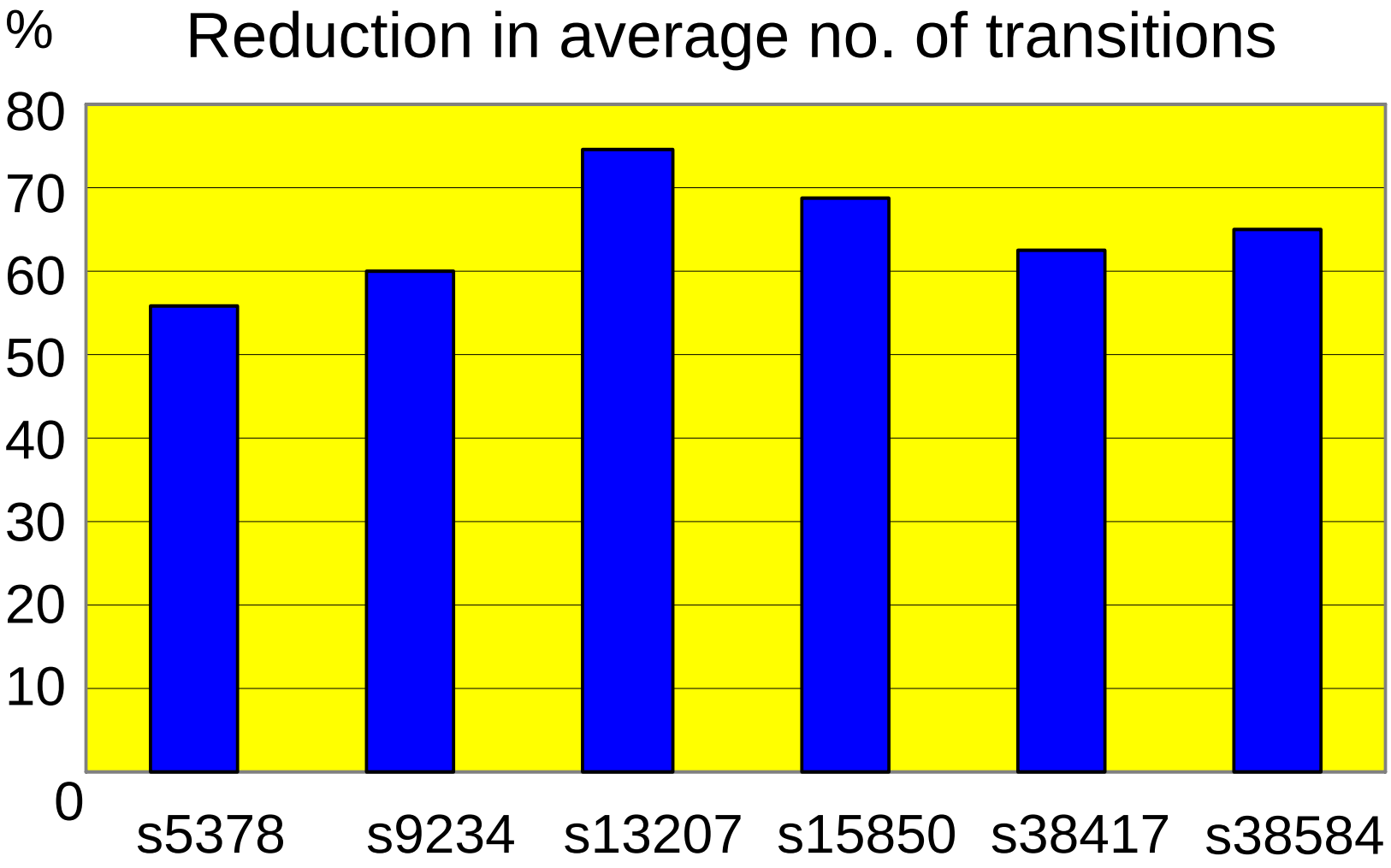
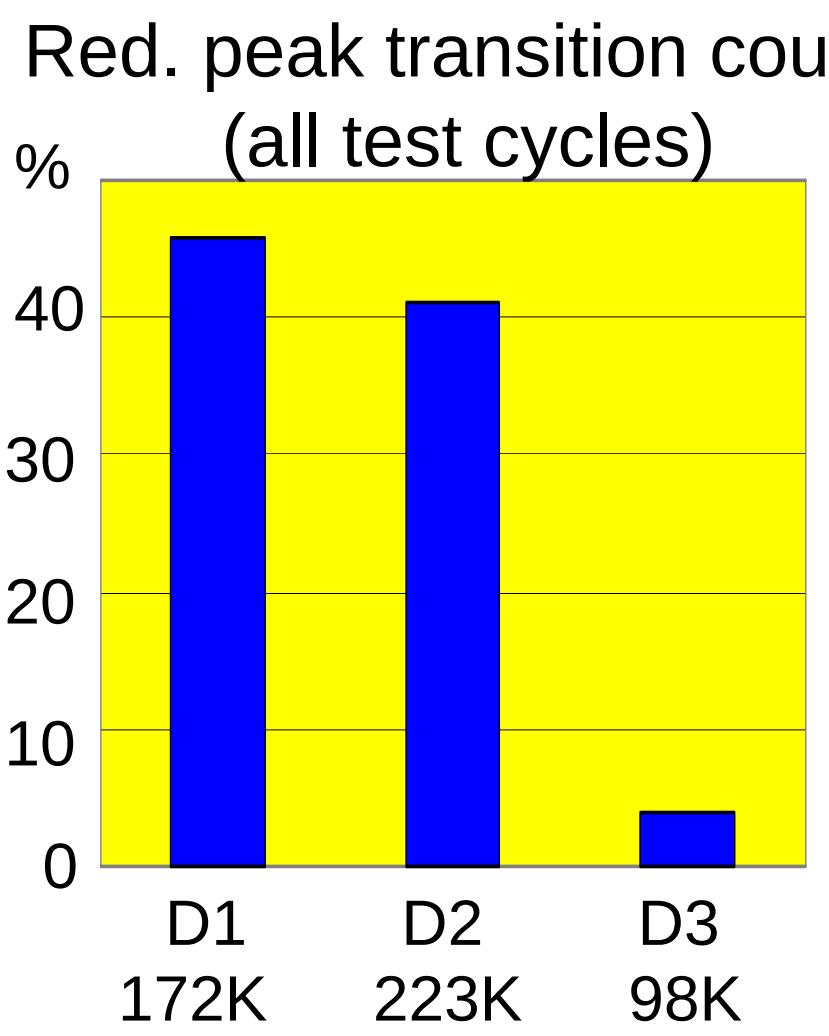
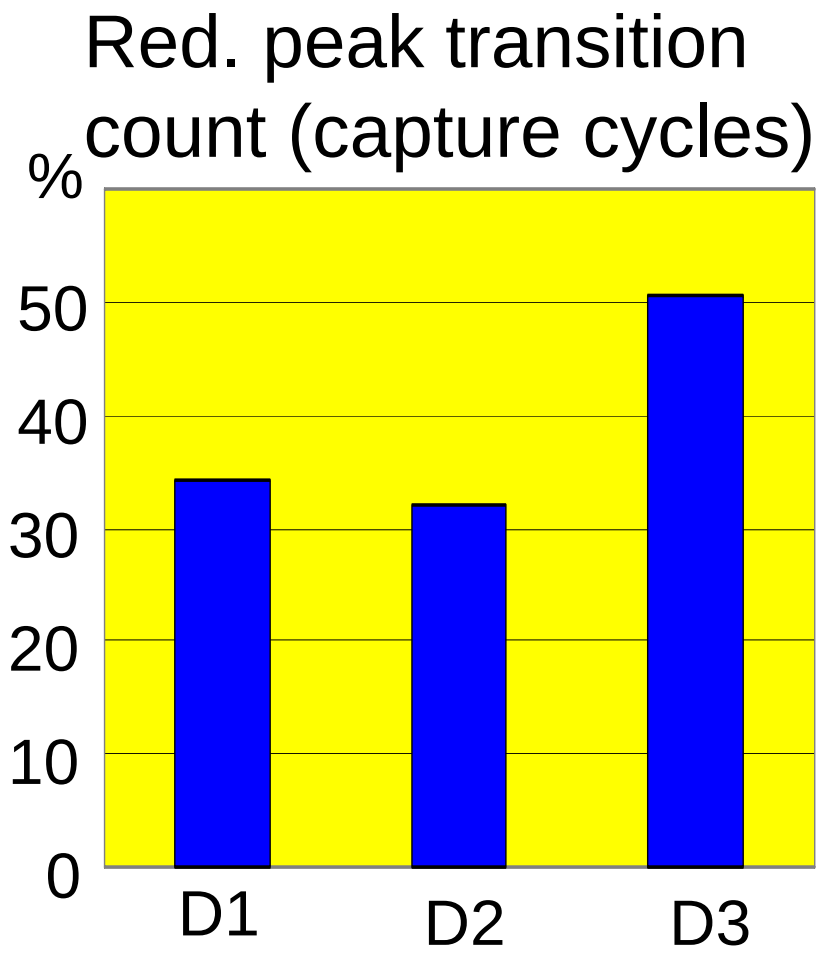
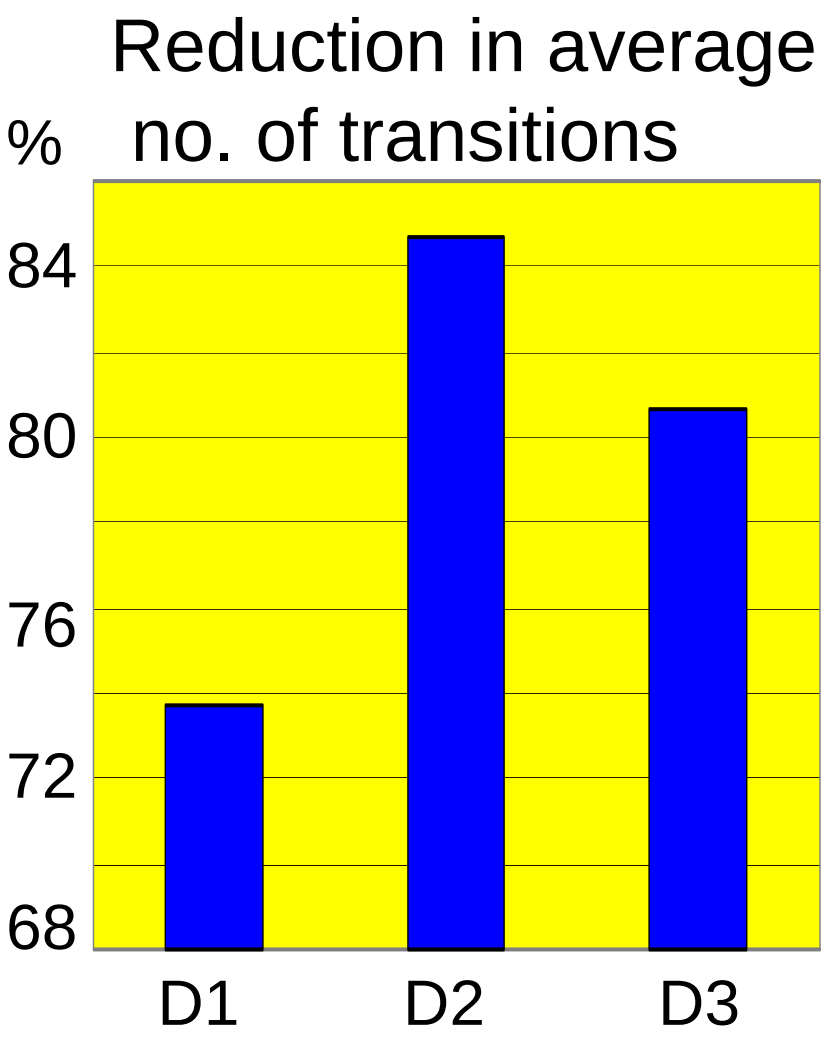


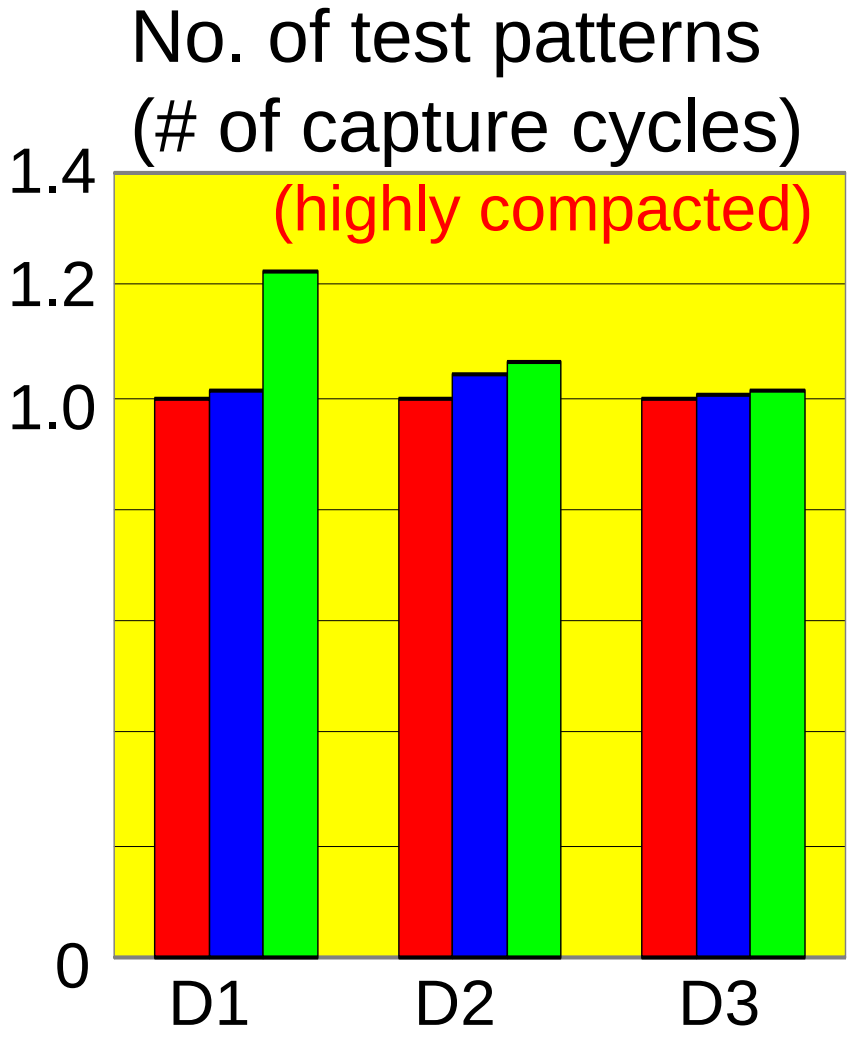
# Experimental Results (Industrial Designs)



# Experimental Results (Industrial Designs)



# Conclusions and Future Research

- Significantly reduces power dissipation and peak current
  - Peak current during capture cycles reduce by average 30% for ISCAS, even larger for industrial designs
  - 36-46% reduction in peak current during entire test cycles
  - 56-85% reduction in average number of transitions
- No decrease in fault coverage
- The proposed technique modifies test patterns generated by any ATPG
  - Flexibility
- No capture violation

# Conclusions and Future Research

- Low hardware overhead
  - One small register
- Minimally intrusive
  - Need not change clock tree or scan chain architecture
- Extension to delay testing (Future work)
  - Scan delay test session is divided into several sub-session in which only one clock domain is tested
  - Scan chains that belong to other clock domains need not capture responses
    - The proposed method naturally fits to this environment!