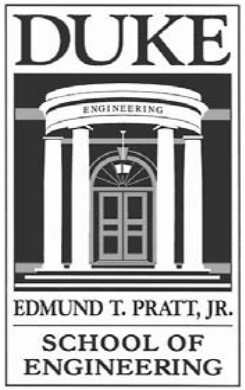
A Wafer-Level Defect Screening Technique to Reduce Test and Packaging Costs for "Big-D/Small-A" Mixed-Signal SoCs

Sudarshan Bahukudumbi, Sule Ozev, Krishnendu Chakrabarty, Vikram Iyengar§

Department of Electrical and Computer Engineering, Duke University

§IBM Microelectronics, Essex Junction, VT

Duke University



Outline

- Introduction
- Motivation: Wafer-level, mixed-signal defect screening
  - Challenges
- Wafer-level defect screening
  - Correlation based signature analysis techniques
- Cost Model
  - Cost components
  - Analysis framework
  - Results
- Experimental Results
- Conclusions

“Big-D Small-A” SoC

Introduction

- Increasing popularity due to importance in consumer electronics market

- Fraction of die area comprising of analog/mixed-signal ~10%

- Typical “Big-D Small-A” SoC components:
  - Pair of complementary data converters
  - Large portion of digital logic
  - Phased Locked Loop (PLL)

"Big-D Small-A" SoC

Example

• Typical *"Big-D small-A"* mixed-signal SoC[*]: DragonBall*TM*-MX1 (ARM-core-based Motorola IC)

• Fraction of die area comprising of analog/mixed-signal: 10%

- 7% Sigma-Delta data converters and 3% PLL

[*] G. Bao, "Challenges in Low Cost Test Approach for ARM9™ Core Based Mixed-Signal SoC DragonBall™-MX1", Proc. Of the Intl. Test Conference, 2003

Motivation: Wafer-Level Defect Screening

- Packaging: significant contributor to product cost
- Wafer-level testing ⇒ early defect screening
  - Results in lower packaging cost
- Packaging cost proportional to number of pins in the die
- Current packaging cost per pin exceed the cost of silicon per sq-mm [*]
- Increasing packaging cost highlight the need to reduce the cost by effective screening at wafer level

---

[*] **A. B. Kahng, "The Road Ahead: The Significance of Packaging", IEEE Design & Test, Nov. 2002**

Motivation: Wafer-Level Defect Screening

- Packaging: significant contributor to product cost
- Wafer-level testing ⇒ early defect screening
  - Results in lower packaging cost

- Packaging cost proportional number of pins in the die

- Current packaging cost per pin exceed the cost of silicon per sq-mm [*]

- ITRS 2005: Current Packaging Cost 0.26 – 2.34 ¢/pin
- Maximum pin/die : 140-990

[*] **A. B. Kahng, "The Road Ahead: The Significance of Packaging", IEEE Design & Test, Nov. 2002**

Motivation: Wafer-Level Defect Screening

- Packaging: significant contributor to product cost
- Wafer-level testing ⇒ early defect screening
  - Results in lower packaging cost
- Packaging cost proportional to number of pins in the die
- Current packaging cost per pin exceed the cost of silicon per sq-mm [*]
- Increasing packaging cost highlight the need to reduce the cost by effective screening at wafer level

---

[*] **A. B. Kahng, "The Road Ahead: The Significance of Packaging", IEEE Design & Test, Nov. 2002**

Challenges: Wafer-Level Mixed-Signal Test

Challenges

- Measurement inaccuracies: analog cores tested in a DSP based mixed-signal test environment

- The problem is further aggravated:
  - Noisy DC power supply lines
  - Improper grounding of the wafer probe
  - Improper noise shielding of the wafer probe station

- Test and characterization extremely difficult

- Leads to high yield loss (undesirable)

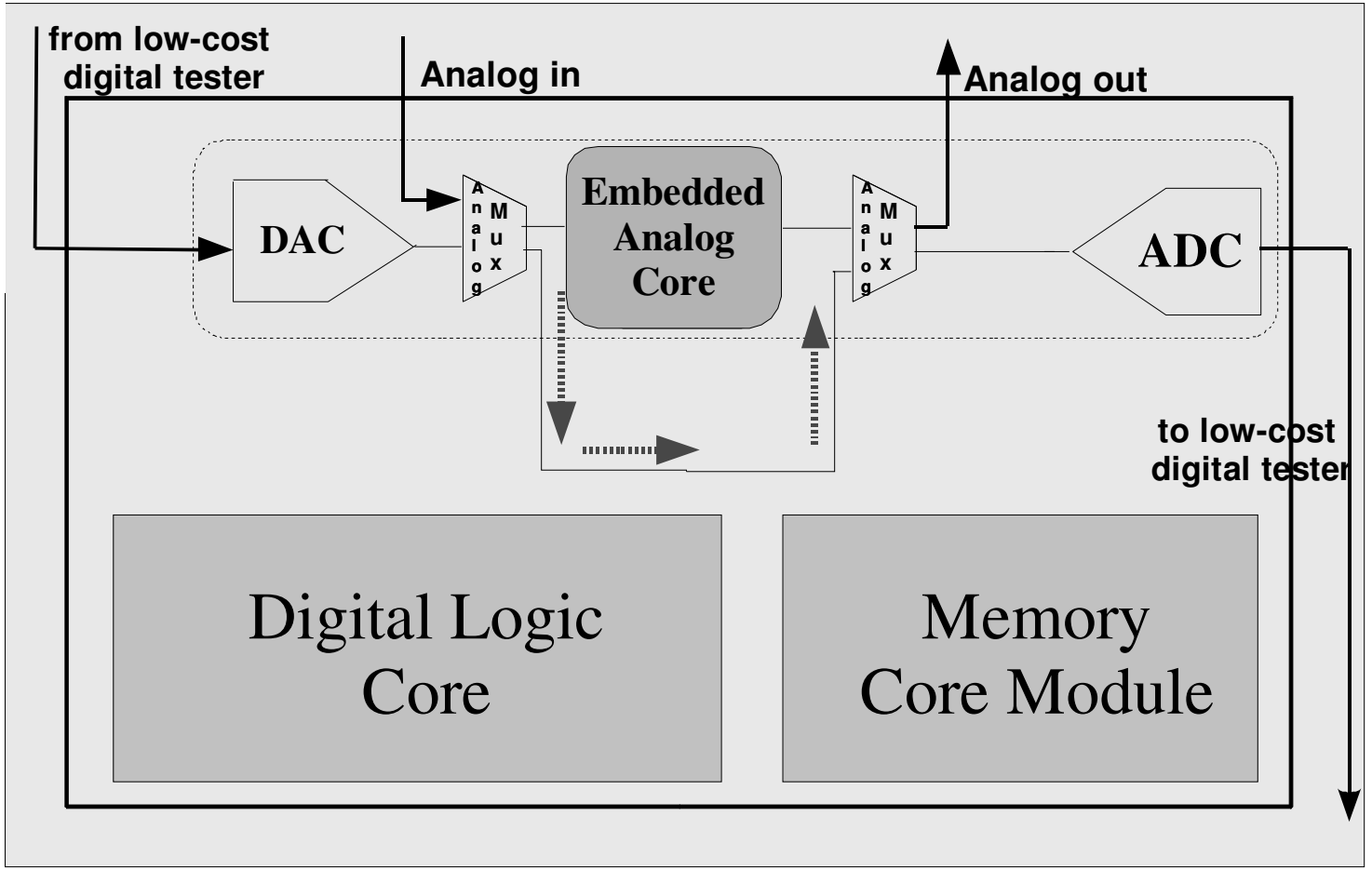
Challenges: Wafer-Level Mixed-Signal Test

Wafer-level defect screening- mixed-signal

- Test methods for analog circuits using low cost digital testers exist
  - Explicit measurements of static and dynamic parameters
  - Wafer-level test environment: yield loss due to inaccurate measurements
  - Use of a mixed-signal ATE: nullify the cost savings due to packaging

- Need for a robust defect screening technique using digital testers for mixed-signal SoCs at the wafer-level

Mixed-Signal Test Data Path



• Digitally compliant mixed-signal test data path in an example SoC

Signature Analysis Based Defect Screening

Signature Analysis

Output response of the circuit compared with a *"pre-determined"* acceptable signature: make a pass/fail decision

Signature Analysis Based Defect Screening

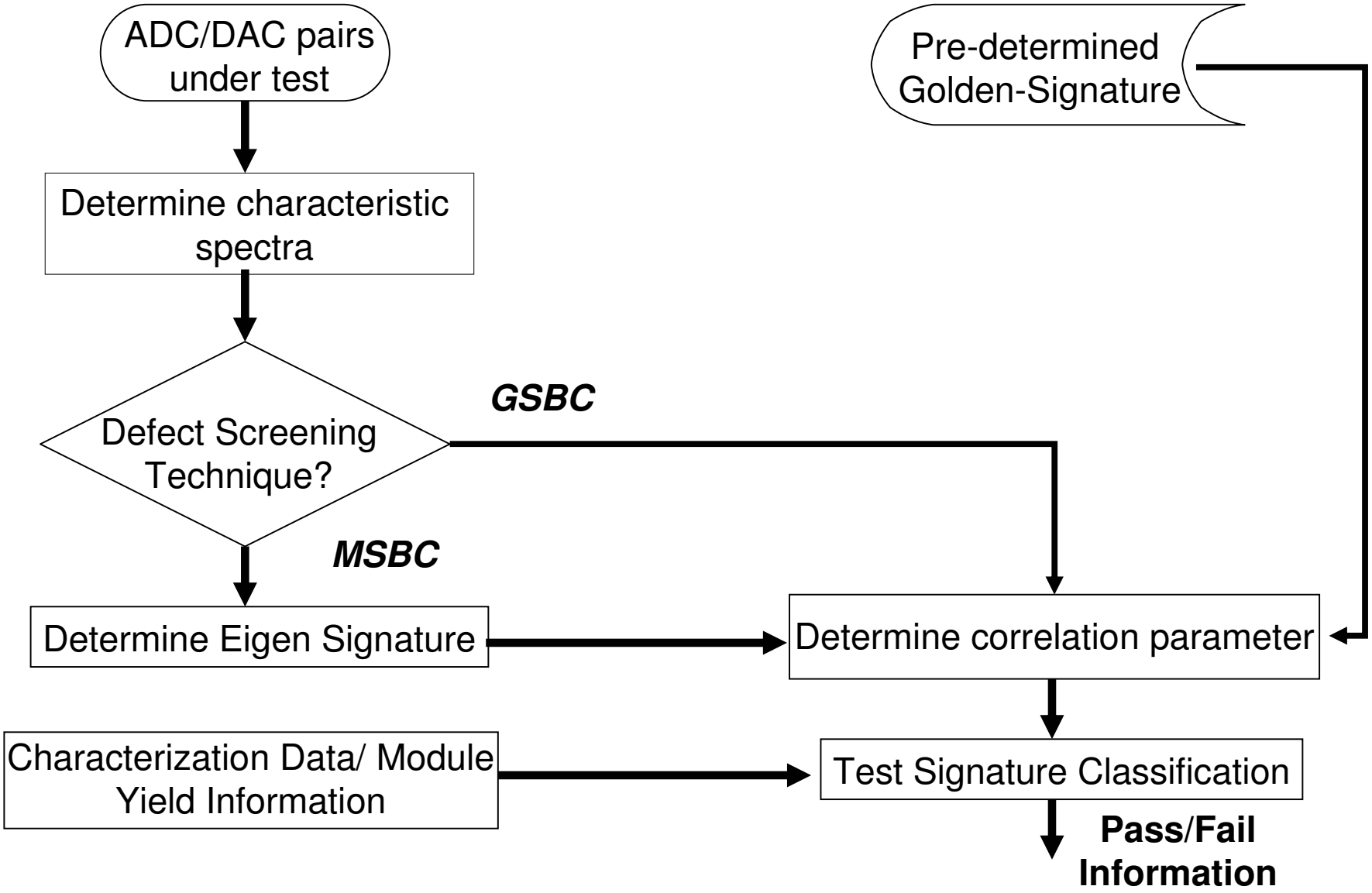
- Acceptable signature: *hard to derive at wafer-sort*

- Defect screening based on outlier analysis
  - Extensively used for testing digital circuits based on IDDQ tests
  - Signature in the form of supply current information

- Spectral based testing
  - Signature spread over multiple data points constituting the spectrum

- Signature analysis technique necessary to encode this information into a single parameter for each core

Signature Analysis



Method 1: Mean Signature Based Correlation (MSBC)

MSBC

Sensitivities to the change in shape of the spectrum from the Eigen Signature determined using correlation parameter

- Eigen signature: *not pre-determined*

1 Spectrum: Acquisition

The characteristic spectrum (X_i) of the i^{th} core (in a batch of m cores) under test → obtained using a P-point FFT and represented as:

$$X_i = \{x_{i1}, x_{i2}, \ldots, x_{iP}\}, \qquad \forall i, 1 \le i \le m$$

2 Determine: Eigen Signature

Eigen Signature E → set of averages of the spectra of m identical cores:

$$E = \left\{ \frac{\sum_{i=1}^{m} x_{i1}}{m}, \frac{\sum_{i=1}^{m} x_{i2}}{m}, \ldots, \frac{\sum x_{iP}}{m} \right\}$$

3 Correlation

Correlation between the Eigen spectrum (E) and the spectrum of the core under test (X_i) can be defined as:

$$\mathrm{corr}(X_i, E) = \frac{\sum_{j=1}^{P} (x_{ij} - \overline{X}_i)\left(\frac{\sum_{i=1}^{m} x_{ij}}{m} - \overline{E}\right)}{\left[\sum_{j=1}^{P} (x_{ij} - \overline{X}_i)^2 \sum_{j=1}^{P} \left(\frac{\sum_{i=1}^{m} x_{ij}}{m} - \overline{E}\right)^2\right]^{1/2}}$$

4 Decision (Pass/Fail)

- Characterization data → Information on expected yield ($Y_{\%}$)
- Modular Testing → Statistical binning → information on expected yield per module
- Information used to make a pass/fail decision on the batch of m dies

Method 2: Golden Signature Based Correlation (GSBC)

GSBC

Sensitivities to change in shape of the spectrum from the Eigen Signature determined using correlation parameter

- Eigen signature: *pre-determined*

Test Flow: GSBC

1 **Determine: Eigen Signature**

- A *golden-signature* spectrum is obtained *a priori*, by assuming ideal and fault-free operating conditions for the circuit under test.
- Pre-determined *golden signature* used as Eigen signature

2 **Spectrum: Acquisition**

The characteristic spectrum (X_i) of the i^{th} core (in a batch of m cores) under test → obtained using a P-point FFT and represented as:

$X_i = \{x_{i1}, x_{i2}, \ldots, x_{iP}\}, \quad \forall i, 1 \le i \le m$

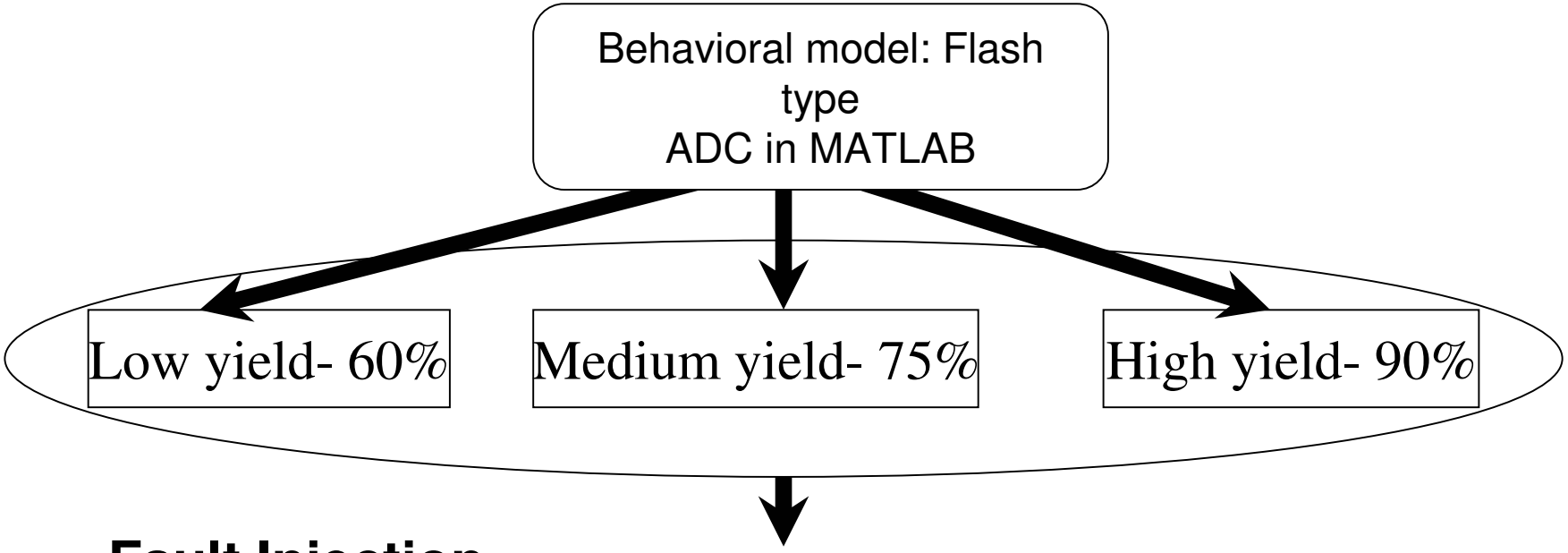
3 **Correlation**

Correlation parameter between the Eigen spectrum (E) and the spectrum of the core under test (X_i) obtained

4 **Decision (Pass/Fail)**

- Characterization data: Information on expected yield ($Y_{\%}$)
- Modular Testing & Statistical binning ⇒ information on expected yield per module
- Information used to make a pass/fail decision on the batch of *m* dies

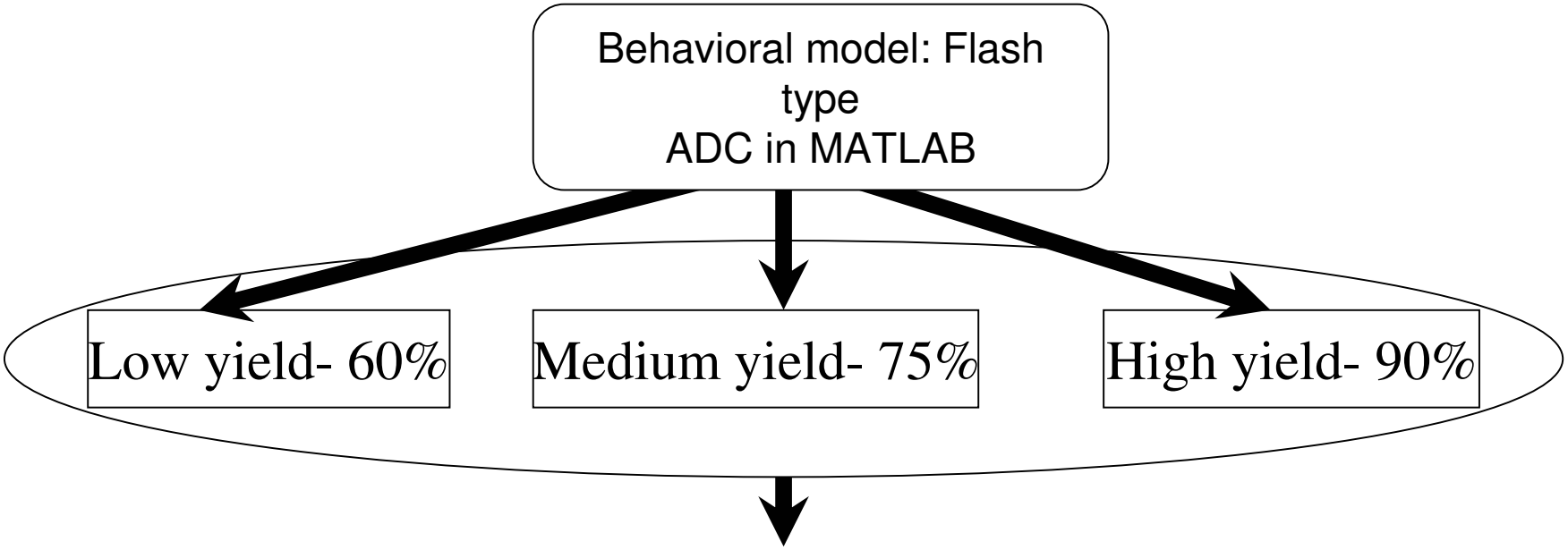
Experimental Environment



Fault Injection

- Failure Type: Hard and Soft failures
- Hard failures: modeled randomly as resistive opens and broken lines in the comparator n/w
- Soft failures: modeled by varying the standard deviation of resistor values and offset voltages: randomly inject soft faults

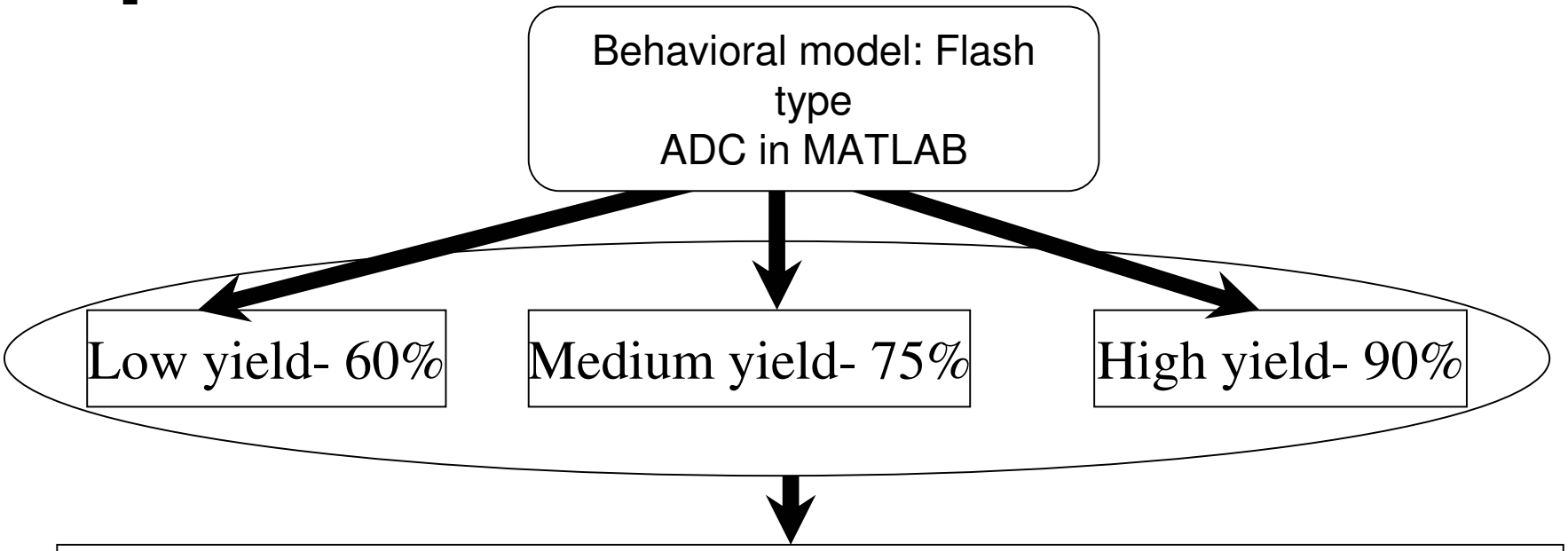
Experimental Environment



Test: *a*

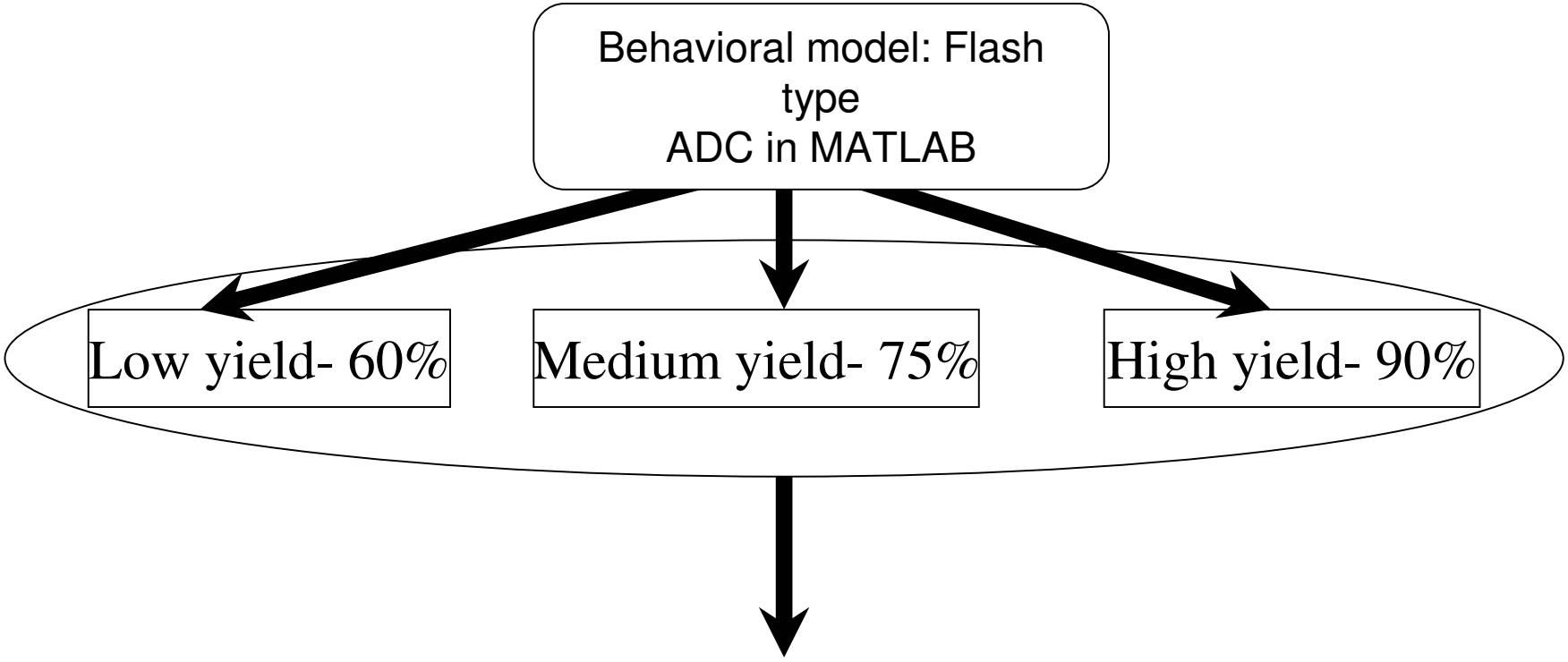
- Determine: correlation parameter for each unique data converter
  - 1024 and 4096 point FFT
- Determine the number of circuits that pass the test
- Determine the number of circuits that fail the test

Experimental Environment



- Independently determine DNL
- Bin data converters as
  - Fault-free: $0 \le DNL \le 0.5$
  - Marginally faulty: $0.5 \le DNL \le 1$
  - Moderately faulty: $1 \le DNL \le 2$
  - Grossly faulty: $DNL > 2$
- Determine the number of faulty circuits that pass the test: F_{pass}
- Determine the number of good circuits that fail the test: G_{fail}

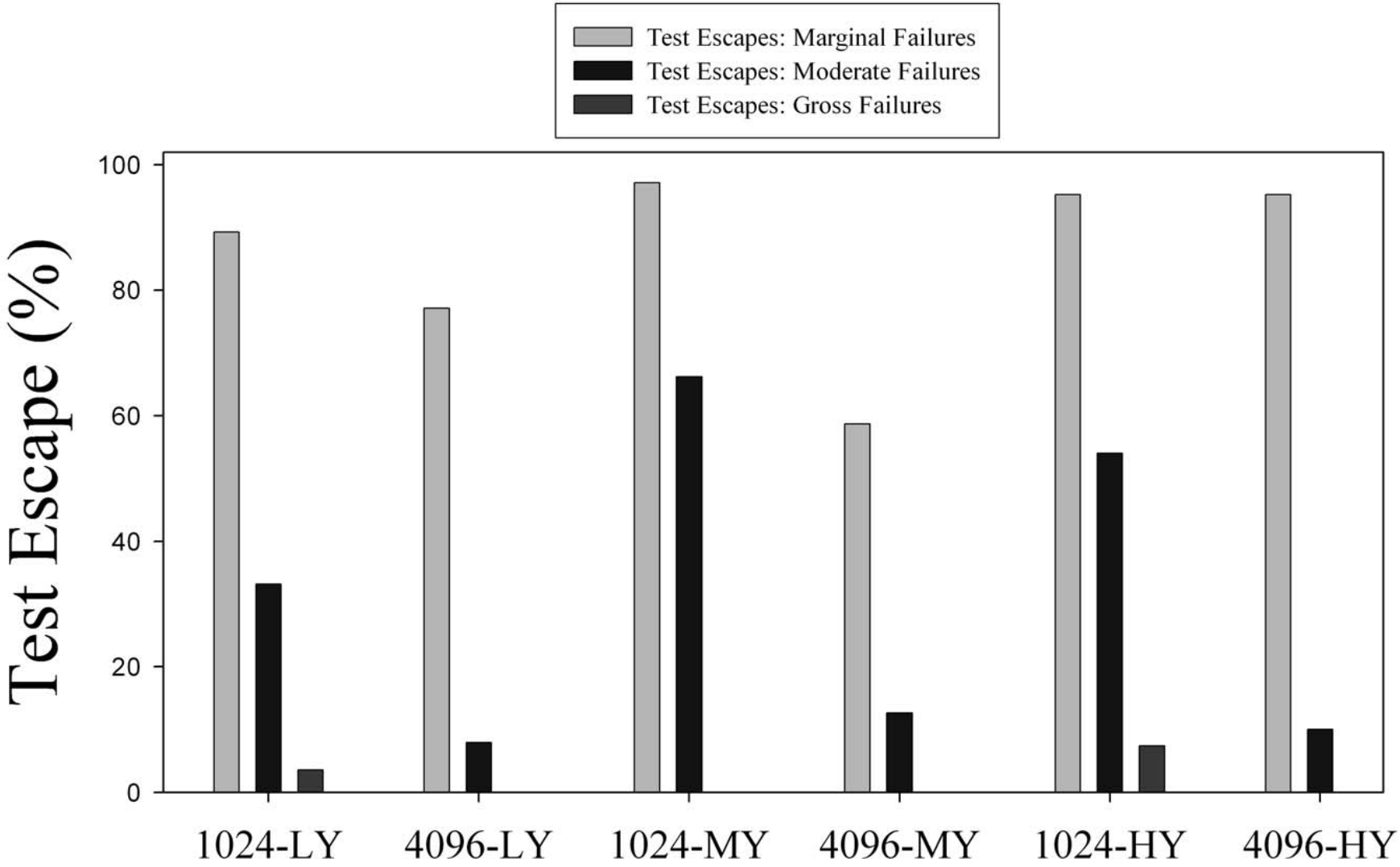
Experimental Environment



- Determine yield loss = G_{fail}/G, where G is number of good circuits
- Determine test escape = $F_{pass}/(N\text{-}G)$, where N is total number of circuits

Experimental Results: MSBC

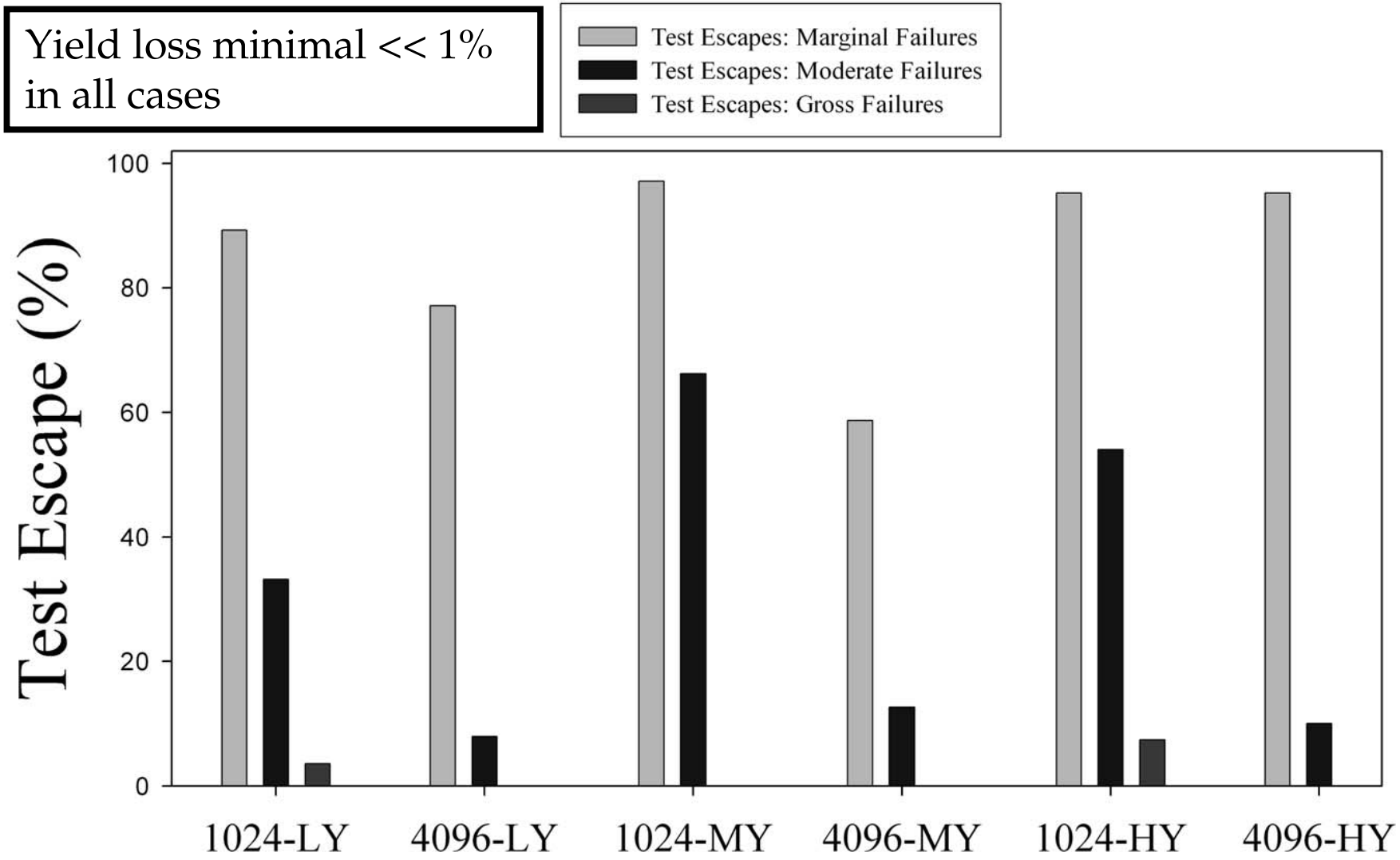
- Gross Failures: Negligible/zero test escape rate
- Implies most gross failures easily detected



Experimental Results: MSBC

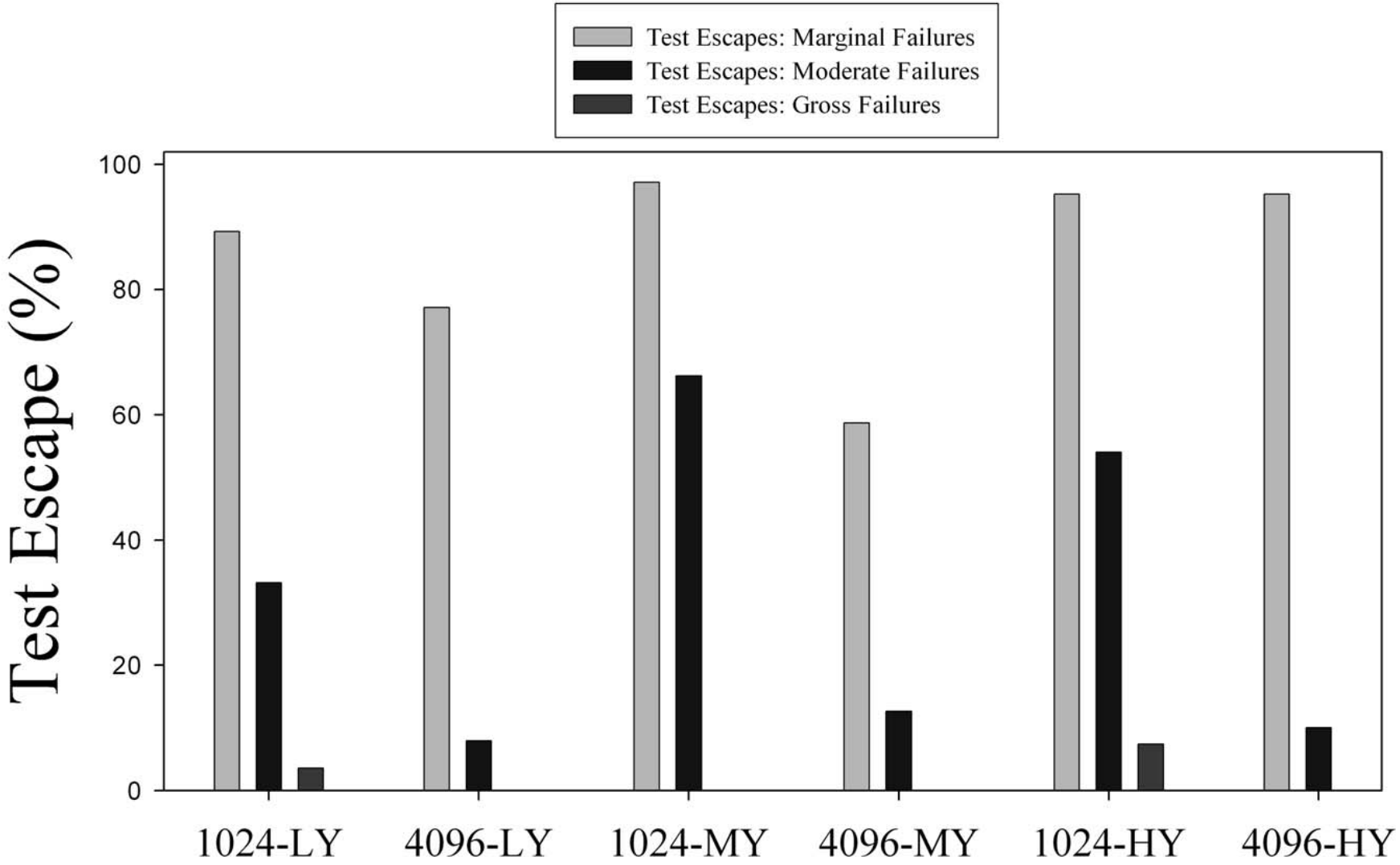
- Significant percentage of marginal failures result in test escapes
- 33-92% of the moderate fails are detected

Yield loss minimal << 1% in all cases



Experimental Results: GSBC

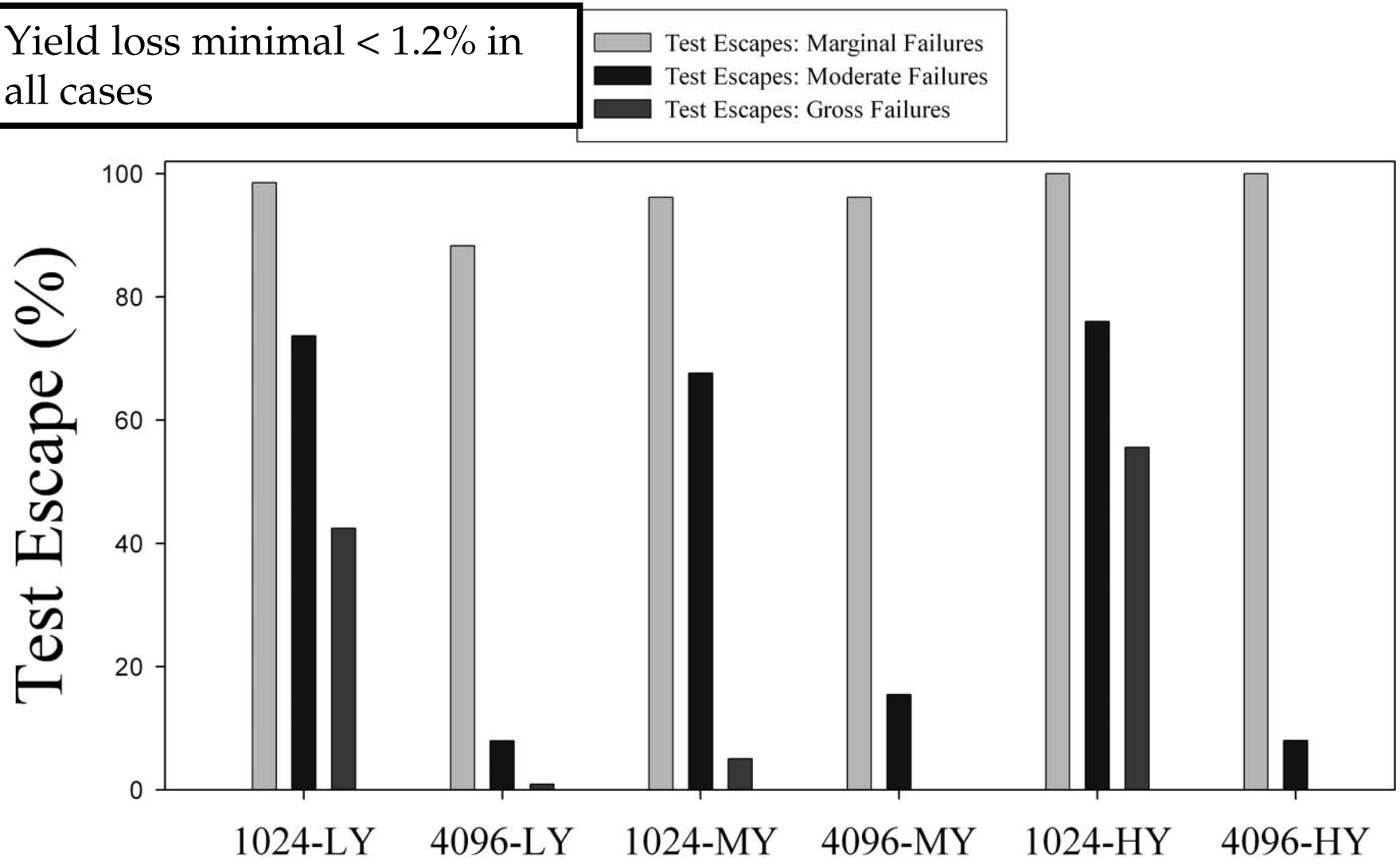
- Gross Failures: Negligible/zero test escape rate
- Implies most gross failures easily detected



Experimental Results: GSBC

- Significant percentage of marginal failures result in test escapes
- 26-92% of the moderate fails are detected

Yield loss minimal < 1.2% in all cases



Cost Model

Cost Model: Purpose

- Evaluate effectiveness of wafer-level testing
- Quantify impact on cost

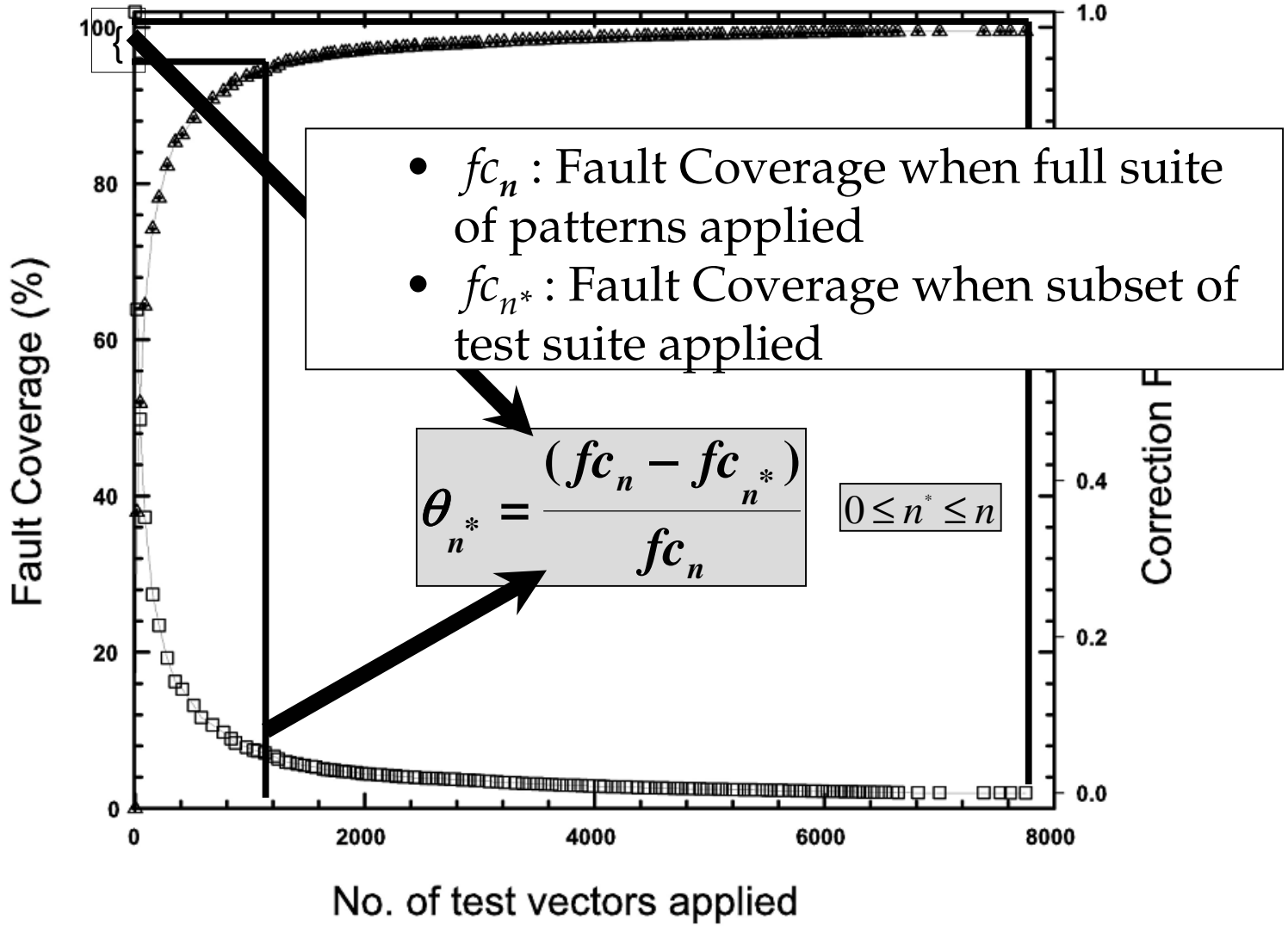
Cost Model

Correction Factors

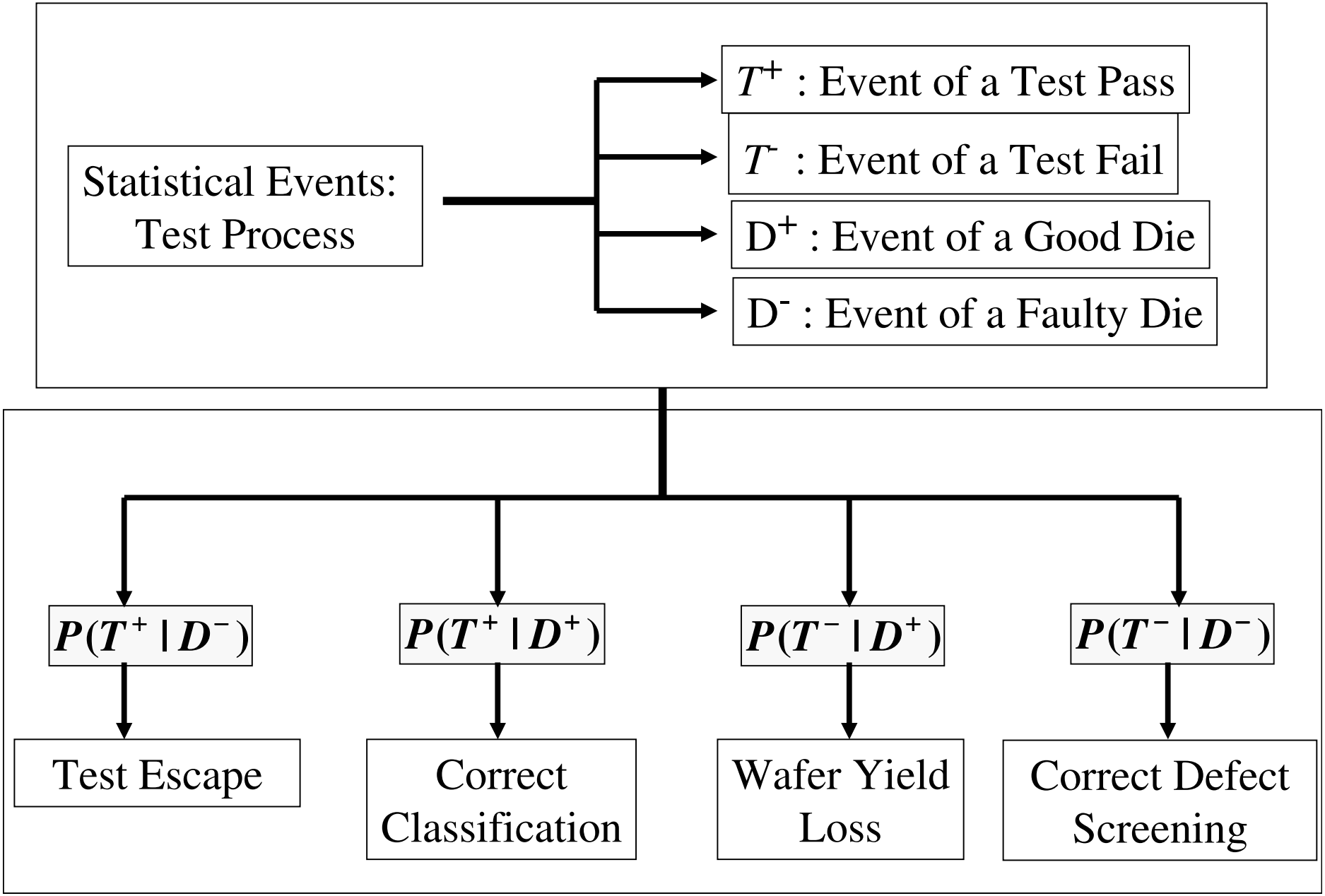
- Test Escape
  - At wafer level impacts packaging cost
  - Test Escape (analog cores): β
  - Test Escape (digital cores): θ_{n^*}
  - SoC Test Escape: $\mathbf{1-(1-\theta_{n^*})\cdot(1-\beta)}$

- Yield Loss is undesirable $\Rightarrow$ Increased cost
- Wafer Yield Loss (analog cores): WYL_a
- Wafer Yield Loss (digital cores): WYL_d
- SoC Test Escape: $\mathbf{1-(1-WYL_d).(1-WYL_a)}$

Cost Model


100
80
60
40
20
0
0
2000
4000
6000
8000
1.0
0.4
0.2
0.0
Fault Coverage (%)
No. of test vectors applied
Correction F
• fc_n : Fault Coverage when full suite of patterns applied
• fc_{n^*} : Fault Coverage when subset of test suite applied
$\theta_{n^*} = \frac{(fc_n - fc_{n^*})}{fc_n}$
$0 \le n^* \le n$

Cost Model


Statistical Events:
Test Process
T^+ : Event of a Test Pass
T^- : Event of a Test Fail
D^+ : Event of a Good Die
D^- : Event of a Faulty Die
$P(T^+ \mid D^-)$
$P(T^+ \mid D^+)$
$P(T^- \mid D^+)$
$P(T^- \mid D^-)$
Test Escape
Correct Classification
Wafer Yield Loss
Correct Defect Screening

Cost Components

$C_{oc_{wap}}$ → Cost :Wafer-Level + Assembled Package Test

$C_{oc_{ap}}$ → Cost : Assembled Package Test

$$C_{oc_{ap}} = (N \cdot t_{ap} \cdot c_{ap}) + N \cdot P + (N \cdot A_{die} \cdot C_{sil})$$

Test Cost

Packaging Cost

Cost of Silicon

$$C_{oc_{wap}} = (N \cdot t_{w} \cdot c_{w}) + P(T^{+}) \cdot N \cdot P + (P(T^{+}) \cdot N \cdot t_{ap} \cdot c_{ap}) + (N \cdot A_{die} \cdot C_{sil})$$

Cost Saving

Incorporating Correction Factors : Analytical Framework

$$P(T^+) = P(T^+ \mid D^+)P(D^+) + P(T^+ \mid D^-)P(D^-)$$

$$P(T^+) = 1 - P(T^-)$$

$$P(T^-) = P(T^- \mid D^+)P(D^+) + P(T^- \mid D^-)P(D^-)$$

$$P(T^+ \mid D^+) = \frac{1 - P(T^-) - (P(T^+ \mid D^-)P(D^-)}{P(D^+)}$$

Used to Calculate Yielded Dies

Cost Savings/Die

$$\delta C = \frac{C_{oc_{ap}}}{(N \cdot Y)} - \frac{C_{oc_{wap}}}{N \cdot Y \cdot P(T^+ \mid D^+)}$$

Analysis Framework

- Mixed-Signal SoC consists of:
  - Flattened section of digital logic → industrial ASIC K
  - Pair of identical data converters → identical bit resolution

- Packaging cost : derived from published data [*], varied with size of die

- Three typical die sizes considered – (10,40,120) mm^2

- Cost of silicon : $0.1/ mm^2[*]

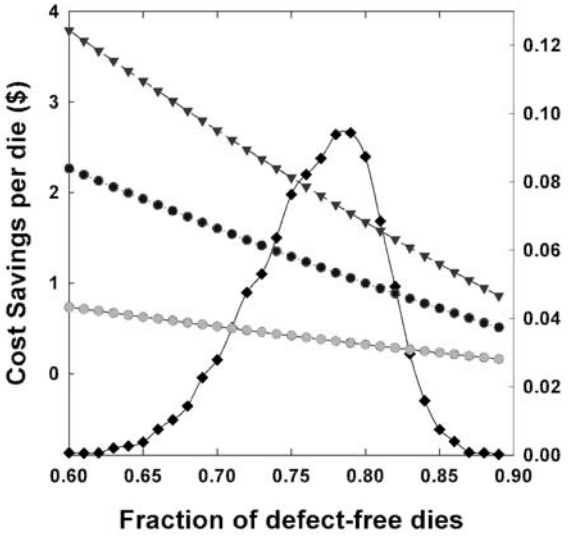
---

[*] A. B. Kahng, "The Road Ahead: The Significance of Packaging", IEEE Design & Test, Nov. 2002

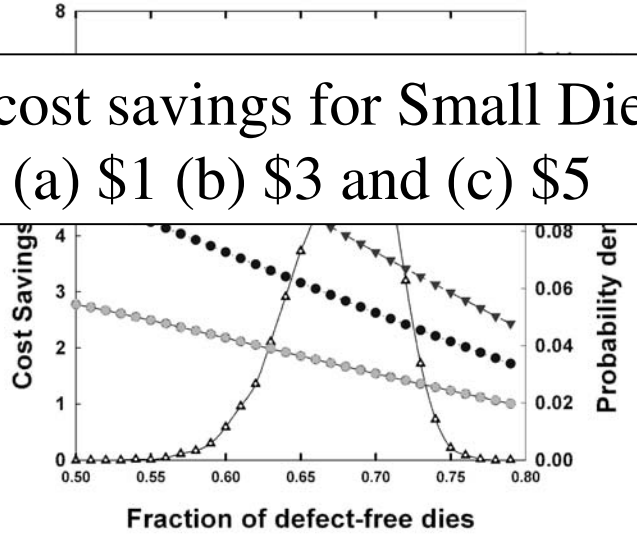
[*] International Technology Roadmap for Semiconductors: Assembly and Packaging, 2005

[*] http://www.mosis.org

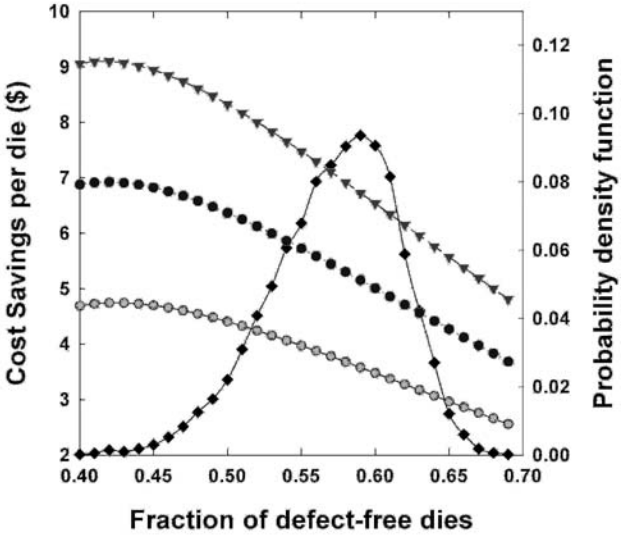
Quantitative Analysis



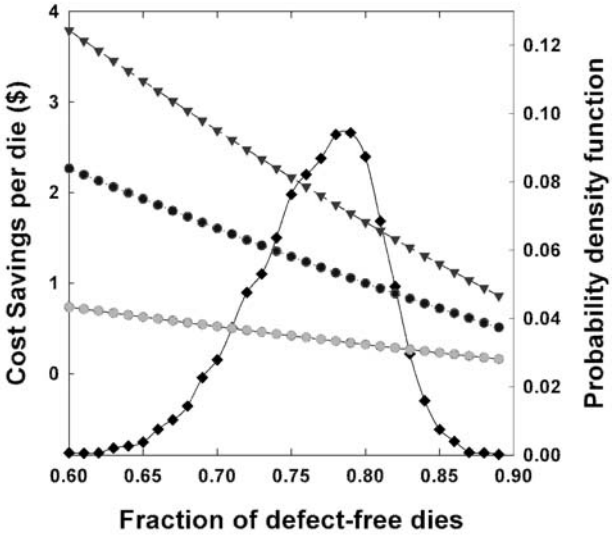
- Distributions of cost savings for Small Die
- Packaging Costs (a) $1 (b) $3 and (c) $5

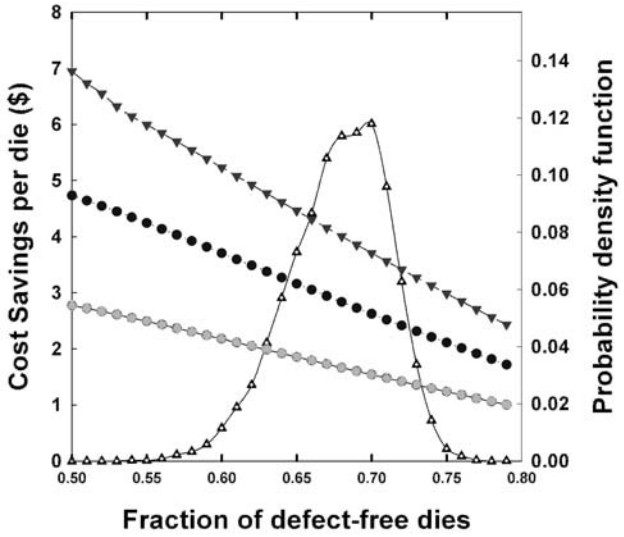


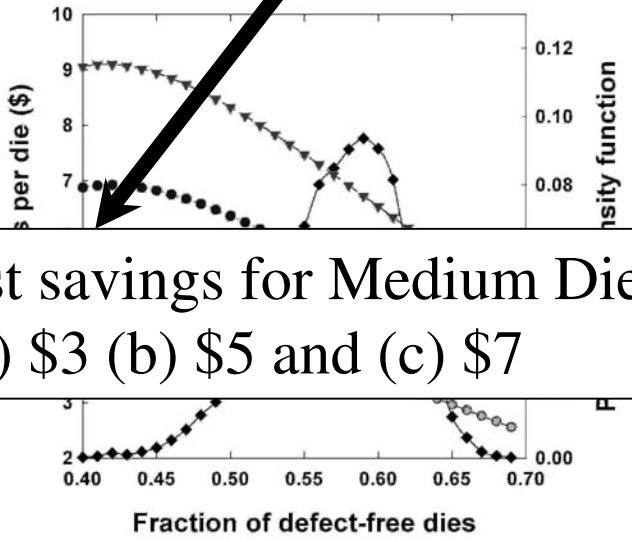
- Tester Cost : $0.30/sec
- ASIC Chip K : Tested with 4046 test patterns
- 50% of test escapes are due to mixed-signal cores
- Yield Distribution : Adjusted to die size



Quantitative Analysis





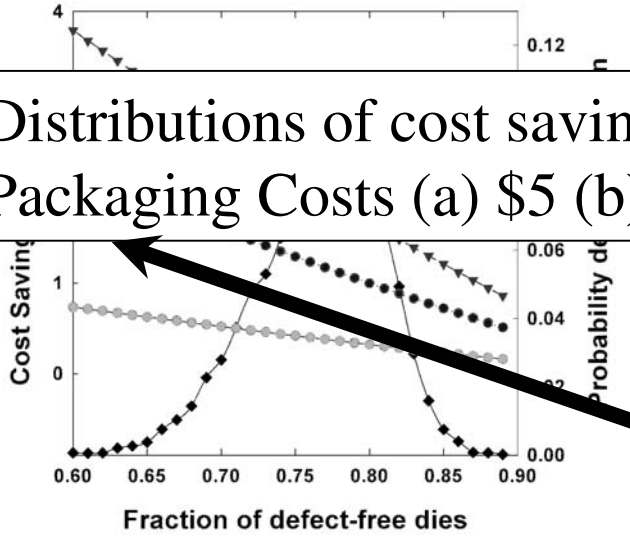


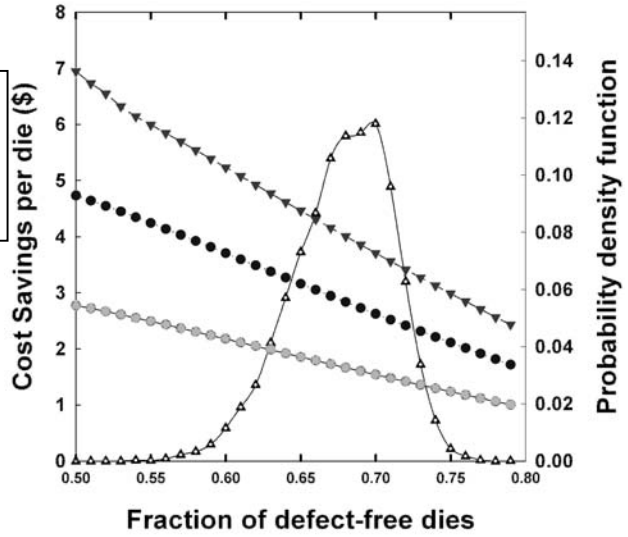
- Tester Cost : $0.30/sec
- ASIC Chip K : Tested with 4046 test patterns
- Test Escape : 50% for
cores
- Yield Distribution : Adjusted to die size

- Distributions of cost savings for Medium Die
- Packaging Costs (a) $3 (b) $5 and (c) $7

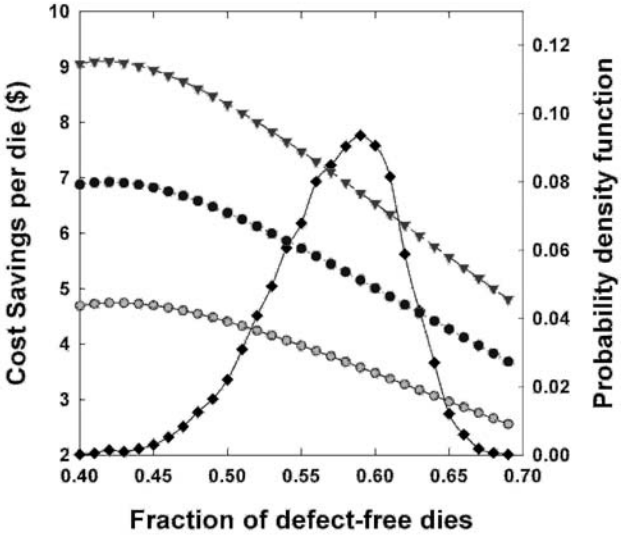
Quantitative Analysis

- Distributions of cost savings for Large Die
- Packaging Costs (a) $5 (b) $7 and (c) $9





- Tester Cost : $0.30/sec
- ASIC Chip K : Tested with 4046 test patterns
- Test Escape : 50% for mixed-signal cores
- Yield Distribution : Adjusted to die size



Conclusions

- Wafer-level defect screening technique suited for commercial "Big-D Small-A" mixed-signal SoCs
  - Using low cost digital tester
  - Significant percentage of moderate (26-92%) and gross failures (45-100%) can be screened at the wafer-level maintaining yield loss to a minimum (~1%)
- Cost model for a generic mixed-signal SoC
  - Benefits of wafer-level tests illustrated