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Design Consideration of 6.25 Gbps Signaling for High-Performance Server

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Outline

- High-speed server interconnects
- High-speed server interconnects design challenges
- 6.25 Gbps design over backplane
- Experiments
- Simulation and layout challenges
- Summary

High-Speed Server Interconnects

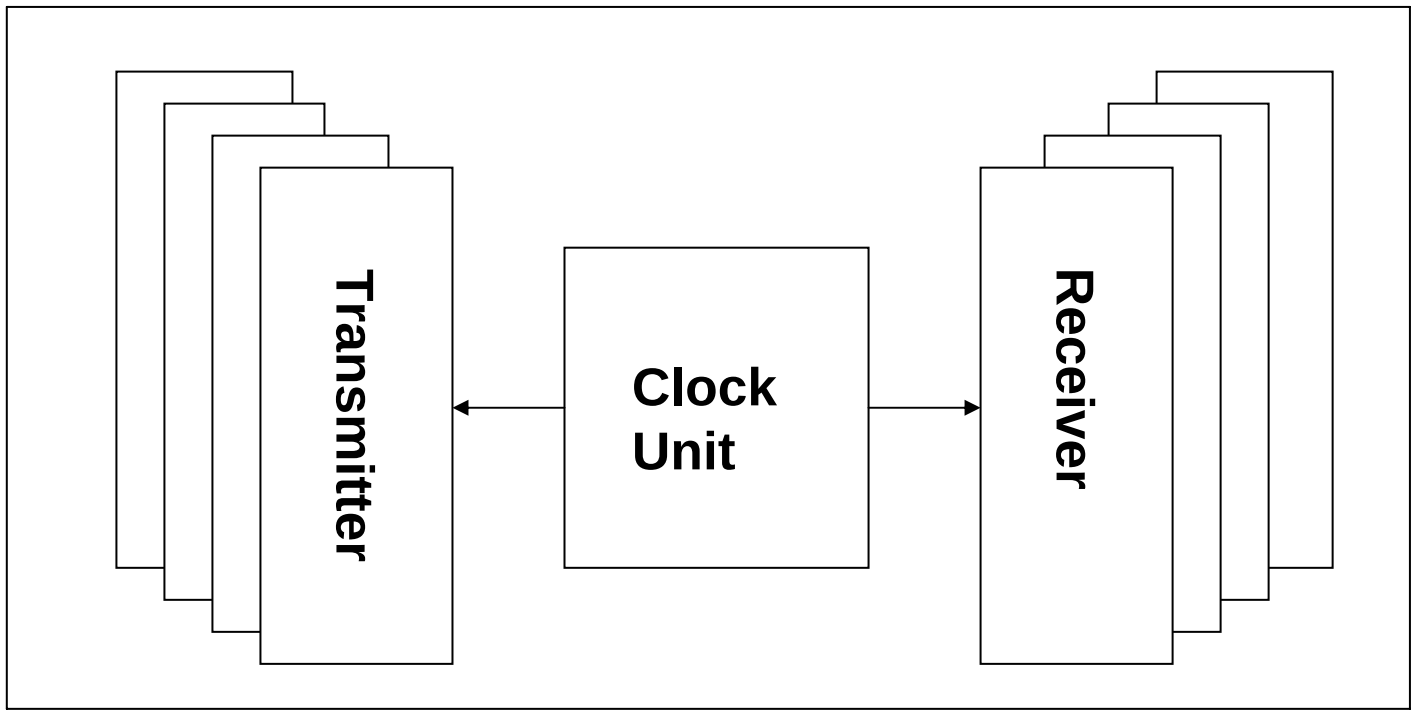
- **High-speed server interconnects**
  - **Link among high-speed servers**
  - **Multi-Gbps data rate**
  - **I/O standards such as 10G Ethernet, InfiniBand, PCI express and Fibre Channel**
- **High-speed interconnect medium**
  - **PCB – with length up to 50cm**
  - **Backplane – with multiple connectors, and PCB length up to 1m**
  - **High-performance copper cable – with length up to 15m**

High-Speed Server Interconnects Design Challenges

- **Speed**
  - **Data rate from one Gbps to ten Gbps**
- **Loss**
  - **Frequency-dependant amplitude loss in interconnect: skin effect, dielectric loss**
- **Power**
  - **Low power consumption**
  - **Low supply voltage (1.2V or less)**
- **Bit Error Rate (BER)**
  - **Very low Bit Error Rate**
- **Density**
  - **Multiple data ports for high bandwidth**

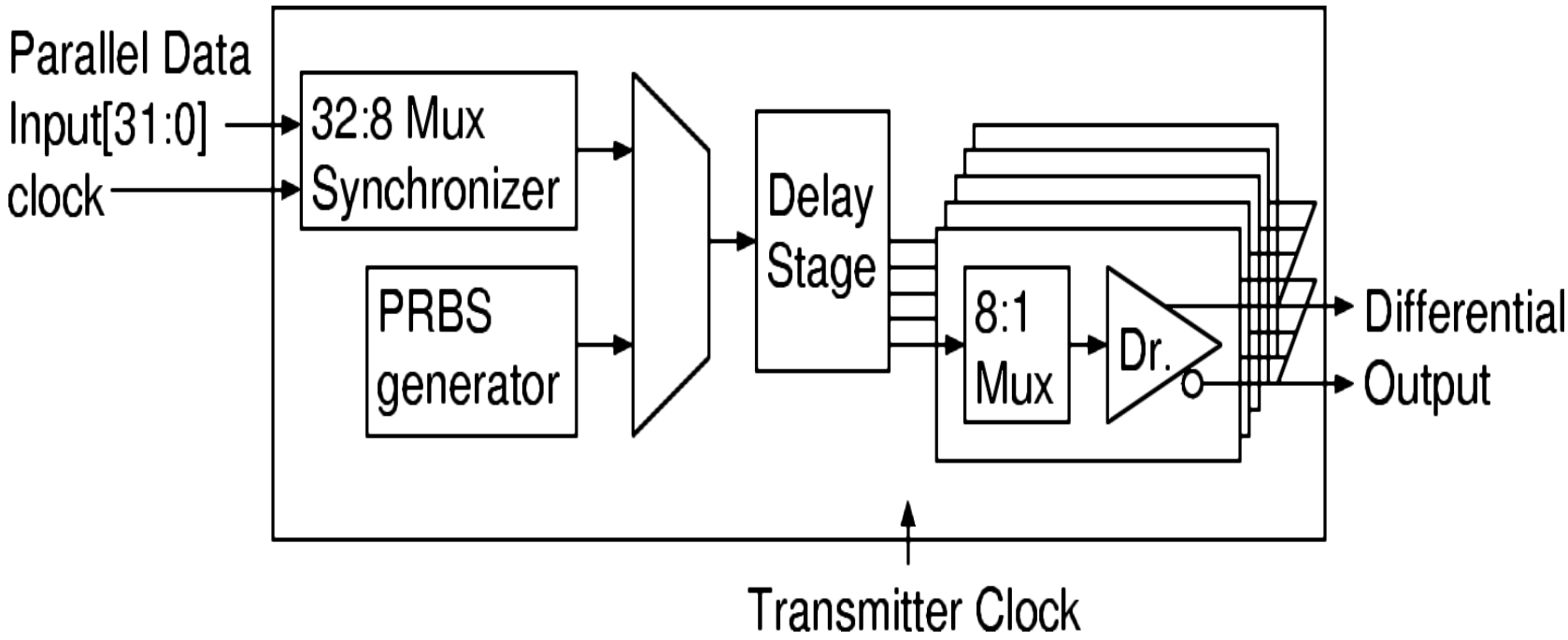
6.25 Gbps Macro

- 4 transmitter channels with equalizer
- 4 receiver channels with equalizer
- One clock unit

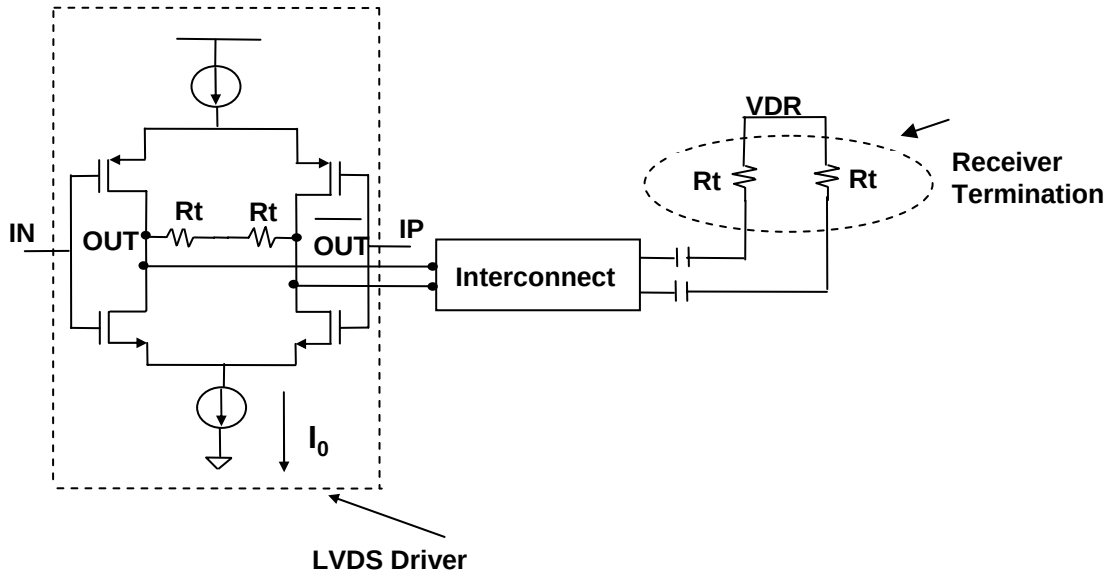


6.25 Gbps Macro

Transmitter

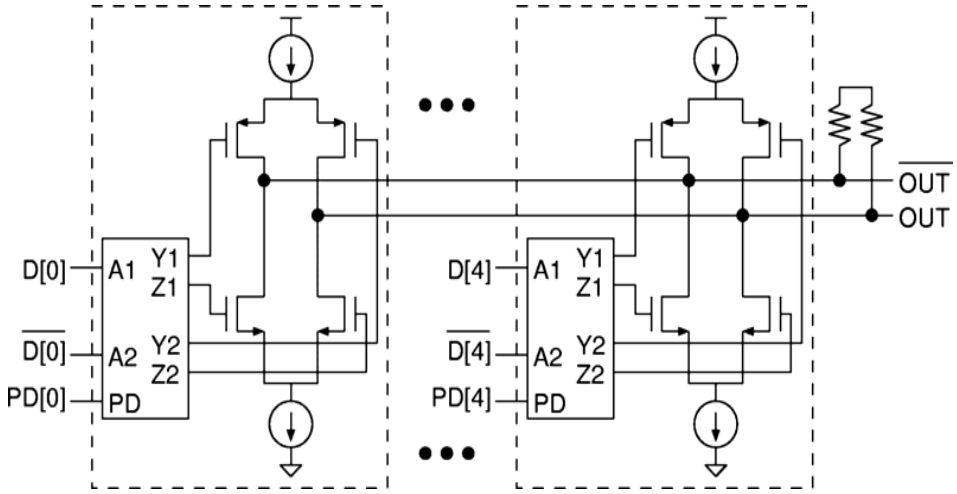


Transmitter Output Driver



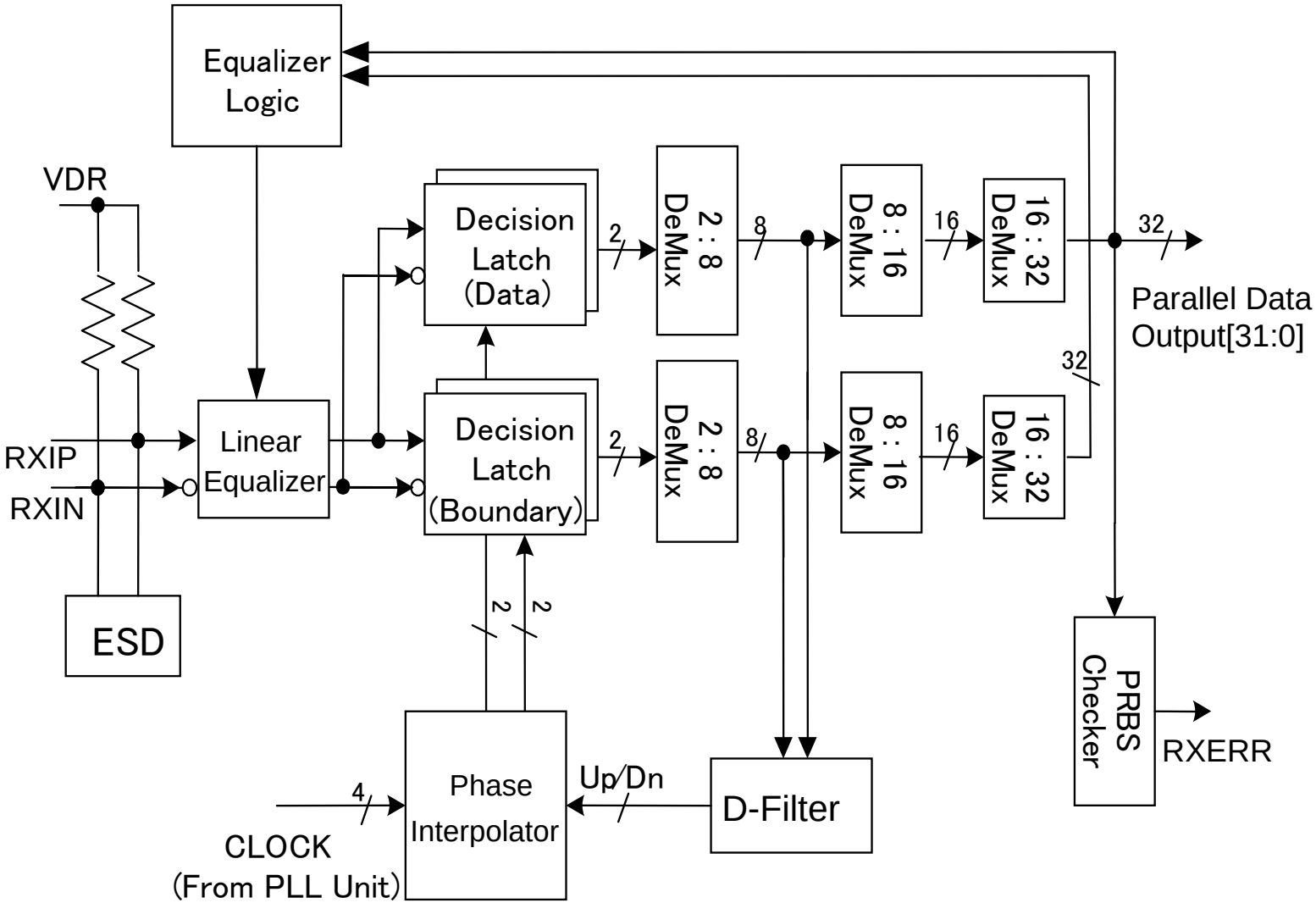
- **LVDS type driver**
  - **Low power – half of CML driver**
  - **Large amplitude swing – up to 700mV single end**
  - **1.2V power supply – same with other circuits**
  - **Multiple I/O standards compliant**

Multiple-Finger Output Stage

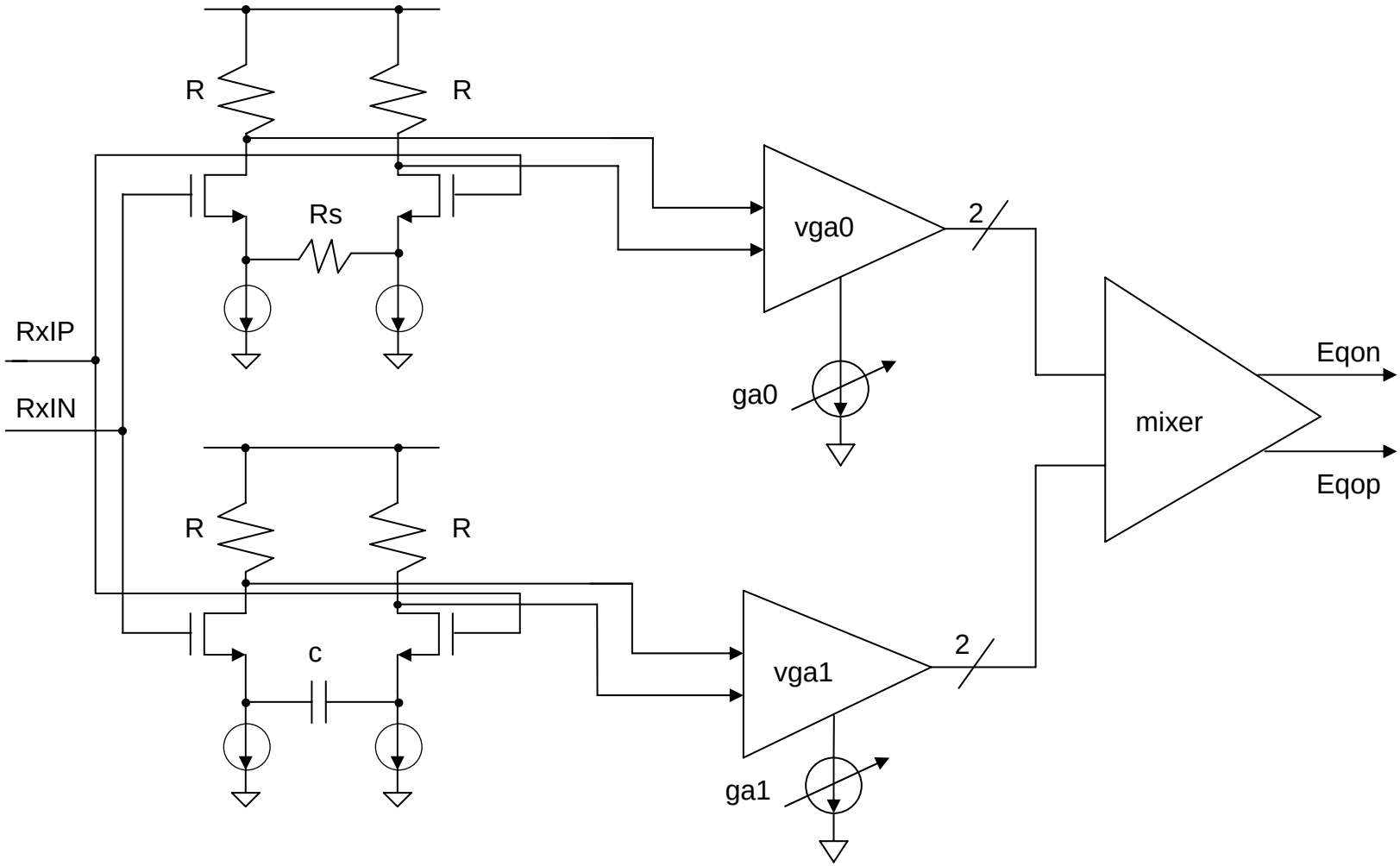


- **Transmitter pre-emphasis**
  - **2 to 5 tap FIR filter is formed with selected output stage, delay stage to compensate frequency-dependant loss**
- **Output slew rate control**
  - **Each output finger is turned on or off by associated logic value of PD**

Receiver


Equalizer Logic
VDR
RXIP
RXIN
ESD
Linear Equalizer
Decision Latch (Data)
Decision Latch (Boundary)
2
2 : 8 DeMux
8
8 : 16 DeMux
16
16 : 32 DeMux
32
Parallel Data Output[31:0]
PRBS Checker
RXERR
D-Filter
Up/Dn
Phase Interpolator
4
CLOCK (From PLL Unit)

Linear Analog Equalizer



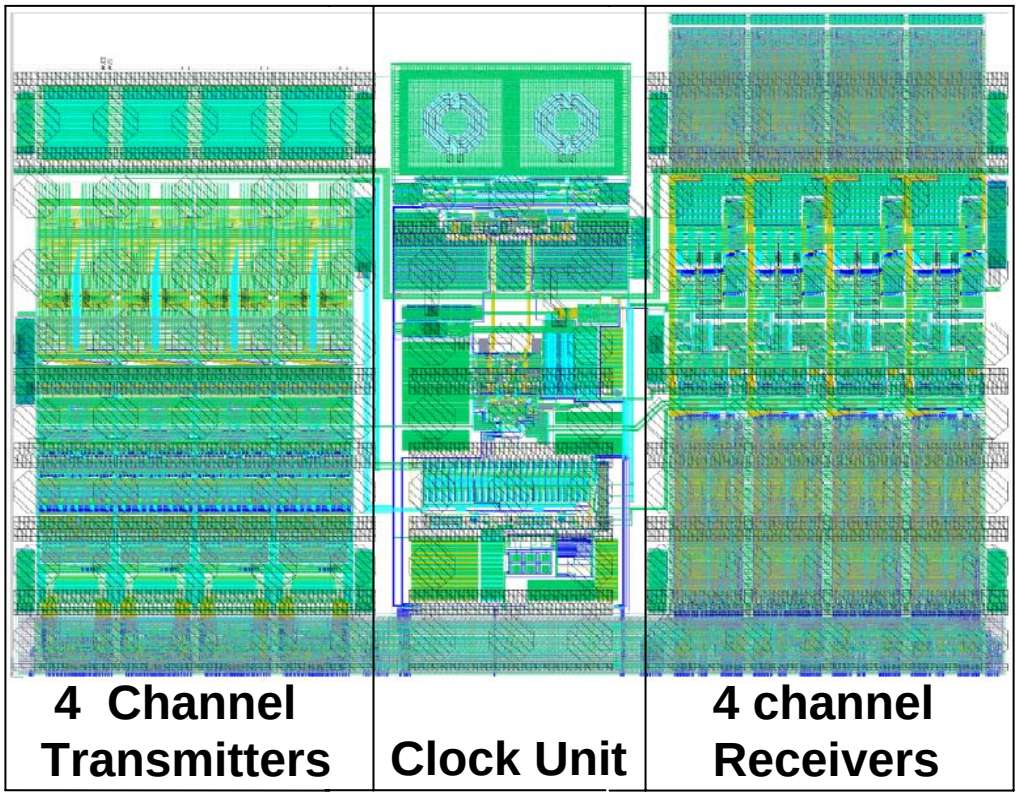
- **Frequency-dependent loss compensation**

Clock Unit

- Clock sources for transmitters and receivers
- Low jitter PLL circuits
  - Dedicated bandgap reference bias circuits
  - LC tank VCO
  - Differential clock buffer delivery

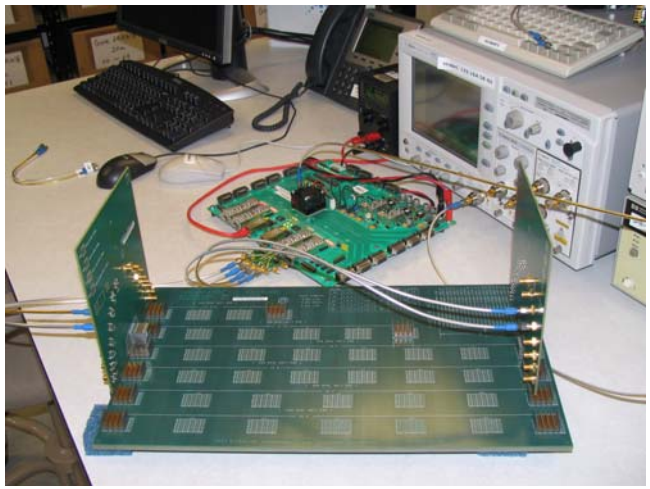
Implementation

- 90nm CMOS technology
- 1.2 V supply voltage except bandgap reference
- Data rate at 6.25 Gbps
- Power consumption 760mW(total)



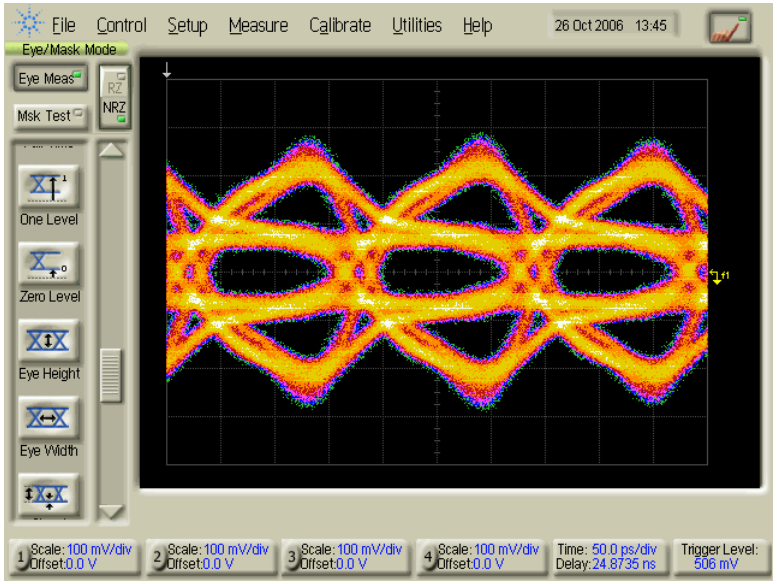
Experiments

- Transmitter → Backplane → Receiver
  - 2 connectors, 40” total PCB
  - 6.25 Gbps PRBS 23 data pattern
  - 3 taps transmitter pre-emphasis
  - Receiver equalization
  - Receiver BER < 10^{-15}

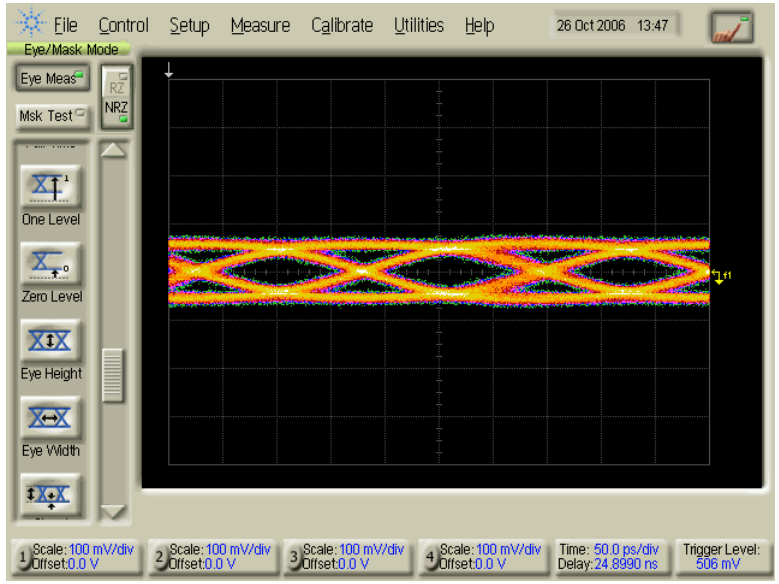


Experiments

- **Transmitter → Backplane → Receiver**



Transmitter near end eye diagram



Transmitter far end eye diagram

Simulation and Layout Challenges

- **Wide range of time constant**
  - **High-speed circuits (pico-second)**
  - **Control loop (milli-second)**
  - **Long transient simulation time because of resolutions**
- **Mixed-mode circuit simulator may not support all transmission line model**
  - **Partition circuit blocks**
  - **Use different simulators**
  - **Long simulation time**
- **Manual layout of all high-speed analog cells**
- **No accurate and user-friendly electrical migration check tools**

Summary

- High-speed server interconnect challenges
- 6.25 Gbps signaling circuits design over backplane
- Experiment results of 6.25 Gbps for backplane operation
- Simulation and layout challenges