System Co-Design and Co-Analysis Approach to Implementing the XDR™ Memory System of the Cell Broadband Engine™ Processor

Realizing 3.2 Gbps Data Rate per Memory Lane in Low Cost, High Volume Production

Wai-Yeung Yip, Scott Best, Wendem Beyene, Ralf Schmitt
Rambus Inc
Los Altos, CA, USA

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Agenda

- Motivation
- PLAYSTATION®3 (PS3™) Memory System
- XIO (XDR™ I/O) Clock Generation
- Power Distribution System Design & Analysis
- Designing for Low Cost Manufacturing Tolerances
- Summary

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Motivation

- The Cell Broadband Engine™ (Cell B.E.), designed for PS3, must be manufacturable at low cost and in high volume
- High speed interfaces have little margin to give
  - Bit time of the Cell B.E. XDR memory system is only 312.5 ps
  - Traditional system design and analysis approach may not have worked in implementing such a system cost-effectively

*** Cell Broadband Engine is a trademark of Sony Computer Entertainment Inc.**

Traditional Design/Analysis Approach

- Components may be designed and optimized independent of each other
  - Components may be designed by teams across multiple companies, at different design stages
  - Silicon may be designed independent of package & PCB
  - DRAM may be designed independent of memory controller physical layer (PHY)

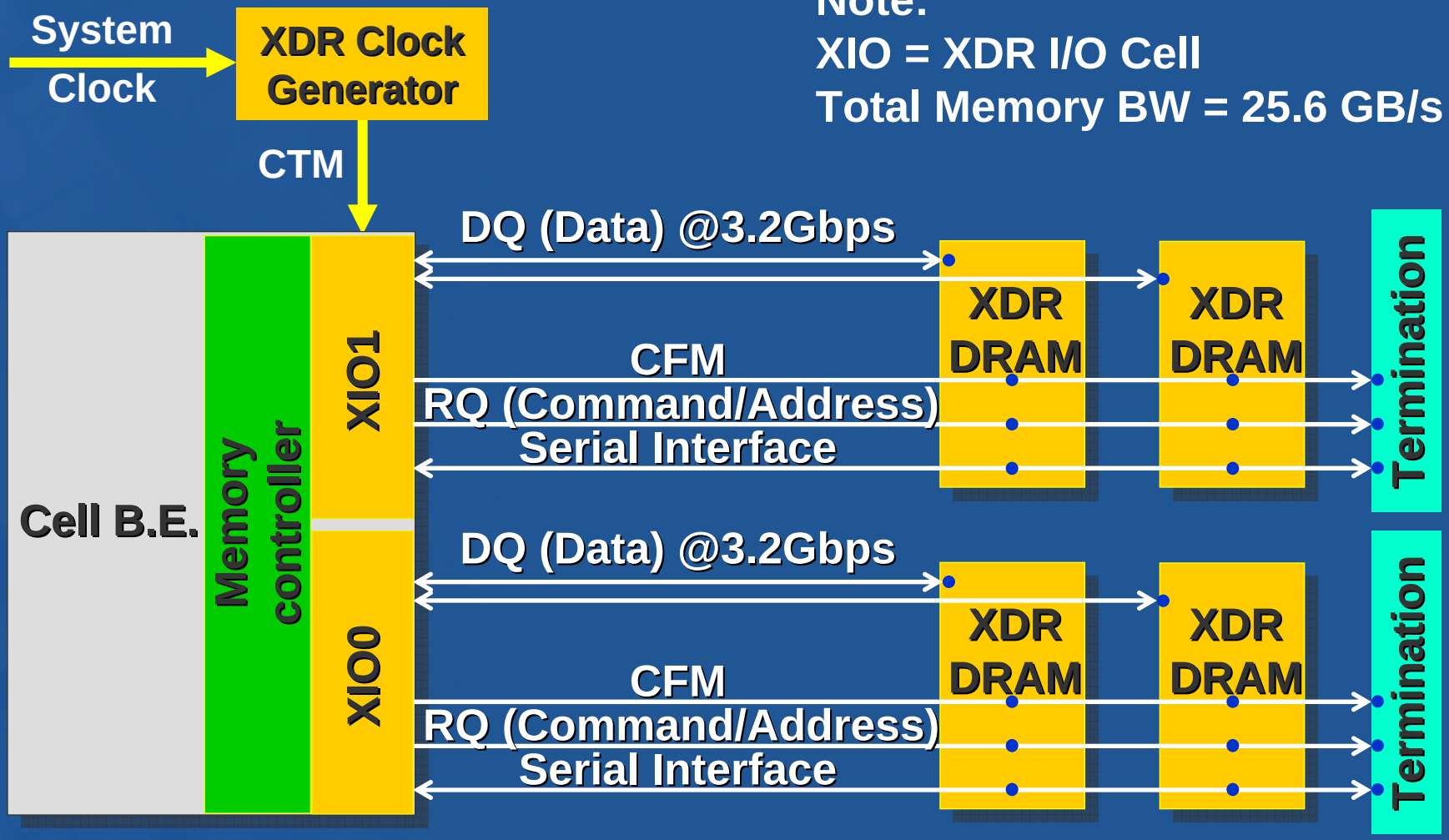
System Co-Design/Co-Analysis Approach

- Different components of the XDR memory system were designed and analyzed simultaneously
  - Including XIO, DRAM device, clock chip, packages, and PCB
  - System level analysis and optimization performed taking into consideration interactions between components before the design of any component was finalized

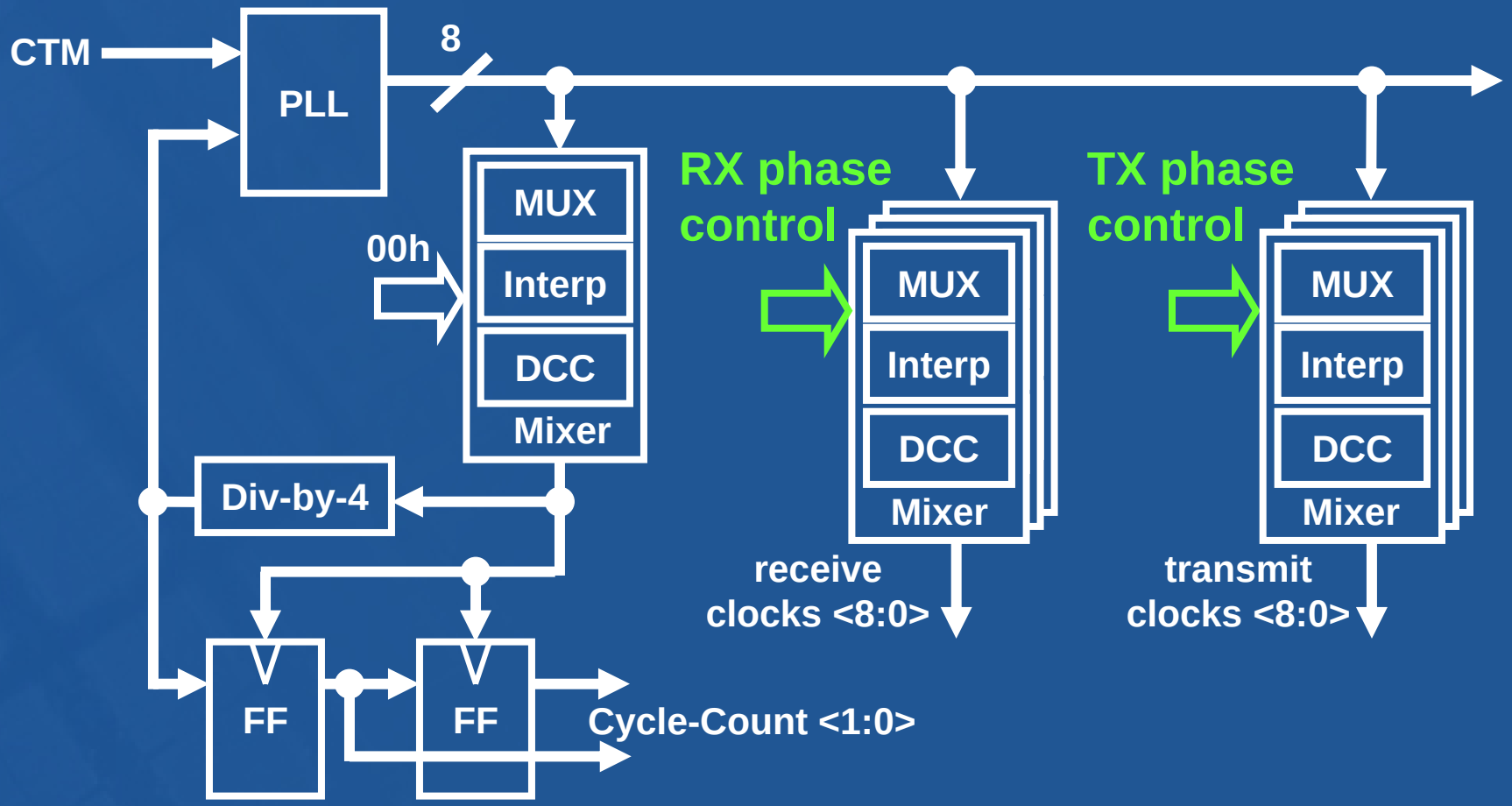
Merits of Co-Design/Co-Analysis Approach

- Allows best trade-off between system cost & performance
- Uncovers potential power integrity and signal integrity issues at system level early in the design cycle
  - Allows resolution of such issues with a combination of architectural, circuit, package, & PCB improvements
  - Results in solutions with the lowest system cost

PS3 Memory System Block Diagram



XIO Clock Generation Circuit



Per-Byte Block Diagram

XIO Clock Generation Circuit Features

- Both TX (write) and RX (read) mixers for precision phase control were implemented in the XIO
  - No phase mixers in the DRAM to keep its cost low
- Each DQ (data) bit has its own independent controls
  - Data-to-data PCB trace length matching not required resulting in simpler PCB layout in smaller area

Power Distribution System Design/Analysis

- Power Integrity considered from start of design process
- Power Integrity analyzed at system level
  - Every component of the power distribution system included in the model
  - Explored different trade-offs to arrive at most cost-effective power distribution system design

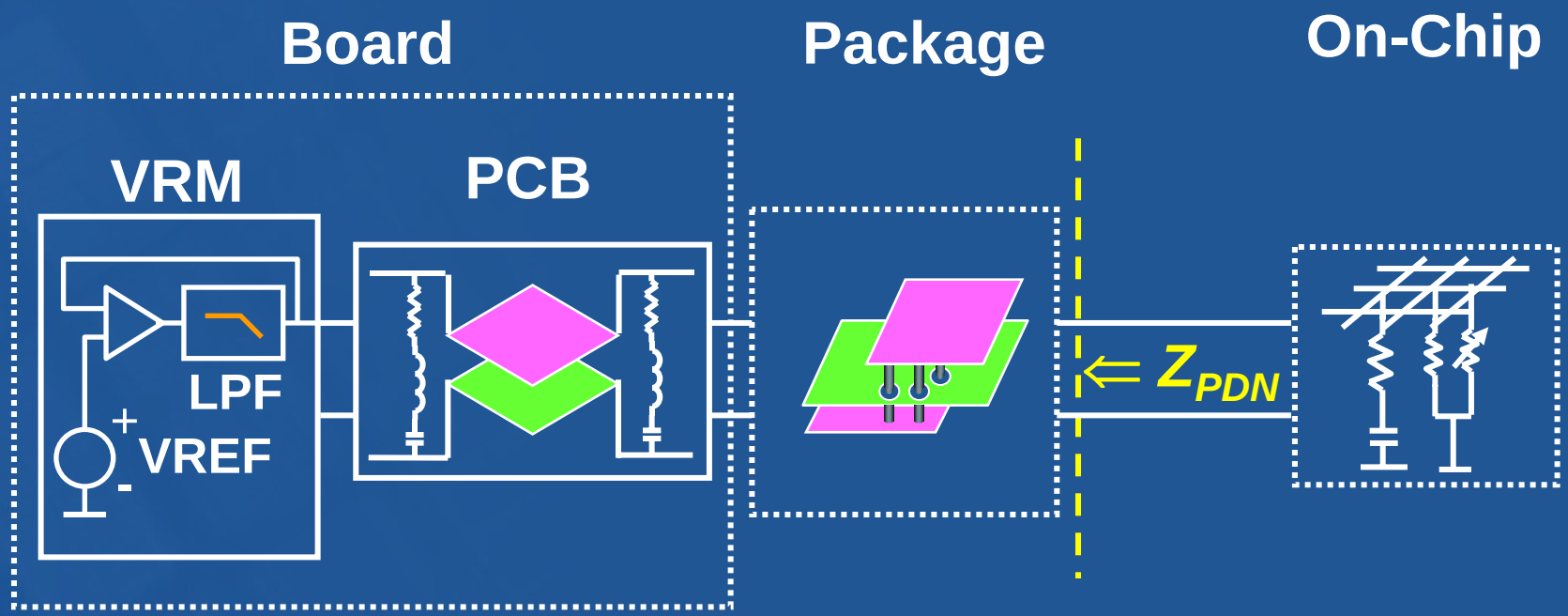
Optimally Accurate Analysis Approach

- Power distribution system consists of multiple components: VRM, PCB, package, chip
- Relative significance of a component in power integrity depends on the noise frequency
- Performed separate power integrity analyses, one for each frequency range
- In each frequency range, simplified models of components whose contribution to power supply noise is relatively small

Power Integrity Analyses

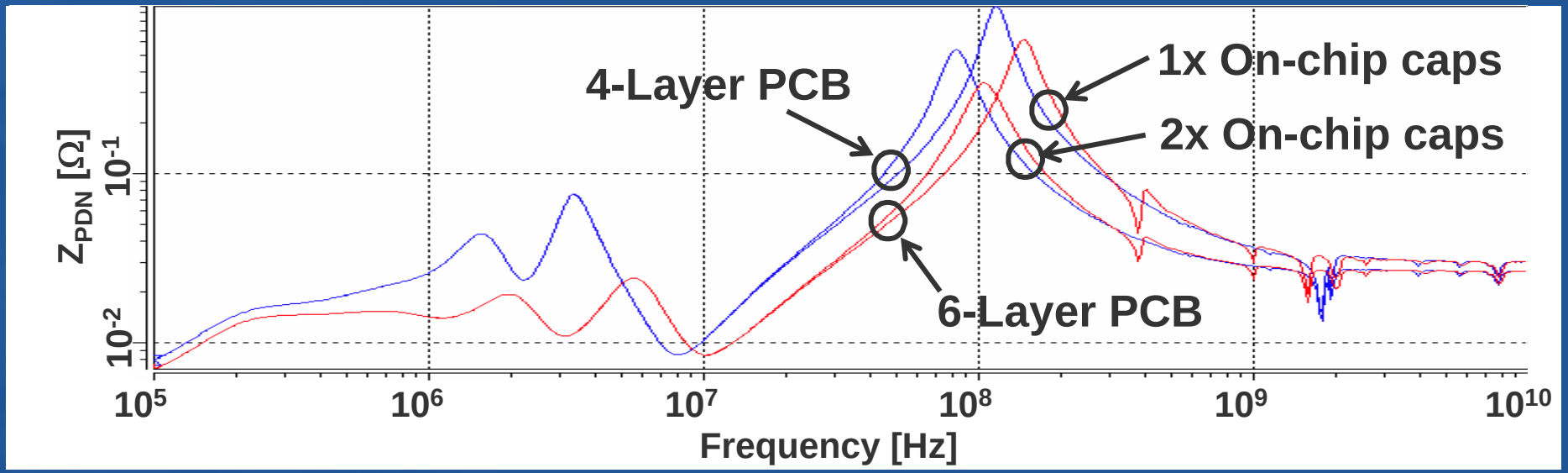
- On-chip IR drop analysis
  - Voltage drop due to resistance of on-chip wires
  - Package & PCB models removed due to relatively low resistance
- High-frequency noise analysis
  - Voltage noise due to high frequency switching of core & I/O
  - Package & PCB models simplified to an inductor
- Medium-frequency noise analysis
  - Voltage noise due to medium frequency switching of core & I/O
  - On-chip power distribution and decoupling capacitor model simplified to a lumped RC network

Power Distribution System Components



Note:
PDN = Power distribution network
VRM = Voltage Regulator Module

Power Integrity Trade-off Analysis



- Resonance peak in medium frequency can be lowered in two different ways
  - Convert from 4 to 6-layer PCB, or
  - Double amount of on-chip capacitance
- Choose solution with a lower system cost

Low Cost Manufacturing Tolerances

- Design parameters allowed to vary from their nominal values within tolerances to minimize manufacturing costs
  - PCB impedance allowed to vary by ±15%
  - Package impedance allowed to vary by ±20%
- Such parameter variations result in variations in voltage and timing margins
- Signal integrity analysis to quantify such variations can be computationally expensive

Statistical Analysis Methods

- Statistical signal integrity analysis methods explored to find an accurate approach with low computational cost
- Taguchi-based method
  - Uses an orthogonal array to minimize amount of simulations needed to explore design space
  - Generates accurate voltage & timing margin distributions
  - Provides insight into parameter sensitivities

Orthogonal Arrays

- An orthogonal array consists of columns which are mutually orthogonal
- For any pair of columns, all combinations of factor levels occur an equal number of times

	Factor 1	Factor 2	Factor 3
Simulation 1	L	L	L
Simulation 2	L	H	H
Simulation 3	H	L	H
Simulation 4	H	H	L

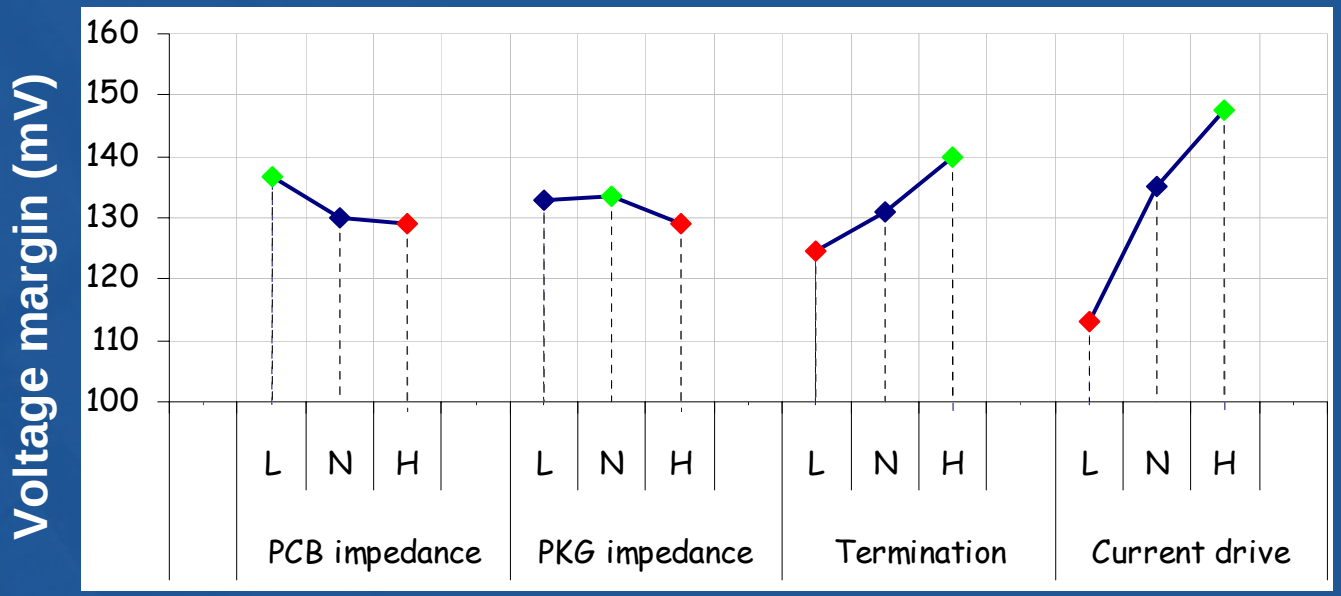
Comparison of Statistical Methods

- Taguchi-based method yields similar distribution as Monte Carlo at a much lower computational cost

Eye Height Statistics	Monte Carlo	Taguchi Based
Mean	0.341	0.334
Std. Deviation	0.038	0.036
Kurtosis	-0.473	-0.583
Skewness	0.187	-0.043
Minimum	0.244	0.237
Maximum	0.456	0.434
# of Simulations	5000	27
Simulation Time (hours)	210	1

Factor Effects Plots

- Taguchi-based method yields factor effects plots
  - Reveal sensitivity of system performance to individual design parameters
  - Facilitate design trade-off to optimize performance at low overall system cost



Summary

- System Co-Design & Co-Analysis approach applied to the implementation of the XDR memory system of the Cell B.E. processor
  - Allowed best trade-off between system cost and performance
- Precision phase control circuits implemented in the XIO to lower cost of DRAM and PCB design
- Optimally accurate approach applied to system-level power integrity analysis at low computational cost
- Taguchi-based statistical approach quantified signal integrity variations resulting from manufacturing tolerances at low computational cost