ASP-DAC 2007

Contents

Highlights

Opening & Keynote I

Wednesday, January 24, 8:30-10:00, Small Auditorium, 5F

"Next-generation Design and EDA Challenges: Small Physics, Big Systems, and Tall Toolchains"
Rob A. Rutenbar - Electrical & Computer Engineering, Carnegie Mellon University, United States

Keynote II

Thursday, January 25, 9:00-10:00, Small Auditorium, 5F

"Meeting with the Forthcoming IC Design — The Era of Power, Variability and NRE Explosion and a Bit of the Future —"
Takayasu Sakurai - Center for Collaborative Research, and Institute of Industrial Science, University of Tokyo, Japan

Keynote III

Friday, January 26, 9:00-10:00, Small Auditorium, 5F

"How Foundry can Help Improve your Bottomline? Accuracy Matters!"
Fu-Chieh Hsu - Vice President of Design and Technology Platform, Taiwan Semiconductor Manufacturing Company, Taiwan

Special Sessions

1D: Wednesday, January 24, 10:15-12:20, Room 416+417
Presentation + Poster Discussion: "University Design Contest" **(See page 19 for more details.)**

2D: Wednesday, January 24, 13:30-15:35, Room 416+417
Invited Talks + Panel Discussion: "Design for Manufacturability"

2D-1: Modeling Sub-90nm On-chip Variation for DFM
Kelvin Doong (TSMC, Taiwan)
2D-2: DFM Reality in Sub-nanometer IC Design
Nishath Verghese (Clear Shape, United States)
2D-3: DFM/DFY Practices during Physical Designs for Timing, Signal Integrity, and Power
Jiing-Yuan Lin (Global Unichip, Taiwan)
2D-4: Advanced Academic Researches Pertinent to DFM
Ting-Chi Wang (NTHU, Taiwan)
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Panelists: Kelvin Doong (TSMC, Taiwan)
Nishath Verghese (Clear Shape, United States)
Jiing-Yuan Lin (Global Unichip, Taiwan)
Ting-Chi Wang (NTHU, Taiwan)
Andrew Kahng (Blaze DFM, United States)

3D: Wednesday, January 24, 16:00-18:05, Room 416+417
Invited Talks: "Embedded Software for Multiprocessor Systems-on-Chip"

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Soonhoi Ha (SNU, Korea)
3D-2: RTOS and Codesign Toolkit for Multiprocessor Systems-on-chip
Shinya Honda (Nagoya Univ., Japan)
3D-3: Energy-efficient Real-time Task Scheduling in Multiprocessor DVS Systems
Jian-Jia Chen (National Taiwan Univ., Taiwan)
3D-4: Towards Scalable and Secure Execution Platform for Embedded Systems
Junji Sakai (NEC, Japan)

4D: Thursday, January 25, 10:15-12:20, Room 416+417
Invited Talks: "EDA Challenges for Analog/RF"

7D: Friday, January 26, 10:15-12:20, Room 416+417
Panel Discussion: "Multi-Processor Platforms for Next Generation Embedded Systems"
Organizer: Nikil Dutt (Univ. of California, Irvine, United States)
Panelists: Chris Rowen (Tensilica, United States)
Kazuyuki Hirata (ARM, Japan)
Peter Hofstee (IBM, United States)
Rudy Lauwereins (IMEC, Belgium)
Pierre Paulin (STMicroelectronics, Canada)

Designers' Forum

5D: Thursday, January 25, 13:30-15:35, Small Auditorium, 5F
Panel Discussion : "Presilicon SoC HW/SW Verification"
Organizer: Tetsuji Sumioka (Sony, Japan)
Moderator: Tetsuji Sumioka (Sony, Japan)
Panelists: Jason Andrews (Cadence, United States)
Graham Hellestrand (VaST Systems Technology, United States)
Hidefumi Kurokawa (NEC Electronics, Japan)
Ilya Klebanov (ATI Technologies, United States)
Seiji Koino (Toshiba, Japan)

6D: Thursday, January 25, 16:00-17:50, Small Auditorium, 5F
Invited Talks: "Low-power SoC Technologies"

6D-1: The Development of Low-power and Real-time VC-1/H.264/MPEG4 Video Processing Hardware

Masaru Hase (Renesas Technology, Japan)

6D-2: Development of Low Power ISDB-T One-segment Decoder by Mobile Multi-media Engine SoC (S1G)

Koichi Mori, Masakazu Suzuki, Yasuo Ohara, Satoru Matsuo, Atsushi Asano (Toshiba, Japan)

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Masaitsu Nakajima, Takao Yamamoto, Masayuki Yamasaki, Masaya Sumita (Matsushita Electric Industrial, Japan)

8D: Friday, January 26, 13:30-15:35, Small Auditorium, 5F

Invited Talks: "High-speed Chip to Chip Signaling Solutions"

8D-1: Preferable Improvements and Changes to FB-DiMM High-speed Channel for 9.6Gbps Operation

Atsushi Hiraishi, Toshio Sugano (Elpida Memory, Japan), Hideki Kusamitsu (Yamaichi Electronics)

8D-2: Xbox360 Front Side Bus - A 21.6 G B/s End to End Interface Design

David Siljenberg, Steve Baumgartner, Tim Buchholtz, Mark Maxson (IBM, United States)

8D-3: High-speed Signaling Technology for Servers

Jian Hong Jiang (Fujitsu Laboratories of America, United States)

8D-4: System Co-design and Analysis Approach to Implementing the XDR Memory System of the Cell Processor Realizing 3.2 Gbps in Low Cost, High Volume Production

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9D: Friday, January 26, 16:00-18:05, Small Auditorium, 5F

Panel Disussion: "Top 10 Design Issues"

Organizer: Takeshi Yamamura (Fujitsu Laboratory, Japan)
Moderator: Peter Hofstee (IBM, United States)
Panelists: TBD

Two Full-Day and Four Half-Day Tutorials

FULL-DAY Tutorials:
Tuesday, January 23, 2007, 9:30-17:00

1 **DFM Tools, Methodologies and Practice at 65nm and Beyond**

Organizer: ***Andrew B. Kahng*** - Univ. of California, San Diego, United States

Speakers: ***N. S. Nagaraj*** - Texas Instruments, United States, ***Jean-Pierre Schoellkopf*** - STMicroelectronics, France, ***Mike Smayling*** - Applied Materials, United States, ***Ban P. Wong*** - Chartered Semiconductor, United States, ***Andrew B. Kahng*** - Univ. of California, San Diego, United States

2 **Functional Verification Planning and Management — The Road to Verification Closure is Paved with Good Intentions**

Organizers: ***Andrew Piziali*** - Cadence, United States, ***Avi Ziv*** - IBM, Islael

Speakers: ***Andrew Piziali*** - Cadence, United States, ***Avi Ziv*** - IBM, Islael

HALF-DAY Tutorials:
Tuesday, January 23, 2007, 9:30-12:30

3 **Low Power CMOS Design: The Fabrics: Research Front-end**

Organizer: ***Tadahiro Kuroda*** - Keio Univ., Japan

Speakers: ***Hitoshi Wakabayashi*** - Sony, Japan, ***Tadahiro Kuroda*** - Keio Univ., Japan, ***Ankur Gupta*** - Cadence, United States, ***Luca Benini*** - Bologna Univ., Italy

Tuesday, January 23, 2007, 14:00-17:00

4 **Low Power CMOS Design: The Applications: State-of-the-art Practice**

Organizer: ***Tadahiro Kuroda*** - Keio Univ., Japan

Speakers: ***Toshihiro Hattori*** - Renesas, Japan, ***Atsuki Inoue*** - Fujitsu Laboratory, Japan, ***Masaya Sumita*** - Panasonic, Japan, ***Mototsugu Hamada*** - Toshiba, Japan

Tuesday, January 23, 2007, 9:30-12:30

5 **Fast Physical Synthesis for Multi-million Gate ASIC Designs**

Organizer: ***Charles J. Alpert*** - IBM, United States

Speaker: ***Charles J. Alpert*** - IBM, United States

Tuesday, January 23, 2007, 14:00-17:00

6 **Concepts and Tools for Practical Embedded System Design**

Organizer: ***Nikil Dutt*** - Univ. of California, Irvine, United States

Speakers: ***Daniel Gajski*** - Univ. of California, Irvine, United States, ***Andreas Gerstlauer*** - Univ. of California, Irvine, United States, ***Samar Abdi*** - Univ. of California, Irvine, United States

Welcome to ASP-DAC 2007

On behalf of the Organizing Committee, I would like to invite you to attend the Asia and South Pacific Design Automation Conference 2007 (ASP-DAC 2007). ASP-DAC 2007 will be held at Pacifico Yokohama, Japan, from January 23 through 26, 2007, jointly with the Electronic Design and Solution Fair 2007. I hope you visit the conference to learn about all the latest advances in electric design technology and automation.

The core of the conference is the technical program. This year, ASP-DAC received 408 submissions from 30 countries/regions. Based on the result of a rigorous and thorough review followed by a full day face-to-face discussion, 131 papers were selected and compiled into an exciting final program which is further enriched by multiple special sessions and panels.

Each day, the technical program starts with a keynote address. On Wednesday, Prof. Rob A. Rutenbar, Carnegie Mellon University, will explore next-generation design and EDA challenges. On Thursday, Prof. Takayasu Sakurai, University of Tokyo, will discuss fundamental issues in nano-meter CMOS design. On Friday, Dr. Fu-Chieh Hsu, TSMC, will explain their effort for improving process data accuracy.

Last year, ASP-DAC successfully launched a new program called Designers' Forum that shares design experience and solutions of real product designs of the industries. This year's program includes oral sessions of low-power design and high-speed signaling, panels of top 10 design issues and HW/SW verification.

The University Design Contest is also an important annual event of ASP-DAC where 18 designs were selected for presentation. On Tuesday, two full-day and four half-day tutorials are scheduled to provide introductions to hot topics such as DFM, low-power, verification, physical design, and embedded system design.

As we are going into the era of nano-scale integrated circuits, many issues will confront us such as complexity, manufacturability, and power dissipation. These issues can be overcome by tighter collaboration than ever among EDA researchers, designers, manufacturers, and application engineers. ASP-DAC 2007 offers an ideal place for all these people to meet and exchange ideas about the challenges and solutions for the future. We are looking forward to an exciting ASP-DAC 2007, and we hope that you will join us in January.

Hidetoshi Onodera
General Chair
ASP-DAC 2007

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[6] Physical Design (Placement)

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[7] Timing, Power, Signal/Power Integrity Analysis and Optimization

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[8] Interconnect, Device and Circuit Modeling and Simulation

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[9] Test and Design for Testability

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[10] Analog, RF and Mixed Signal Design and CAD

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[11] Leading Edge Design Methodology for SOCs and SIPs

∗**Hideharu Amano**
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University LSI Design Contest

The University LSI Design Contest was conceived as a unique program of ASP-DAC Conference. The purpose of the Contest is to encourage education and research in LSI design, and its realization on chips at universities, and other educational organizations by providing opportunities to present and discuss innovative and state-of-the-art designs at the conference. Application areas and types of circuits include (1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal processing, (3) Microprocessors, and (4) Custom Application Specific Circuits and Memories. Methods or technology used for implementation include (a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices, including FPGA/PLDs.

This year, eighteen selected designs from two countries/areas will be disclosed in Session 1D with a short presentations followed by live discussions in front of posters with light meals. Submitted designs were reviewed by the members of the University Design Contest Committee based on the following criteria: Reliability of design and implementation, Quality of implementation, Performance of the design, Novelty, and Additional special features. In the selection process, emphasis was placed more on reliability, quality, and performance. As a result, the eighteen designs were selected. Also, we have instituted one outstanding design award and two special feature awards.

It is with great pleasure that we acknowledge the contributions to the Design Contest, and it is our earnest belief that it will promote and enhance research and education in LSI design in academic organizations. It is also our hope that many people not only in academia but in industry will attend the contest and enjoy the stimulating discussions.

Date, Time and Locations:

Oral Presentation 10:15-12:20, January 24, 2007, Room 416+417
Poster Presentation 12:20-13:30, January 24, 2007, Room 418 (Food will be served.)

University LSI Design Contest Committee

Chair
Makoto Nagata
Kobe University

Designers' Forum

Designers' Forum is conceived as a unique program that shares design experience and solutions of real product designs of the industries among LSI/PCB designers and EDA academia/developers. It consists of these four special sessions.

Oral Sessions:	6D High-speed Chip to Chip Signaling Solutions
	8D Low-power SoC Technologies
Panel Discussions:	5D Presilicon SoC HW/SW Verification
	9D Top 10 Design Issues

Here, designs will be presented focusing on design styles, design issues, and ways to tackle design issues. Panel discussions will also be held for the latest design issues. Detailed information of each session is as follows.

Session 6D (16:00-17:50, Jan 25th) [Low-power SoC Technologies] — This session deals with brand-new low-power SoC technologies for mobile digital consumer electronics. 3 presentation will be shown from Renesas, Toshiba and Matsushita. Renenas introduces a dedicated multimedia hardware embedded on SH-mobile. Toshiba shows a digital-TV decoder based on a configurable processor "MeP". Matsushita introduces miscellaneous low power technologies on an SoC Platform called "Uniphier".

Session 8D (13:30-15:35, Jan 26th) [High-speed Chip to Chip Signaling Solutions] — 4 presentations will be shown related to board or system level designs on PCs, games and servers given by Elpida, IBM, Fujitsu Lab. and Rambus. Elpida shows a 9.6Gbs FB-DiMM interface technology. IBM overviews a 21.6Gbs interface design on Xbox360. Fujitsu Lab. introduces a 6.25Gbs cable link for servers. Rambus describes a 3.2Gbps XDR memory system for the Cell processor.

Session 5D (13:30-15:35, Jan 25th) [Presilicon SoC HW/SW Verification] — Panelists discuss with verification technologies on system levels including hardwares and softwares prior to LSI fabrication. Three panelists are LSI designers for digital TV application and two panelists are from EDA vendors, The point of discussion is how to develop software using emulators, co-simulation and other technologies.

Session 9D (16:00-18:05, Jan 26th) [Top10 Design Issues] — Panelists will focus on the top 10 design issues seen by LSI designers and EDA vendors.

Designers' Forum Chair
Haruyuki Tago
Toshiba Corporation
Designers' Forum Vice Chair
Kazutoshi Kobayashi
Kyoto University

Student Forum at ASP-DAC 2007

A poster session for graduate students to present their research work is held during ASP-DAC 2007. This is a great opportunity for students to get feedback and have discussion with people from academia and industry.

Date and Time: 12:20-13:30, January 25, 2007

Location: Room 418 (Food will be served.)

We would like to thank the following poster selection committee members that evaluated the submissions,

- Ali Afzali-Kusha (Tehran University, Iran)
- Supratik Chakraborty (IIT Bombay, India)
- Naehyuk Chang (Seoul National University, South Korea)
- Sheqin Dong (Tsinghua University, China)
- Toru Ishihara (Kyushu University, Japan)
- Kazuhito Ito (Saitama University, Japan)
- Philip Leong (Chinese University of Hong Kong, Hong Kong)
- Hiroshi Saito (Aizu University, Japan)
- Omid Shoaei (University of Tehran, Iran)
- Makoto Sugihara (Institute of Systems and Information Technologies, Japan)
- Nozomu Togawa (Waseda University, Japan)

This forum is hosted by Tokyo section and Technical Group on VLSI Design Technologies (TGVLD) of the Institute of Electronics, Information and Communication Engineers (IEICE), which will give awards to outstanding presentations for encouragement of student activities. We would also like to thank the Engineering Sciences Society of the IEICE for providing travel grants and sponsoring the event. Special thanks to Dr. Farzan Fallah, Professors Shinji Kimura, Yoichi Shiraishi, Atsushi Takahashi, and Mr. Bakhtiar Affendi for supporting and contributing to the Student Forum.

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Invitation to ASP-DAC 2008

Welcome to Korea, where a dazzling progress in Information Technology is occurring in diverse areas like semiconductor, display, and mobile phone. On behalf of the Organizing Committee, it is my great pleasure to invite all of you to ASP-DAC 2008, which is the thirteenth in a series of ASP-DAC. ASP-DAC is now well stabilized in its position as the premier annual event of Electronic Design Automation and Design community in Asian and South Pacific region. ASP-DAC 2008 will be held in the COEX Conference Center, in the center of Seoul during January 21–24, 2008 including a one-day tutorial followed by technical session in three days, in three parallel tracks.

Technical Program Chair of ASP-DAC 2008 is Professor Kiyoung Choi from Seoul National University, Korea, and Technical Program Vice Chair is Professor Ren-Song Tsay from National Tsinghua University, Taiwan. Under their strong leadership, internationally organized Program Committee will structure ASP-DAC as a high-quality conference that emphasizes original contributions that open up new vistas in the field with significant theoretical and practical impact.

I would like to invite you to actively participate in the ASP-DAC 2008 in Seoul by submitting cutting-edge research results for publication, by proposing interesting topics for tutorials and special sessions, or simply by dropping by in January 2008 to enjoy diverse ASP-DAC events.

Expecting to see you in Seoul in 2008!

Chong-Min Kyung
General Chair
ASP-DAC 2008

About ASP-DAC

The ASP-DAC, is a premier Design Automation and Design conference, especially for Asian and South Pacific Electronic Design Automation and Design community, providing a forum to present and exchange ideas in order to promote the research, and accelerating cooperation between the IC Design and Design methodologies. The conference attendees are primarily developers of the EDA/CAD Tools and designers of VLSI circuits & systems (IP & SoC).

Keynote Addresses

Opening & Keynote I
Wednesday, January 24, 8:30-10:00,
Small Auditorium, 5F
"Next-Generation Design and EDA Challenges: Small Physics, Big Systems, and Tall Tool-Chains"

Rob A. Rutenbar
Electrical & Computer Engineering
Carnegie Mellon University, United States

There is much discussion of two challenges in the design of tomorrow's electronics: the difficult "small physics" of nanoscale transistors, and the silicon/software complexity of "big systems". But those of us who want to build beautiful algorithms have an additional hurdle: "tall tool-chains". If it takes 50 tool-steps to build an industrial-strength design flow, and each tool is based on 1-2 "big algorithms", does this mean that each new algorithm idea is worth, at best, 1-2% of the success of a design? This seems to me a bad way of accounting for the tremendous value that EDA brings to the world of design. How can we have a big impact in this important technology area?

In this talk, I will offer several pieces of advice for how not to get buried by the tall-tool-chain problem. I will discuss how to identify design problems that can have large impact, how to embrace the strange physics of tomorrow's silicon technologies in the service of building beautiful algorithms, and how to get fresh (and unique) insights on problems by spending time working with a real design team. I will use design examples ranging from lithography, to computational finance, to silicon-based speech recognition, to illustrate the point that this is an exciting time to be working on tomorrow's tool and design challenges.

Keynote II
Thursday, January 25, 9:00-10:00,
Small Auditorium, 5F
"Meeting with the Forthcoming IC Design — The Era of Power, Variability and NRE Explosion and a Bit of the Future —"

Takayasu Sakurai
Center for Collaborative Research, and
Institute of Industrial Science
University of Tokyo, Japan

In the foreseeable future, VLSI design will meet a couple of explosions: power, variability and NRE (non-recurring engineering cost). Some of the solutions for power-aware designs are covered in this talk with relation to variability. A remedy for the NRE explosion is to reduce the number of developments and manufacture and sell tens of millions of chips under a fixed design. System-in-a-Package approach may embody such possibility. Several new technologies are described to enable 3-dimensional stacking of chips to build high-performance yet low-power electronics systems.

On the other extreme of the silicon VLSI's which stay as small as a centimeter square, a new domain of electronics called large-area integrated circuit as large as meters is waiting, which may open up a new continent of applications in the era of ubiquitous electronics. One of the implementations of the large-area electronics is based on organic transistors. The talk will provide perspectives of the organic circuit design taking E-skin, sheet-type scanner and Braille display as examples.

Keynote III
Friday, January 26, 9:00-10:00,
Small Auditorium, 5F
"How Foundry can Help Improve your Bottom-Line? Accuracy Matters!"

Fu-Chieh Hsu
Vice President of Design and
Technology Platform
Taiwan Semiconductor Manufacturing
Company, Taiwan

As the leading edge of technology advances into the nanometer era, process data accuracy becomes increasingly important to the success of product designs. The gap between theoretical benefit and benefit obtainable by designers grows wider with each new technology node. However, foundries and EDA tool vendors can collaborate to reclaim some of the lost benefits of these technology nodes.

In this talk, I will discuss how foundries can contribute in the effort to reclaim lost benefits through better model and data accuracy, while EDA tool vendors contribute through improved design approaches. I will give some examples of TSMC's approaches in improving SPICE model accuracy and DFM accuracy, as well as collaboration with EDA tool vendors in creating our DFM Data Kit. By increasing awareness of TSMC's approach to this issue, I hope to stimulate discussion from all sides of the industry in the search for more solutions.

Technical Program

Wednesday, January 24, 8:30 - 10:00

Wednesday, January 24, 8:30 - 10:00 Small Auditorium, 5F
Opening Session and Keynote Address I

Next-generation Design and EDA Challenges: Small Physics, Big Systems, and Tall Tool-chains
Rob A. Rutenbar — Electrical & Computer Engineering, Carnegie Mellon University, United States

Wednesday, January 24, 10:15 - 12:20

Wednesday, January 24, 10:15 - 12:20 Room 411+412
Session 1A: DFM in Physical Design

Chair(s): ***Ting-Chi Wang*** – National Tsing Hua Univ., Taiwan
Toshiyuki Shibuya – Fujitsu Lab., Japan

1A-1 Model Based Layout Pattern Dependent Metal Filling Algorithm for Improved Chip Surface Uniformity in the Copper Process
Subarna Sinha, Jianfeng Luo, Charles Chiang (Synopsys, United States)

1A-2 Fast and Accurate OPC for Standard-Cell Layouts
David M. Pawlowski (Intel Co., United States), Liang Deng, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, United States)

1A-3 Coupling-aware Dummy Metal Insertion for Lithography
Liang Deng (Univ. of Illinois, Urbana-Champaign, United States), Kaiyuan Chao (Intel Co., United States), Hua Xiang (IBM, United States), Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, United States)

1A-4 Fast Buffer Insertion for Yield Optimization under Process Variations
Ruiming Chen, Hai Zhou (Northwestern Univ., United States)

1A-5 A Global Minimum Clock Distribution Network Augmentation Algorithm for Guaranteed Clock Skew Yield
Bao Liu, Andrew Kahng, Xu Xu (Univ. of California, San Diego, United States), Jiang Hu, Ganesh Venkataraman (Texas A&M Univ., United States)

Wednesday, January 24, 10:15 - 12:20 Room 413
Session 1B: SoC Software Design and Performance Analysis

Chair(s): ***Qiang Zhu*** – Fujitsu Lab., Japan
Youn-Long Steve Lin – National Tsing-Hua Univ., Taiwan

1B-1 Control-Flow Aware Communication and Conflict Analysis of Parallel Processes
Axel Siebenborn, Alexander Viehl, Oliver Bringmann (FZI Forschungszentrum Informatik, Germany), Wolfgang Rosenstiel (Universität Tübingen, Germany)

1B-2 Software Performance Estimation in MPSoC Design
Marcio Oyamada, Flavio Wagner (UFRGS, Brazil), Marius Bonaciu (TIMA Lab., France), Wander Cesario (MnD, France), Ahmed Jerraya (TIMA Lab., France)

1B-3 Effective OpenMP Implementation and Translation for Multiprocessor System-On-Chip without using OS
Woo-Chul Jeun, Soonhoi Ha (Seoul National Univ., Republic of Korea)

1B-4 Creating Explicit Communication in SoC Models Using Interactive Re-Coding
Pramod Chandraiah, Junyu Peng, Rainer Doemer (Univ. of California, Irvine, United States)

1B-5 System Architecture for Software Peripherals
Siddharth Choudhuri, Tony Givargis (Univ. of California, Irvine, United States)

Wednesday, January 24, 10:15 - 12:20 Room 414+415
Session 1C: Advances in High-Frequency and High-Speed Circuit Design and CAD

1C-1 A New Boundary Element Method for Multiple-Frequency Parameter Extraction of Lossy Substrates
Xiren Wang, Wenjian Yu, Zeyi Wang (Tsinghua Univ., China)

1C-2 Variability-Aware Hierarchical Optimization Methodology for Wideband Low Noise Amplifiers
Arthur Nieuwoudt, Tamer Ragheb, Yehia Massoud (Rice Univ., United States)

1C-3 PLLSim - An Ultra Fast Bang-bang Phase Locked Loop Simulation Tool
Michael James Chan, Adam Postula (Univ. of Queensland, Australia), Yong Ding (NanoSilicon Pty Ltd, Australia)

1C-4 A Programmable Fully-Integrated GPS receiver in 0.18ìm CMOS with Test Circuits
Mahta Jenabi, Noshin Riahi, Ali Fotowat-Ahmadi (Unistar Micro Technology Inc., Canada)

1C-5 Ultralow-Power Reconfigurable Computing with Complementary Nano-Electromechanical Carbon Nanotube Switches
Swarup Bhunia, Massood Tabib Azar, Daniel Saab (Case Western Reserve Univ., United States)

Wednesday, January 24, 10:15 - 12:20 Room 416+417
Session 1D: University Design Contest (Short speech)
Wednesday, January 24, 12:20 - 13:30 Room 418
Poster Presentation of University Design Contest

Chair(s): ***Makoto Nagata*** – Kobe Univ., Japan
Fumio Arakawa – Hitachi, Japan

1D-1 A 1Tb/s 3W Inductive-Coupling Transceiver Chip
Noriyuki Miura, Tadahiro Kuroda (Keio Univ., Japan)

1D-2 22-29GHz Ultra-Wideband CMOS Pulse Generator for Collision Avoidance Short Range Vehicular Radar Sensors
Ahmet Oncu, B.B.M. Wasanthamala Badalawa, Tong Wang, Minoru Fujishima (Univ. of Tokyo, Japan)

1D-3 A 2.8-V Multibit Complex Bandpass Delta-Sigma AD Modulator in 0.18μmCMOS
Hao San, Yoshitaka Jingu, Hiroki Wada, Hiroyuki Hagiwara, Akira Hayakawa, Haruo Kobayashi (Gunma Univ., Japan), Masao Hotta (Musashi Inst. of Tech., Japan)

1D-4 A Wideband CMOS LC-VCO Using Variable Inductor
Kazuma Ohashi, Yusaku Ito, Yoshiaki Yoshihara, Kenichi Okada, Kazuya Masu (Tokyo Inst. of Tech., Japan)

1D-5 Design of Active Substrate Noise Canceller using Power Suplly di/dt Detector
Taisuke Kazama, Toru Nakura, Makoto Ikeda, Kunihiro Asada (Univ. of Tokyo, Japan)

1D-6 A 20 Gbps Scalable Load Balanced Birkhoff-von Neumann Symmetric TDM Switch IC with SERDES Interfaces
Yu-Hao Hsu, Min-Sheng Kao, Hou-Cheng Tzeng, Ching-Te Chiu, Jen-Ming Wu (Inst. of Communications Engineering, NTHU, Taiwan), Shuo-Hung Hsu (Inst. of Electronics Engineering, NTHU, Taiwan)

1D-7 Reconfigurable CMOS Low Noise Amplifier Using Variable Bias Circuit for Self Compensation
Satoshi Fukuda, Daisuke Kawazoe, Kenichi Okada, Kazuya Masu (Tokyo Inst. of Tech., Japan)

1D-8 Pseudo-Millimeter-Wave Up-Conversion Mixer with On-Chip Balun for Vehicular Radar Systems
Chee Hong Ivan Lai, Minoru Fujishima (Univ. of Tokyo, Japan)

1D-9 Improving Execution Speed of FPGA using Dynamically Reconfigurable Technique
Roel Pantonial, Md. Ashfaquzzaman Khan, Naoto Miyamoto, Koji Kotani, Shigetoshi Sugawa, Tadahiro Ohmi (Tohoku Univ., Japan)

1D-10 Single-Issue 1500MIPS Embedded DSP with Ultra Compact Codes
Li-Chun Lin, Shih-Hao Ou (National Chiao Tung Univ., Taiwan), Tay-Jyi Lin (Industrial Technology Research Institute, Taiwan), Siang-Sen Deng, Chih-Wei Liu (National Chiao Tung Univ., Taiwan)

1D-11 A Highly Integrated 8 mW H.264/AVC Main Profile Real-time CIF Video Decoder on a 16 MHz SoC Platform
Huan-Kai Peng, Chun-Hsin Lee, Jian-Wen Chen, Tzu-Jen Lo, Yung-Hung Chang, Sheng-Tsung Hsu, Yuan-Chun Lin, Ping Chao, Wei-Cheng Hung, Kai-Yuan Jan (National Tsing Hua Univ., Taiwan)

1D-12 Configurable AMBA On-Chip Real-Time Signal Tracer
Chung-Fu Kao, Chi-Hung Lin, Ing-Jer Huang (National Sun Yat-Sen Univ., Taiwan)

1D-13 Implementation of a Standby-Power-Free CAM Based on Complementary Ferroelectric-Capacitor Logic
Shoun Matsunaga, Takahiro Hanyu (Tohoku Univ., Japan), Hiromitsu Kimura, Takashi Nakamura, Hidemi Takasu (ROHM, Japan)

1D-14 A Multi-Drop Transmission-Line Interconnect in Si LSI
Junki Seita, Hiroyuki Ito, Kenichi Okada, Takashi Sato, Kazuya Masu (Tokyo Inst. of Tech., Japan)

1D-15 A 10GHz/channel On-Chip Signaling Circuit with an Impedance-Unmatched CML Driver in 90nm CMOS Technology
Takeshi Kuboki, Akira Tsuchiya, Hidetoshi Onodera (Kyoto Univ., Japan)

1D-16 A 90nm 8x16 FPGA Enhancing Speed and Yield Utilizing Within-Die Variations
Yuuri Sugihara, Manabu Kotani, Kazuya Katsuki, Kazutoshi Kobayashi, Hidetoshi Onodera (Kyoto Univ., Japan)

1D-17 A 0.35um CMOS 1,632-gate-count Zero-Overhead Dynamic Optically Reconfigurable Gate Array VLSI
Minoru Watanabe, Fuminori Kobayashi (Kyushu Inst. of Tech., Japan)

1D-18 Low-Power High-Speed 180-nm CMOS Clock Drivers
Tadayoshi Enomoto, Suguru Nagayama, Nobuaki Kobayashi (Chuo Univ., Japan)

Wednesday, January 24, 13:30 - 15:35

Wednesday, January 24, 13:30 - 15:35 Room 411+412
Session 2A: New Techniques in Placement

Chair(s): ***Shin'ichi Wakabayashi*** – Hiroshima City Univ., Japan
Hung-Ming Chen – National Chiao Tung Univ., Taiwan

2A-1 Fast Analytic Placement using Minimum Cost Flow
Ameya R Agnihotri, Patrick H Madden (SUNY Binghamton, United States)

2A-2 FastPlace 3.0: A Fast Multilevel Quadratic Placement Algorithm with Placement Congestion Control
Natarajan Viswanathan, Min Pan, Chris Chu (Iowa State Univ., United States)

2A-3 Hippocrates: First-Do-No-Harm Detailed Placement
Haoxing Ren (IBM, United States), David Pan (Univ. of Texas, Austin, United States), Chuck Alpert, Gi-Joon Nam, Paul Villarrubia (IBM, United States)

2A-4 ECO-system: Embracing the Change in Placement
Jarrod Roy, Igor Markov (Univ. of Michigan, United States)

2A-5 Bisection Based Placement for the X Architecture
Satoshi Ono, Patrick H. Madden (SUNY Binghamton CSD, United States)

Wednesday, January 24, 13:30 - 15:35 Room 413
Session 2B: On Chip Communication Methodology

Chair(s): ***Soonhoi Ha*** – Seoul National Univ., Republic of Korea
Nikil Dutt – Univ. of California, Irvine, United States

2B-1 Slack-based Bus Arbitration Scheme for Soft Real-time Constrained Embedded Systems
Minje Jun, Kwanhu Bang (Yonsei Univ., Republic of Korea), Hyuk-Jun Lee (Cisco Systems Incorporated, United States), Naehyuck Chang (Seoul National Univ., Republic of Korea), Eui-Young Chung (Yonsei Univ., Republic of Korea)

2B-2 A Precise Bandwidth Control Arbitration Algorithm for Hard Real-Time SoC Buses
Bu-Ching Lin, Geeng-Wei Lee, Juinn-Dar Huang, Jing-Yang Jou (National Chiao Tung Univ., Taiwan)

2B-3 Communication Architecture Synthesis of Cascaded Bus Matrix
Junhee Yoo, Dongwook Lee (Seoul National Univ., Republic of Korea), Sungjoo Yoo (Samsung Electronics, Republic of Korea), Kiyoung Choi (Seoul National Univ., Republic of Korea)

2B-4 Topology exploration for energy efficient intra-tile communication
Jin Guo, Antonis Papanikolaou, Francky Catthoor (IMEC, Belgium)

2B-5 Application Specific Network-on-Chip Design with Guaranteed Quality Approximation Algorithms
Krishnan Srinivasan, Karam S. Chatha, Goran Konjevod (Arizona State Univ., United States)

Wednesday, January 24, 13:30 - 15:35 Room 414+415

Session 2C: Analog CAD Techniques: From Analysis to Verification

2C-1 Thermal-driven symmetry constraint for analog layout with CBL representation
Jiayi Liu, Sheqin Dong, Yunchun Ma, Di Long, Xianlong Hong (Tsinghua Univ., China)

2C-2 A Graph Reduction Approach to Symbolic Circuit Analysis
Guoyong Shi, Weiwei Chen (Shanghai Jiao Tong Univ., China), C.-J. Richard Shi (Univ. of Washington, United States)

2C-3 Robust Analog Circuit Sizing Using Ellipsoid Method and Affine Arithmetic
Xuexin Liu, Wai-Shing Luk, Yu Song (Fudan Univ., China)

2C-4 WCOMP: Waveform Comparison Tool for Mixed-signal Validation
Peng Zhang, Luk Waishing, Yu Song, Pushan Tang, Xuan Zeng (Fudan Univ., China)

2C-5 Structured Placement with Topological Regularity Evaluation
Shigetoshi Nakatake (Univ. of Kitakyushu, Japan)

Wednesday, January 24, 13:30 - 15:35 Room 416+417

Session 2D: SPECIAL SESSION: Design for Manufacturability

Chair(s): ***Keh-Jeng Chang*** – National Tsing Hua Univ., Taiwan

2D-1 Modeling Sub-90nm On-chip Variation for DFM
Kelvin Doong (TSMC, Taiwan)

2D-2 DFM Reality in Sub-nanometer IC Design
Nishath Verghese (Clear Shape, United States)

2D-3 DFM/DFY Practices during Physical Designs for Timing, Signal Integrity, and Power
Jiing-Yuan Lin (Global Unichip, Taiwan)

2D-4 Advanced Academic Researches Pertinent to DFM
Ting-Chi Wang (NTHU, Taiwan)

2D-5 Panel Discussion
Moderator: Keh-Jeng Chang (NTHU, Taiwan)
Panelists: Kelvin Doong (TSMC, Taiwan)
Nishath Verghese (Clear Shape, United States)
Jiing-Yuan Lin (Global Unichip, Taiwan)
Ting-Chi Wang (NTHU, Taiwan)
Andrew Kahng (Blaze DFM, United States)

Wednesday, January 24, 16:00 - 18:05

Wednesday, January 24, 16:00 - 18:05 Room 411+412

Session 3A: Routing

Chair(s): ***Martin Wong*** – Univ. of Illinois, Urbana-Champaign, United States
Youichi Shiraishi – Gunma Univ., Japan

3A-1 A Novel Performance-Driven Topology Design Algorithm
Min Pan, Chris Chu (Iowa State Univ., United States), Priyadarsan Patra (Intel Co., United States)

3A-2 FastRoute 2.0: A High-quality and Efficient Global Router
Min Pan, Chris Chu (Iowa State Univ., United States)

3A-3 DpRouter: A Fast and Accurate Dynamic-Pattern-Based Global Routing Algorithm
Zhen Cao, Tong Jing (Tsinghua Univ., China), Jinjun Xiong, Yu Hu, Lei He (Univ. of California, Los Angeles, United States), Xianlong Hong (Tsinghua Univ., China)

3A-4 A Fast and Stable Algorithm for Obstacle-Avoiding Rectilinear Steiner Minimal Tree Construction
Pei-Ci Wu, Jhih-Rong Gao, Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

3A-5 A Theoretical Study on Wire Length Estimation Algorithms for Placement with Opaque Blocks
Tan Yan, Shuting Li, Yasuhiro Takashima, Hiroshi Murata (Univ. of Kitakyushu, Japan)

Wednesday, January 24, 16:00 - 18:05 Room 413

Session 3B: System Synthesis and Optimization Techniques

Chair(s): ***Ren-Song Tsay*** – National Tsing Hua Univ., Taiwan
Ahmed Jerraya – TIMA, France

3B-1 LEAF: A System Level Leakage-Aware Floorplanner for SoCs
Aseem Gupta, Nikil Dutt, Fadi Kurdahi (Univ. of California, Irvine, United States), Kamal Khouri, Magdy Abadir (Freescale Semiconductor Inc., United States)

3B-2 Protocol Transducer Synthesis using Divide and Conquer approach
Shota Watanabe, Kenshu Seto, Yuji Ishikawa, Satoshi Komatsu, Masahiro Fujita (Univ. of Tokyo, Japan)

3B-3 A Processor Generation Method from Instruction Behavior Description Based on Specification of Pipeline Stages and Functional Units
Takeshi Shiro, Masaaki Abe, Keishi Sakanushi, Yoshinori Takeuchi, Masaharu Imai (Osaka Univ., Japan)

3B-4 Power and Memory Bandwidth Reduction of an H.264/AVC HDTV Decoder LSI with Elastic Pipeline Architecture
Kentaro Kawakami, Mitsuhiko Kuroda, Hiroshi Kawaguchi, Masahiko Yoshimoto (Kobe Univ., Japan)

3B-5 Architectural Optimizations for Text to Speech Synthesis in Embedded Systems
Soumyajit Dey, Monu Kedia, Anupam Basu (Indian Inst. of Tech. Kharagpur, India)

Wednesday, January 24, 16:00 - 18:05 Room 414+415

Session 3C: Model Checking and Applications to Digital and Analog Circuits

Chair(s): ***Igor Markov*** – Univ. of Michigan, United States
Shin'ichi Minato – Hokkaido Univ., Japan

3C-1 Deeper Bound in BMC by Combining Constant Propagation and Abstraction
Roy Armoni (-, Israel), Limor Fix (Intel, United States), Ranan Fraer (Intel, Israel), Tamir Heyman (Carnegie Mellon Univ., United States), Moshe Vardi (Rich Univ., United States), Yakir Vizel, Yael Zbar (Intel, Israel)

3C-2 Efficient BMC for Multi-Clock Systems with Clocked Specifications
Malay K Ganai, Aarti Gupta (NEC, United States)

3C-3 Symbolic Model Checking of Analog/Mixed-Signal Circuits
David Walter, Scott Little, Nicholas Seegmiller, Chris Myers (Univ. of Utah, United States), Tomohiro Yoneda (National Institute of Informatics, Japan)

3C-4 Efficient Automata-Based Assertion-Checker Synthesis of SEREs for Hardware Emulation
Marc Boule, Zeljko Zilic (McGill Univ., Canada)

Wednesday, January 24, 16:00 - 18:05 Room 416+417
Session 3D: SPECIAL SESSION: Embedded Software for Multiprocessor Systems-on-Chip

Chair(s): ***Hiroyuki Tomiyama*** – Nagoya Univ., Japan

3D-1 Model-based Framework of Embedded Software Design for MPSoC
Soonhoi Ha (SNU, Korea)

3D-2 RTOS and Codesign Toolkit for Multiprocessor Systems-on-chip
Shinya Honda (Nagoya Univ., Japan)

3D-3 Energy-efficient Real-time Task Scheduling in Multiprocessor DVS Systems
Jian-Jia Chen (National Taiwan Univ., Taiwan)

3D-4 Towards Scalable and Secure Execution Platform for Embedded Systems
Junji Sakai (NEC, Japan)

Thursday, January 25, 9:00 - 10:00

Thursday, January 25, 9:00 - 10:00 Small Auditorium, 5F
Keynote Address II

Meeting with the Forthcoming IC Design — The Era of Power, Variability and NRE Explosion and a Bit of the Future —

Takayasu Sakurai — Center for Collaborative Research, and Institute of Industrial Science, University of Tokyo, Japan

Thursday, January 25, 10:15 - 12:20

Thursday, January 25, 10:15 - 12:20 Room 411+412
Session 4A: Model Order Reduction and Macromodeling

Chair(s): ***Sheldon Tan*** – Univ. of California, Riverside, United States
Yehia Massoud – Rice Univ., United States

4A-1 Passive Interconnect Macromodeling Via Balanced Truncation of Linear Systems in Descriptor Form
Boyuan Yan, Sheldon X.-D. Tan, Pu Liu (Univ. of California, Riverside, United States), Bruce McGaughy (Cadence Design Systems Inc., United States)

4A-2 Automated Extraction of Accurate Delay/Timing Macromodels of Digital Gates and Latches using Trajectory Piecewise Methods
Sandeep Dabas, Ning Dong, Jaijeet Roychowdhury (Univ. of Minnesota, Twin Cities, United States)

4A-3 Practical Implementation of Stochastic Parameterized Model Order Reduction via Hermite Polynomial Chaos
Yi Zou, Yici Cai, Qiang Zhou, Xianlong Hong (Tsinghua Univ., China), Sheldon X.D-Tan (Univ. of California, Riverside, United States), Le Kang (Tsinghua Univ., China)

4A-4 Reduced-Order Wide-Band Interconnect Model Realization using Filter-Based Spline Interpolation
Arthur Nieuwoudt, Mehboob Alam, Yehia Massoud (Rice Univ., United States)

4A-5 A Frequency Selective Passivity Preserving Model Order Reduction for RLC Interconnect
Mehboob Alam, Arthur Nieuwoudt, Yehia Massoud (Rice Univ., United States)

Thursday, January 25, 10:15 - 12:20 Room 413
Session 4B: System Level Modeling

Chair(s): ***Tei-Wei Kuo*** – National Taiwan Univ., Taiwan
Shinya Honda – Nagoya Univ., Japan

4B-1 Abstract, Multifaceted Modeling of Embedded Processors for System Level Design
Gunar Schirner, Andreas Gerstlauer, Rainer Doemer (Univ. of California, Irvine, United States)

4B-2 Flexible and Executable Hardware/Software Interface Modeling for Multiprocessor SoC Design Using SystemC
Patrice Gerin, Hao Shen, Alexandre Chureau, Aimen Bouchhima, Ahmed Amine Jerraya (TIMA Laboratory, France)

4B-3 A Retargetable Software Timing Analyzer Using Architecture Description Language
Xianfeng Li (Peking Univ., China), Abhik Roychoudhury, Tulika Mitra (National Univeristy of Singapore, Singapore), Prabhat Mishra (Univ. of Florida, United States), Xu Cheng (Peking Univ., China)

Thursday, January 25, 10:15 - 12:20 Room 414+415
Session 4C: Logic Synthesis

Chair(s): ***Deming Chen*** – Univ. of Illinois, Urbana-Champaign, United States
Yutaka Tamiya – Fujitsu Lab., Japan

4C-1 Automating Logic Rectification by Approximate SPFDs
Yu-Shen Yang (Univ. of Toronto, Canada), Subarna Sinha (Synopsys, United States), Andreas Veneris (Univ. of Toronto, Canada), Robert Brayton (Univ. of California, United States)

4C-2 BddCut: Towards Scalable Symbolic Cut Enumeration
Andrew Chaang Ling, Jianwen Zhu (Univ. of Toronto, Canada), Stephen Dean Brown (Altera Toronto Technology Centre, Canada)

4C-3 Node Mergers in the Presence of Don't Cares
Stephen Plaza, Kai-hui Chang, Igor Markov, Valeria Bertacco (Univ. of Michigan, United States)

4C-4 Synthesis of Reversible Sequential Elements
Min-Lung Chuang, Chun-Yao Wang (National Tsing Hua Univ., Taiwan)

4C-5 Recognition of Fanout-free Functions
Tsung-Lin Lee, Chun-Yao Wang (National Tsing Hua Univ., Taiwan)

Thursday, January 25, 10:15 - 12:20 Room 416+417
Session 4D: SPECIAL SESSION: EDA Challenges for Analog/RF

Chair(s): ***Georges Gielen*** – Katholieke Universiteit Leuven, Belgium

Thursday, January 25, 13:30 - 15:35

Thursday, January 25, 13:30 - 15:35 Room 411+412
Session 5A: Statistical Interconnect Modeling and Analysis

Chair(s): ***Hideki Asai*** – Shizuoka Univ., Japan
Weiping Shi – Texas A&M Univ., United States

5A-1 A New Methodology for Interconnect Parasitics Extraction Considering Photo-Lithography Effects
Ying Zhou (Texas A&M Univ., United States), Zhuo Li (Pextra Corp., United States), Yuxin Tian, Weiping Shi (Texas A&M Univ., United States), Frank Liu (IBM, United States)

5A-2 Simple and Accurate Models for Capacitance Increment due to Metal Fill Insertion
Youngmin Kim (Univ. of Michigan of Ann Arbor, United States), Dusan Petranovic (Mentor Graphics, United States), Dennis Sylvester (Univ. of Michigan of Ann Arbor, United States)

5A-3 New Block-based Statistical Timing Analysis Approaches without Moment Matching
Ruiming Chen, Hai Zhou (Northwestern Univ., United States)

5A-4 Parameter Reduction for Variability Analysis by Slice Inverse Regression (SIR) Method
Alexandar Mitev, Michael Marefact, Dongsheng Ma, Janet Wang (Univ. of Arizona, Tucson, United States)

5A-5 Stochastic Sparse-grid Collocation Algorithm (SSCA) for Periodic Steady-State Analysis of Nonlinear System with Process Variations
Jun Tao, Xuan Zeng (Fudan Univ., China), Wei Cai (Univ. of North Carolina, Charlotte, United States), Dian Zhou (Univ. of Texas, Dallas, United States), Charles Chiang (Synopsys Inc., United States)

Thursday, January 25, 13:30 - 15:35 Room 413
Session 5B: Optimization Issues in Embedded Systems

Chair(s): ***Pai Chou*** – Univ. of California, Irvine, United States
Maziar Goudarzi – Kyushu Univ., Japan

5B-1 Retiming for Synchronous Data Flow Graphs
Nikolaos Liveris, Chuan Lin, Jia Wang, Hai Zhou (Northwestern Univ., United States), Prithviraj Banerjee (Univ. of Illinois, Chicago, United States)

5B-2 Signal-to-Memory Mapping Analysis for Multimedia Signal Processing
Ilie I. Luican, Hongwei Zhu, Florin Balasa (Univ. of Illinois, Chicago, United States)

5B-3 MODLEX: Multi Objective Data Layout Exploration for Embedded Systems on Chip
Rajesh Kumar Srinivasa (Texas Instruments India, India), Govindarajan R (Indian Institute of Science, India), Ravikumar C P (Texas Instruments, India)

5B-4 A Run-Time Memory Protection Methodology
Nagaraju Bussa (Philips Research, India), Udaya Seshua (Philips Semiconductors, India), Bart Vermeulen (Philips Research, Netherlands)

5B-5 Short-Circuit Compiler Transformation: Optimizing Conditional Blocks
Mohammad Ali Ghodrat, Tony Givargis, Alex Nicolau (Univ. of California, Irvine, United States)

Thursday, January 25, 13:30 - 15:35 Room 414+415
Session 5C: High-Level Synthesis

Chair(s): ***Ki-seok Chung*** – Hanyang Univ., Republic of Korea
Katsuharu Suzuki – NEC, Japan

5C-1 Optimization of Arithmetic Datapaths with Finite Word-Length Operands
Sivaram Gopalakrishnan, Priyank Kalla (Univ. of Utah, United States), Florian Enescu (Georgia State Univ., United States)

5C-2 Exploiting Power-Area Tradeoffs in Behavioural Synthesis through clock and operations throughput selection
Marco A. Ochoa-Montiel (Univ. of Southampton, Great Britain)

5C-3 A Parameterized Architecture Model in High Level Synthesis for Image Processing Applications
Yazhuo Dong, Yong Dou (National Univ. of Defense Technology, China)

5C-4 High-Level Power Estimation and Low-Power Design Space Exploration for FPGAs
Deming Chen (Univ. of Illinois, Urbana-Champaign, United States), Jason Cong, Yiping Fan, Zhiru Zhang (Univ. of California, Los Angeles, United States)

5C-5 Numerical Function Generators Using Edge-Valued Binary Decision Diagrams
Shinobu Nagayama (Hiroshima City Univ., Japan), Tsutomu Sasao (Kyushu Inst. of Tech., Japan), Jon Butler (Naval Postgraduate School, United States)

Thursday, January 25, 13:30 - 15:35 Small Auditorium, 5F
Session 5D: Designers' Forum Panel : Presilicon SoC HW/SW Verification

Organizer: ***Tetsuji Sumioka*** – Sony, Japan
Moderator: ***Tetsuji Sumioka*** – Sony, Japan
Panelists: ***Jason Andrews*** – Cadence, United States
Graham Hellestrand – VaST Systems Technology, United States
Hidefumi Kurokawa – NEC Electronics, Japan
Ilya Klebanov – ATI Technologies, United States
Seiji Koino – Toshiba, Japan

Thursday, January 25, 16:00 - 18:05

Thursday, January 25, 16:00 - 18:05 Room 411+412
Session 6A: Timing Modeling and Optimization

Chair(s): ***Masanori Hashimoto*** – Osaka Univ., Japan
Charlie Chung-Ping Chen – National Taiwan Univ., Taiwan

6A-1 Clock Skew Scheduling with Delay Padding for Prescribed Skew Domains
Chuan Lin (Magma Design Automation Inc., United States), Hai Zhou (Northwestern Univ., United States)

6A-2 An Efficient Computation of Statistically Critical Sequential Paths Under Retiming
Mongkol Ekpanyapong (Intel Co., United States), Xin Zhao, Sung Kyu Lim (Georgia Inst. of Tech., United States)

6A-3 Fast Electrical Correction Using Resizing and Buffering
Shrirang Karandikar, Chuck Alpert, Mehmet Yildiz, Paul Villarrubia, Steve Quay, Tuhin Mahmud (IBM, United States)

6A-4 SmartSmooth: A linear time convexity preserving smoothing algorithm for numerically convex data with application to VLSI design
Sanghamitra Roy (Univ. of Wisconsin-Madison, United States), Charlie Chung-Ping Chen (National Taiwan Univ., Taiwan)

6A-5 Modeling the Overshooting Effect for CMOS Inverter in Nanometer Technologies
Zhangcai Huang, Hong Yu (Waseda Univ., Japan), Atsushi Kurokawa (Sanyo Company, Japan), Yasuaki Inoue (Waseda Univ., Japan)

Thursday, January 25, 16:00 - 18:05 Room 413
Session 6B: Application Examples with Leading Edge Design Methodology

Chair(s): ***Ing-Jer Huang*** – National Sun-Yat-Sen Univ., Taiwan
Takeshi Ikenaga – Waseda Univ., Japan

6B-1 Flow-Through-Queue based Power Management for Gigabit Ethernet Controller
Hwisung Jung (Univ. of Southern California, United States), Andy Hwang (Broadcom Corp., United States), Massoud Pedram (Univ. of Southern California, United States)

6B-2 Application Throughput Maximization on Network Processor Architectures
Chris Ostler, Karam S. Chatha, Goran Konjevod (Arizona State Univ., United States)

6B-3 Implementation of a Real Time Programmable Encoder for Low Density Parity Check Code on a Reconfigurable Instruction Cell Architecture (RICA)
Zahid Khan, Tughrul Arslan (Univ. of Edinburgh, Great Britain)

6B-4 VLSI Design of Multi Standard Turbo Decoder for 3G and Beyond
Imran Ahmed, Tughrul Arslan (Univ. of Edinburgh, Great Britain)

6B-5 A High-Throughput Low-Power AES Cipher for Network Applications
Shin-Yi Lin, Chih-Tsun Huang (National Tsing Hua Univ., Taiwan)

Thursday, January 25, 16:00 - 18:05 Room 414+415
Session 6C: Module/Circuit Synthesis

Chair(s): ***Shinji Kimura*** – Waseda Univ., Japan
Chun-Yao Wang – National Tsing Hua Univ., Taiwan

6C-1 Improving XOR-Dominated Circuits by Exploiting Dependencies between Operands
Ajay K. Verma, Paolo Ienne (Ecole Polytechnique Federale de Lausanne, Switzerland)

6C-2 Optimum Prefix Adders in a Comprehensive Area, Timing and Power Design Space
Jianhua Liu, Yi Zhu, Haikun Zhu (Univ. of California, San Diego, United States), John Lillis (Univ. of Illinois, Chicago, United States), Chung-Kuan Cheng (Univ. of California, San Diego, United States)

6C-3 An Interconnect-Centric Approach to Cyclic Shifter Design Using Fanout Splitting and Cell Order Optimization
Haikun Zhu, Yi Zhu, Chung-Kuan Cheng (Univ. of California, San Diego, United States)

6C-4 Optimization of Robust Asynchronous Circuits by Local Input Completeness Relaxation
Cheoljoo Jeong, Steven M. Nowick (Columbia Univ., United States)

6C-5 Safe Delay Optimization for Physical Synthesis
Kai-hui Chang, Igor L. Markov, Valeria Bertacco (Univ. of Michigan at Ann Arbor, United States)

Thursday, January 25, 16:00 - 17:50 Small Auditorium, 5F
Session 6D: Designers' Forum: Low-power SoC Technologies

Chair(s): ***Haruyuki Tago*** – Toshiba, Japan
Kazutoshi Kobayashi – Kyoto Univ., Japan

6D-1 The Development of Low-power and Real-time VC-1/H.264/MPEG4 Video Processing Hardware
Masaru Hase (Renesas Technology, Japan)

6D-2 Development of Low Power ISDB-T One-segment Decoder by Mobile Multi-media Engine SoC (S1G)
Koichi Mori, Masakazu Suzuki, Yasuo Ohara, Satoru Matsuo, Atsushi Asano (Toshiba, Japan)

6D-3 Low Power Techniques for Mobile Application SoCs based on Integrated Platform "UniPhier"
Masaitsu Nakajima, Takao Yamamoto, Masayuki Yamasaki, Masaya Sumita (Matsushita Electric Industrial, Japan)

Friday, January 26, 9:00 - 10:00

Friday, January 26, 9:00 - 10:00 Small Auditorium, 5F
Keynote Address III

How Foundry can Help Improve your Bottom-line? Accuracy Matters!
Fu-Chieh Hsu — Vice President of Design and Technology Platform, Taiwan Semiconductor Manufacturing Company, Taiwan

Friday, January 26, 10:15 - 12:20

Friday, January 26, 10:15 - 12:20 Room 411+412
Session 7A: Advanced Methods for Leakage Reduction

Chair(s): ***Hongliang Chang*** – Cadence, United States

7A-1 Simultaneous Control of Subthreshold and Gate Leakage Current in Nanometer-Scale CMOS Circuits
Youngsoo Shin, Sewan Heo, Hyung-Ock Kim (KAIST, Republic of Korea), Jung Yun Choi (Samsung Electronics, Republic of Korea)

7A-2 Runtime leakage power estimation technique for combinational circuits
Yu-Shiang Lin, Dennis Sylvester (Univ. of Michigan, United States)

7A-3 Logic and Layout Aware Voltage Island Generation for Low Power Design
Liangpeng Guo, Yici Cai, Qiang Zhou, Xianlong Hong (Tsinghua Univ., China)

7A-4 A Fast Probability-Based Algorithm for Leakage Current Reduction Considering Controller Cost
Tsung-Yi Wu (National Changhua Univ. of Education, Taiwan)

7A-5 A Timing-Driven Algorithm for Leakage Reduction in MTCMOS FPGAs
Hassan Hassan, Mohab Anis, Mohamed Elmasry (Univ. of Waterloo, Canada)

Friday, January 26, 10:15 - 12:20 Room 413

Session 7B: Uncertainty Aware Interconnect Design

Chair(s): ***Chih-Tsun Huang*** – National Tsing Hua Univ., Taiwan
Takashi Sato – Tokyo Inst. of Tech., Japan

7B-1 Approaching Speed-of-light Distortionless Communication for On-chip Interconnect
Haikun Zhu, Rui Shi (Univ. of California, San Diego, United States), Hongyu Chen (Synopsys Inc., United States), Chung-Kuan Cheng (Univ. of California, San Diego, United States)

7B-2 Delay Uncertainty Reduction by Gate-Interconnect Splitting
Vineet Agarwal, Jin Sun, Alexandar Mitev, Janet Wang (Univ. of Arizona, Tucson, United States)

7B-3 Transition Skew Coding: A Power and Area Efficient Encoding Technique for Global On-Chip Interconnects
Charbel Akl, Magdy Bayoumi (Univ. of Louisiana, Lafayette, United States)

7B-4 Fast Buffered Delay Estimation Considering Process Variations
Tien-Ting Fang, Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

7B-5 Predicting the Performance and Reliability of Carbon Nanotube Bundles for On-Chip Interconnect
Arthur Nieuwoudt, Mosin Mondal, Yehia Massoud (Rice Univ., United States)

Friday, January 26, 10:15 - 12:20 Room 414+415

Session 7C: Test Cost Reduction Techniques

Chair(s): ***Sudhakar M. Reddy*** – Univ. of Iowa, United States
Tomoo Inoue – Hiroshima City Univ., Japan

7C-1 Shelf Packing to the Design and Optimization of A Power-Aware Multi-Frequency Wrapper Architecture for Modular IP Cores
Danella Zhao, Unni Chandran (Univ. of Louisiana, Lafayette, United States), Hideo Fujiwara (NAIST, Japan)

7C-2 Core-Based Testing of Multiprocessor System-on-Chips Utilizing Hierarchical Functional Buses
Fawnizu Azmadi Hussin, Tomokazu Yoneda (NAIST, Japan), Alex Orailoglu (Univ. of California, San Diego, United States), Hideo Fujiwara (NAIST, Japan)

7C-3 An Architecture for Combined Test Data Compression and Abort-on-Fail Test
Erik Larsson, Jon Persson (Linköpings Universitet, Sweden)

7C-4 RunBasedReordering: A Novel Approach for Test Data Compression and Scan Power
Hao Fang, Chenguang Tong, Xu Cheng (Peking Univ., China)

7C-5 Systematic Scan Reconfiguration
Ahmad Al-Yamani (KFUPM, Saudi Arabia), Narendra Devta-Prasanna (Univ. of Iowa, United States), Arun Gunda (LSI Logic, United States)

Friday, January 26, 10:15 - 12:20 Room 416+417

Session 7D: SPECIAL SESSION: Multi-Processor Platforms for Next Generation Embedded Systems

Organizer: ***Nikil Dutt*** – Univ. of California, Irvine, United States

Panelists: ***Chris Rowen (or substitute)*** – Tensilica, United States
Kazuyuki Hirata – ARM, Japan
Peter Hofstee – IBM, United States
Rudy Lauwereins – IMEC, Belgium
Pierre Paulin – STMicroelectronics, Canada

Friday, January 26, 13:30 - 15:35

Friday, January 26, 13:30 - 15:35 Room 411+412

Session 8A: Advancement in Power Analysis and Optimization

Chair(s): ***Youngsoo Shin*** – KAIST, Republic of Korea
Takayuki Watanabe – Univ. of Shizuoka, Japan

8A-1 Fast Decoupling Capacitor Budgeting for Power/Ground Network Using Random Walk Approach
Le Kang, Yici Cai, Yi Zou, Jin Shi, Xianlong Hong (Tsinghua Univ., China), Sheldon X.-D. Tan (Univ. of California, Riverside, United States)

8A-2 Timing-Aware Decoupling Capacitance Allocation in Power Distribution Networks
Sanjay Pant, David Blaauw (Univ. of Michigan, United States)

8A-3 Fast Placement Optimization of Power Supply Pads
Yu Zhong, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, United States)

8A-4 Efficient Second-Order Iterative Methods for IR Drop Analysis in Large Power Grid
Yu Zhong, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, United States)

8A-5 A Current-based Method for Short Circuit Power Calculation under Noisy Input Waveforms
Hanif Fatemi, Shahin Nazarian, Massoud Pedram (Univ. of Southern California, United States)

Friday, January 26, 13:30 - 15:35 Room 413

Session 8B: Electrical Optimization in Floorplanning/Placement

Chair(s): ***Shigetoshi Nakatake*** – Univ. of Kitakyushu, Japan
David Pan – Univ. of Texas, Austin, United States

8B-1 Thermal-Aware 3D IC Placement Via Transformation
Jason Cong, Guojie Luo, Jie Wei, Yan Zhang (Univ. of California, Los Angeles, United States)

8B-2 Noise-Direct: A Technique for Power Supply Noise Aware Floorplanning Using Microarchitecture Profiling
Fayez Mohamood, Michael Healy, Sung Kyu Lim, Hsien-Hsin S. Lee (Georgia Tech, United States)

8B-3 On Increasing Signal Integrity with Minimal Decap Insertion in Area-Array SoC Floorplan Design
Chao-Hung Lu (National Central Univ., Taiwan), Hung-Ming Chen (National Chiao Tung Univ., Taiwan), Chien-Nan Jimmy Liu (National Central Univ., Taiwan)

8B-4 Voltage Island Generation under Performance Requirement for SoC Designs
Wai-Kei Mak, Jr-Wei Chen (National Tsing Hua Univ., Taiwan)

8B-5 Fast Flip-Chip Pin-Out Designation Respin by Pin-Block Design and Floorplanning for Package-Board Codesign
Ren-Jie Lee, Ming-Fang Lai, Hung-Ming Chen (National Chiao Tung Univ., Taiwan)

Friday, January 26, 13:30 - 15:35 Room 414+415

Session 8C: Advances in Test and Diagnosis

Chair(s): ***Erik Larsson*** – Royal Inst. of Tech., Sweden
Xiaoging Wen – Kyushu Inst. of Tech., Japan

8C-1 A Technique to Reduce Peak Current and Average Power Dissipation in Scan Designs by Limited Capture
Seongmoon Wang, Wenlong Wei (NEC, United States)

8C-2 Warning: Launch off Shift Tests for Delay Faults May Contribute to Test Escapes
Zhuo Zhang, Sudhakar Reddy (Univ. of Iowa, United States), Irith Pomeranz (Purdue Univ., United States)

8C-3 A Wafer-Level Defect Screening Technique to Reduce Test and Packaging Costs for "Big-D/Small-A" Mixed-Signal SoCs
Sudarshan Bahukudumbi, Sule Ozev, Krishnendu Chakrabarty (Duke Univ., United States), Vikram Iyengar (IBM, United States)

8C-4 Fault Dictionary Size Reduction for Million-Gate Large Circuits
Yu-Ru Hong, Juinn-Dar Huang (National Chiao Tung Univ., Taiwan)

8C-5 Cyclic-CPRS : A Diagnosis Technique for BISTed Circuits for Nano-meter Technologies
Chun-Yi Lee, Hung-Mao Lin, Fang-Min Wang, James Chien-Mo Li (National Taiwan Univ., Taiwan)

Friday, January 26, 13:30 - 15:35 Small Auditorium, 5F

Session 8D: Designers' Forum: High-speed Chip to Chip Signaling Solutions

Chair(s): ***Haruyuki Tago*** – Toshiba, Japan
Kazutoshi Kobayashi – Kyoto Univ., Japan

8D-1 Preferable Improvements and Changes to FB-DiMM High-speed Channel for 9.6Gbps Operation
Atsushi Hiraishi, Toshio Sugano (Elpida Memory, Japan), Hideki Kusamitsu (Yamaichi Electronics)

8D-2 Xbox360 Front Side Bus - A 21.6 G B/s End to End Interface Design
David Siljenberg, Steve Baumgartner, Tim Buchholtz, Mark Maxson (IBM, United States)

8D-3 High-speed Signaling Technology for Servers
Jian Hong Jiang (Fujitsu Laboratories of America, United States)

8D-4 System Co-design and Analysis Approach to Implementing the XDR Memory System of the Cell Processor Realizing 3.2 Gbps in Low Cost, High Volume Production
Wai-Yeung Yip, Scott Best, Wendemagegnehu Beyene, Ralf Schmitt (Rambus, United States)

Friday, January 26, 16:00 - 18:05

Friday, January 26, 16:00 - 18:05 Room 411+412

Session 9A: Power Efficient Design Techniques

Chair(s): ***Hiroyuki Tomiyama*** – Nagoya Univ., Japan
Gang Zeng – Nagoya Univ., Japan

9A-1 Flow Time Minimization under Energy Constraints
Jian-Jia Chen (National Taiwan Univ., Taiwan), Kazuo Iwama (Kyoto Univ., Japan), Tei-Wei Kuo, Hseuh-I Lu (National Taiwan Univ., Taiwan)

9A-2 Integrating Power Management into Distributed Real-time Systems at Minimum Implementation Cost
Bita Gorjiara, Nader Bagherzadeh, Pai Chou (Univ. of California, Irvine, United States)

9A-3 A Software Technique to Improve Yield of Processor Chips in Presence of Ultra-Leaky SRAM Cells Caused by Process Variation
Maziar Goudarzi, Tohru Ishihara, Hiroto Yasuura (Kyushu Univ., Japan)

9A-4 Program Phase Directed Dynamic Cache Way Reconfiguration for Power Efficiency
Subhasis Banerjee, Surendra G, S. K. Nandy (Indian Institute of Science, India)

9A-5 CLIPPER: Counter-based Low Impact Processor Power Estimation at Run-time
Jorgen Peddersen, Sri Parameswaran (Univ. of New South Wales, Australia)

Friday, January 26, 16:00 - 18:05 Room 413

Session 9B: Leading Edge Design Methodology for Processors

Chair(s): ***Takashi Miyamori*** – Toshiba, Japan

9B-1 Design Methodology for 2.4GHz Dual-Core Microprocessor
Noriyuki Ito, Hiroaki Komatsu, Akira Kanuma, Akihiko Yoshitake, Yoshiyasu Tanamura, Hiroyuki Sugiyama, Ryoichi Yamashita, Ken-ichi Nabeya, Hironobu Yoshino, Hitoshi Yamanaka, Masahiro Yanagida, Yoshitomo Ozeki, Kinya Ishizaka, Takeshi Kono, Yutaka Isoda (Fujitsu Ltd., Japan)

9B-2 An Embedded Low Power/Cost 16-Bit Data/Instruction Microprocessor Compatible with ARM7 Software Tools
Fu-Ching Yang, Ing-Jer Huang (National Sun Yat-Sen Univ., Taiwan)

9B-3 A Novel Reconfigurable Low Power Distributed Arithmetic Architecture for Multimedia Applications
Zhenyu Liu, Tughrul Arslan, Ahmet T. Erdogan (Univ. of Edinburgh, Great Britain)

9B-4 Exploration of Low Power Adders for a SIMD Data Path
Giacomo Paci (Univ. of Bologna, Italy), Paul Marchal (IMEC, Belgium), Luca Benini (Univ. of Bologna, Italy)

9B-5 Micro-architecture Pipelining Optimization with Throughput-Aware Floorplanning
Yuchun Ma, Zhuoyuan Li (Tsinghua Univ., China), Jason Cong (Univ. of California, Los Angeles, United States), Xianlong Hong (Tsinghua Univ., China), Glenn Reinman (Univ. of California, Los Angeles, United States), Sheqin Dong, Qian Zhou (Tsinghua Univ., China)

Friday, January 26, 16:00 - 18:05 Room 414+415

Session 9C: Satisfiability and Applications

Chair(s): ***Jun Sawada*** – IBM, United States
Takashi Takenaka – NEC, Japan

9C-1 Multithreaded SAT Solving
Matthew Lewis, Tobias Schubert, Bernd Becker (Albert-Ludwigs-Univ. of Freiburg, Germany)

9C-2 Trace Compaction using SAT-based Reachability Analysis
Sean Safarpour, Andreas Veneris, Hratch Mangassarian (Univ. of Toronto, Canada)

9C-3 Combinational Equivalence Checking Using Incremental SAT Solving, Output Ordering, and Resets
Stefan Disch, Christoph Scholl (Univ. of Freiburg, Germany)

9C-4 Fixing Design Errors with Counterexamples & Resynthesis
Kai-hui Chang, Igor L. Markov, Valeria Bertacco (Univ. of Michigan at Ann Arbor, United States)

Friday, January 26, 16:00 - 18:05 Small Auditorium, 5F
Session 9D: Designers' Forum Panel: Top 10 Design Issues

Organizer: ***Haruyuki Tago*** – Toshiba, Japan
Moderator: ***Peter Hofstee*** – IBM, United States
Panelists: TBD

Tutorials

Tutorial 1 (FULL DAY)
Tuesday, January 23, 9:30–17:00 Room 411+412
DFM Tools, Methodologies and Practice at 65nm and Beyond

Organizer: ***Andrew B. Kahng*** – Univ. of California, San Diego, United States

Speakers: ***N. S. Nagaraj*** – Texas Instruments, United States
Jean-Pierre Schoellkopf – STMicroelectronics, France
Mike Smayling – Applied Materials, United States
Ban P. Wong – Charterd Semiconductor, United States
Andrew B. Kahng – Univ. of California, San Diego, United States

Entering the 65nm node, today's DFM tools attempt to satisfy several basic objectives. To address the failure of "WYSIWYG" in sub-100nm process nodes, "shape" (x-y dimension) and "thickness" (z dimension) simulation technologies are being deployed. To address "uncontrollable variation", statistical analysis technologies (SSTA, statistical extraction, etc.) are being investigated. And, well-established internal technologies for defect-oriented yield analysis (critical area, pattern hotspot finding) and optimization (via/contact doubling, wire spreading, etc.) are being commoditized. The order of tool deployment has been as one would expect: (1) geometric criteria (through process window hot-spots, etc.) before electrical criteria (leakage, timing variation, etc.); (2) library and IP development use models before full-chip use models; and (3) analyses before optimizations.

How are such technologies applied to ensure the fastest library and RET development, the fastest process ramps, the highest yields? This tutorial will discuss DFM technologies and methodologies that provide high-ROI bridges between designers and the manufacturing process.

Part 1: Interactions between layout and manufacturability for devices

Part 2: Interactions between layout and manufacturability for interconnects

Part 3: Design of test structures and test chips to characterize FEOL and BEOL variability, and use of in-line metrology to inform modeling and cycles of yield learning

Part 4: Current DFM tools and methodologies, along with opportunities for improved DFM deployment

Part 5: New tools and futures

Tutorial 2 (FULL DAY)
Tuesday, January 23, 9:30–17:00 Room 413
Functional Verification Planning and Management — The Road to Verification Closure is Paved with Good Intentions

Organizers: ***Andrew Piziali*** – Cadence, United States
Avi Ziv – IBM, Islael

Speakers: ***Andrew Piziali*** – Cadence, United States
Avi Ziv – IBM, Islael

This tutorial teaches the student state-of-the-art techniques and methodologies that are used in the industry today for planning, monitoring and assessing verification progress. Planning, monitoring and assessment of the verification process are essential for predictable, successful verification. Quantifying the scope of the verification problem, specifying its solution and measuring verification progress against this plan dramatically reduces schedule uncertainty and provides an adaptive framework for accommodating design and schedule changes. This planning process provides the information necessary to predict the state of the verification process for risk analysis and management. Overall, good planning, monitoring and assessment prevent late schedule and quality surprises.

Tutorial 3 (HALF DAY)
Tuesday, January 23, 9:30–12:30 Room 414+415
Low Power CMOS Design:
The Fabrics: Research Front-End

Organizer: ***Tadahiro Kuroda*** – Keio University, Japan

Speakers: ***Hitoshi Wakabayashi*** – Sony, Japan
Tadahiro Kuroda – Keio University, Japan
Ankur Gupta – Cadence, United States
Luca Benini – Bologna University, Italy

This tutorial will cover research front-ends of low power CMOS design, including (1) process and device level, (2) circuit level, (3) EDA level, and (4) system level.

Tutorial 4 (HALF DAY)
Tuesday, January 23, 14:00–17:00 Room 414+415
Low Power CMOS Design:
The Applications: State-of-the-Art Practice

Organizer: ***Tadahiro Kuroda*** – Keio University, Japan
Speakers: ***Toshihiro Hattori*** – Renesas, Japan
Atsuki Inoue – Fujitsu Laboratory, Japan
Masaya Sumita – Panasonic, Japan
Mototsugu Hamada – Toshiba, Japan

This tutorial will cover state-of-the-art practice of low power CMOS designs in various application fields, including (1) application processors, (2) ASICs, (3) digital consumer products, and (4) wireless communication chips.

Tutorial 5 (HALF DAY)
Tuesday, January 23, 9:30–12:30 Room 416+417
Fast Physical Synthesis for Multi-Million Gate ASIC Designs

Organizer: ***Charles J. Alpert*** – IBM, United States
Speaker: ***Charles J. Alpert*** – IBM, United States

This tutorial presents new physical synthesis techniques that are designed to improve throughput. This tutorial discusses:

- **Placement techniques:** The tutorial discusses new approaches that make placement fast (such as multi-level clustering) and also modern force-directed placement techniques that have recently proven superior for obtaining high quality placements. The tutorial will also discuss the placement of multi-cycle latches.
- **Innovative buffering techniques:** The tutorial discusses new techniques for inserting buffers quickly (compared to traditional van Ginneken) and how to also handle modern routing congestion constraints.
- **Legalization paradigm shift:** This tutorial discusses a technique called diffusion that smoothly spreads out cells to handle these difficult legalization instances.
- **The optimization model:** No matter what kind of change is required, whether synthesis, repowering or buffering is required, the tool needs a mechanism to evaluate the change and then either accept or reject the solution, via an incremental static timing analysis tool. The tutorial will briefly cover this optimization model.

- **Putting it all together:** All the pieces still need to be assemble into a coherent physical synthesis flow. The tutorial presents ways to combine the techniques of electrical correction, critical path optimization, histogram compression, wirelength reduction, and area recovery into a coherent flow that can be used for timing closure. Insights into design techniques and strategies for interacting with physical synthesis flows will also be discussed.

Tutorial 6 (HALF DAY)
Tuesday, January 23, 14:00–17:00 Room 416+417
Concepts and Tools for Practical Embedded System Design

Organizer: ***Nikil Dutt*** – Univ. of California, Irvine, United States
Speakers: ***Daniel Gajski*** – Univ. of California, Irvine, United States
Andreas Gerstlauer – Univ. of California, Irvine, United States
Samar Abdi – Univ. of California, Irvine, United States

The continuous increase in size, complexity and heterogeneity of embedded system (ES) designs has introduced new challenges in their modeling, synthesis and verification. The ES designs of today are being specified and developed at higher levels of abstraction such as transaction level to cope with their complexity. For ES implementation, the application must be mapped to the target platform. The higher level descriptions are then translated to platform aware RTL/C code that can be input to standard SW and EDA tools. All ES design descriptions also need to be verifiable to ensure their consistency and functional correctness.

In this tutorial, we will cover the key concepts and state of the art tools for ES design using industrial strength case studies such as MP3 player design. We will have in-depth presentations on the following topics:

1. Introduction and ES design requirements.
2. ES programming and modeling at specification and transaction levels.
3. Tools for implementation and verification of ES designs for different HW-SW platforms.
4. Tools for synthesis of HW, SW and interfaces from high level ES models.

5. Verification of ES designs using simulation and FPGA prototyping.
6. A roadmap for establishing an ES design science and tool flow.

ASP-DAC 2007 at a Glance

Tuesday, January 23

FULL-DAY Tutorials

TUTORIAL 1	(9:30–17:00)	Room 411+412

DFM Tools, Methodologies and Practice at 65nm and Beyond

TUTORIAL 2	(9:30–17:00)	Room 413

Functional Verification Planning and Management — The Road to Verification Closure is Paved with Good Intentions

HALF-DAY Tutorials

TUTORIAL 3	(9:30–12:30)	Room 414+415

Low Power CMOS Design: The Fabrics: Research Front-End

TUTORIAL 4	(14:00–17:00)	Room 414+415

Low Power CMOS Design: The Applications: State-of-the-Art Practice

TUTORIAL 5	(9:30–12:30)	Room 416+417

Fast Physical Synthesis for Multi-Million Gate ASIC Designs

TUTORIAL 6	(14:00–17:00)	Room 416+417

Concepts and Tools for Practical Embedded System Design

Wednesday, January 24

	A	B	C	D
8:30	**Opening Session & Keynote Address I** (Small Auditorium, 5F)			
10:00	**Break**			
10:15	1A (Room 411+412) DFM in Physical Design	1B (Room 413) SoC Software Design and Performance Analysis	1C (Room 414+415) Advances in High-Frequency and High-Speed Circuit Design and CAD	1D (Room 416+417) University Design Contest
12:20	**Lunch Break / University Design Contest Discussion at ASP-DAC Site (Room 418)**			
13:30	2A (Room 411+412) New Techniques in Placement	2B (Room 413) On Chip Communication Methodology	2C (Room 414+415) Analog CAD Techniques: From Analysis to Verification	2D (Room 416+417) Special Session: Design for Manufacturability
15:35	**Coffee Break (Room 418)**			
16:00	3A (Room 411+412) Routing	3B (Room 413) System Synthesis and Optimization Techniques	3C (Room 414+415) Model Checking and Applications to Digital and Analog Circuits	3D (Room 416+417) Special Session: Embedded Software for Multiprocessor Systems-on-Chip
18:05				

Thursday, January 25

	A	B	C	D
9:00	**Keynote Address II** (Small Auditorium, 5F)			
10:00	**Break**			
10:15	4A (Room 411+412) Model Order Reduction and Macromodeling	4B (Room 413) System Level Modeling	4C (Room 414+415) Logic Synthesis	4D (Room 416+417) Special Session: EDA Challenges for Analog/RF
12:20	**Lunch Break / Student Forum (Room 418)**			
13:30	5A (Room 411+412) Statistical Interconnect Modeling and Analysis	5B (Room 413) Optimization Issues in Embedded Systems	5C (Room 414+415) High-Level Synthesis	5D (Small Auditorium, 5F) Designers' Forum Panel : Presilicon SoC HW/SW Verification
15:35	**Coffee Break (Room 418)**			
16:00	6A (Room 411+412) Timing Modeling and Optimization	6B (Room 413) Application Examples with Leading Edge Design Methodology	6C (Room 414+415) Module/Circuit Synthesis	6D (Small Auditorium, 5F) Designers' Forum: Low-power SoC Technologies
18:05	Banquet 18:30–20:30 (Room 501+502)			

Friday, January 26

	A	B	C	D
9:00		**Keynote Address III** (Small Auditorium, 5F)		
10:00		**Break**		
10:15	7A (Room 411+412) Advanced Methods for Leakage Reduction	7B (Room 413) Uncertainty Aware Interconnect Design	7C (Room 414+415) Test Cost Reduction Techniques	7D (Room 416+417) Special Session: Multi-Processor Platforms for Next Generation Embedded Systems
12:20		**Lunch Break**		
13:30	8A (Room 411+412) Advancement in Power Analysis and Optimization	8B (Room 413) Electrical Optimization in Floorplanning/Placement	8C (Room 414+415) Advances in Test and Diagnosis	8D (Small Auditorium, 5F) Designers' Forum: High-speed Chip to Chip Signaling Solutions
15:35		**Coffee Break (Room 418)**		
16:00	9A (Room 411+412) Power Efficient Design Techniques	9B (Room 413) Leading Edge Design Methodology for Processors	9C (Room 414+415) Satisfiability and Applications	9D (Small Auditorium, 5F) Designers' Forum Panel: Top 10 Design Issues
18:05				

Registration

Conference pre-registration through Web is strongly advised. Please visit the Online Registration page:

http://www.aspdac.com/

If web-based registration is not convenient, pre-registration is possible by filling in and returning the enclosed registration form together with the appropriate fee to the conference secretariat. Registration will be confirmed only upon receipt of the registration fee.

FEES

Category	By Dec. 15, '06	After Dec. 16, '06 and on site
[Conference]		
∗Member	45,000 yen	50,000 yen
Non-member	55,000 yen	60,000 yen
Full-time Student	25,000 yen	30,000 yen
[Designers' Forum]		
∗Member	15,000 yen	20,000 yen
Non-member	15,000 yen	20,000 yen
Full-time Student	15,000 yen	20,000 yen
[Tutorial] (Full-Day or two Half-Days)		
∗Member	29,000 yen	34,000 yen
Non-member	35,000 yen	39,000 yen
Full-time Student	19,000 yen	22,000 yen
[Tutorial] (Half-Day)		
∗Member	20,000 yen	24,000 yen
Non-member	24,000 yen	28,000 yen
Full-time Student	12,000 yen	14,000 yen

∗ **Member of IEEE, ACM SIGDA, IEICE, IPSJ**

The conference fee includes:

- Admission to all sessions (including keynote speeches and designers' forum) without tutorial
- Banquet (excluding Full-time students)
- One refreshment per break
- Congress kit (with a final program, one copy of conference proceedings, and one CDROM of conference proceedings)

The designers' forum fee includes:

- Admission to Keynote Speech and Designers' Forum
- One CDROM of conference proceesings
- One refreshment per break

The tutorial fee includes:

- Admission to full-day or half-day tutorial(s)
- One copy of all tutorial texts
- One lunch coupon
- One refreshment per break

PAYMENT

All registration fees must be paid in Japanese yen by bank remittance or credit card. Please note that personal checks and bank drafts will not be accepted.

Bank Remittance

Please remit the appropriate amount to the following bank account.

Bank Name: **SUMITOMO MITSUI BANKING CORPORATION** (The Mitsui Sumitomo Bank) **Marunouchi Branch**
SWIFT Code:**SMBCJPJT**
Account Title:**ASP-DAC2007 Hidetoshi Onodera**
Account No.: **6583544** (Ordinary)

Credit Card

The following credit cards will be accepted:

VISA, MasterCard, American Express

CANCELLATION AND REFUND

When written notification of cancellation is received by the conference secretariat by December 15, 2006, 5,000 yen will be deducted from the fees paid to cover administrative costs. No refunds will be made for cancellation requests received after this date.

REGISTRATION HOURS

Tuesday,	January 23:	7:30 – 18:00
Wednesday,	January 24:	7:00 – 17:00
Thursday	January 25:	7:30 – 17:00
Friday	January 26:	7:30 – 17:00

Registration Form

ASP-DAC 2007
January 23 – 26, 2007, Yokohama, Japan

Advance Registration Deadline: Dec. 15th, 2006

Web-based registration is recommended. Please visit the Online Registration page (**http://www.aspdac.com/**). If web-based registration is not convenient, please complete this form and make a copy, and send it by post mail or fax it to:

ASP-DAC 2007 SECRETARIAT
Japan Electronics Show Association
Sumitomo Shibadaimon Bldg. 2-gokan,5F
1-12-16, Shibadaimon, Minato-ku, Tokyo, 105-0012 JAPAN
Tel: +81-3-5402-7601 Fax: +81-3-5402-7605
E-mail: aspdac2007@aspdac.com

ASP-DAC 2007 Registration Form

Registrant: ( )Prof. ( )Dr. ( )Mr. ( )Ms. (Please choose one.)
Family name:_____ First name:_____
Other name:_____
Affiliation:_____
Mailstop: _____
Dept./Div.: _____
Mailing address:_____ City:_____
State:_____ Zip:_____ Country:_____
Phone:_____ Fax:_____
E-mail:_____
Membership:
( )IEICE ( )IPSJ ( )ACM SIGDA ( )IEEE ( )Non-member
Member code:_____

Tutorial: (Please choose one Full-Day topic or one/two Half-Day topics. If you choose two Half-Day topics, please choose Morning Tutorial (Tutorial 3 or 5) and Afternoon Tutorial (Tutorial 4 or 6)).

( )Tutorial 1 (Full-Day): DFM Tools, Methodologies and Practice at 65nm and Beyond
( )Tutorial 2 (Full-Day): Functional Verification Planning and Management — The Road to Verification Closure is Paved with Good Intentions
( )Tutorial 3 (Half-Day): Low Power CMOS Design: The Fabrics: Research Front-End
( )Tutorial 4 (Half-Day): Low Power CMOS Design: The Applications: State-of-the-Art Practice
( )Tutorial 5 (Half-Day): Fast Physical Synthesis for Multi-Million Gate ASIC Designs
( )Tutorial 6 (Half-Day): Concepts and Tools for Practical Embedded System Design

Registration Fee & Payment Method

Category	By Dec. 15, '06	After Dec. 16, '06	Total
[Conference]			
Member	45,000 yen	50,000 yen	¥_____
Non-member	55,000 yen	60,000 yen	¥_____
Full-time Student	25,000 yen	30,000 yen	¥_____
[Designers' Forum]			
Member	15,000 yen	20,000 yen	¥_____
Non-member	15,000 yen	20,000 yen	¥_____
Full-time Student	15,000 yen	20,000 yen	¥_____
[Tutorial] (Full-Day or two Half-Days)			
Member	29,000 yen	34,000 yen	¥_____
Non-member	35,000 yen	39,000 yen	¥_____
Full-time Student	19,000 yen	22,000 yen	¥_____
[Tutorial] (Half-Day)			
Member	20,000 yen	24,000 yen	¥_____
Non-member	24,000 yen	28,000 yen	¥_____
Full-time Student	12,000 yen	14,000 yen	¥_____
		Grand Total	¥_____

( ) BANK TRANSFER:

I remitted or will remit a grand total of _____ yen on _____ (date/month/year) through my bank named _____ to the following account:
Name of Bank: **SUMITOMO MITSUI BANKING CORPORATION** (The Mitsui Sumitomo Bank)
Marunouchi Branch
SWIFT Code: **SMBCJPJT**
Account Title: **ASP-DAC2007 Hidetoshi Onodera**
Account No.: **6583544 (Ordinary)**

( ) CREDIT CARD:

( )VISA ( )MasterCard ( )American Express
Amount to be paid: _____ yen
Card No.:_____- _____- _____- _____
Exp. Date: ___/_____(month/year)
Cardholder's name: _____
Authorized Signature:
Date: _____ **Signature:**_____

Invoices and Receipts

Invoice Required? ( )Yes ( ) No

If you replied "Yes," and you would like the invoice to be sent to a different address from that of your registration, please input the address below.

Invoice to (name): _____
Address: _____

Receipt Required? ( )Yes ( ) No

If you replied "Yes," and you would like the receipt to be sent to a different address from that of your registration, please input the address below.

Receipt to (name): _____
Address: _____

Attendee Survey

1) Which category best describes your work? (choose one only)

( ) System or LSI Design
( ) Research and Development of EDA Tools
( ) Design Methodology ( ) Marketing/Sales ( ) Management
( ) Research/Education in an Academic Institution
( ) Student ( ) Other

2) Which area do you primarily work in? (pick all that apply)

( ) System Level ( ) Logic/Behavioral Level ( ) Circuit Level
( ) Layout Level ( ) Process Technology Level
( ) Design ( ) Design Methodology/Tool environment
( ) Synthesis/Optimization ( ) Verification ( ) Test
( ) Embedded System ( ) Low Power
( ) Timing and Signal Integrity ( ) Power Supply and Heat
( ) Analog, RF, Mixed Signal ( ) System-level Integration, SIP
( ) Other

3) What is your primary motivation/interest for attending ASP-DAC? (pick all that apply)

( ) I am a speaker at the conference
( ) I want to learn about EDA in general
( ) I want to learn more about the basics of EDA
( ) I want to learn more about advances in theory
( ) I want to learn more about practical application of EDA
( ) I have interest in Keynote speakers
( ) I have interest in specific technical presentation(s)
( ) I have interest in Special Sessions and Designers' Forum
( ) I have interest in the technical program as a whole
( ) I have interest in networking and social interaction opportunities
( ) Other

4) How did you learn about ASP-DAC? (choose the two most significant factors)

( ) ASP-DAC Web Site ( ) Advance Program Brochure
( ) E-mail ( ) Previous Attendance ( ) Colleague/Advisor
( ) I have paper presentation at the conference ( ) Other

Registration (4/4)
Note:

1. All payments must be in Japanese yen.
2. Bank drafts and personal checks will not be accepted.
3. If paying by credit card, please visit the Online Registration page (**http://www.aspdac.com/**) or send this form by post mail.
4. The remitter's name should be the same as the registrant's name.
5. If paying by bank transfer using your company's name, please advise us of the ID#, registrant's name, and transfer date (the day you transfer the fees) by e-mail to

   aspdac2007@aspdac.com or by Fax at **+81-3-5402-7605.** If you don't advise us above information within a week after you transfer the fee, we can't confirm your payment.
6. Handling fees and other bank transfer fees are to be borne by the registrant.
7. If payment of the registration fee is unremitted, or the credit card charge cannot be authorized, please go to the accounting desk.
8. If registered contents are changed or added, please notify the ASP-DAC 2007 Secretariat by e-mail at

   aspdac2007@aspdac.com or by Fax at **+81-3-5402-7605**. (Please be sure to specify your ID#.)

Information

Proceedings:

ASP-DAC 2007 will be producing two versions of the ASP-DAC 2007 Proceedings; a bound paper version and a CD-ROM version. All papers will be included in both versions. Conference registration in any of the categories will include copies of both versions of the ASP-DAC 2007 Proceedings. Additional Proceedings will be available for purchase at the Conference. Prices are as follows:

Paper Form: ¥5,000; CD-ROM Form: ¥2,000;

Both versions of the proceedings will also be available for purchase after the conference; please contact IEEE for the bound version and ACM SIGDA for the CD-ROM version.

Banquet:

Conference registrants are invited to attend a banquet to be held on January 25, 2007. The banquet will be held from 18:30 to 20:30 at the fifth floor of conference center. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers' Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay ¥5,000 for a ticket when they register on site.

Visa Application:

Without a legal visa, foreign participants may be denied entry into Japan. Please contact your nearest Japanese embassy in order to ensure entry. Notice that the ASP-DAC 2007 Organizing Committee issues the invitation letters and supports the VISA applications only for presenters of the conference papers. All the other attendees have to apply for VISA through their travel agents or by yourself. In some cases it may take two months to obtain a legal visa. The following Web page of Japanese embassy may be helpful.

http://www.mofa.go.jp/j_info/visit/visa/

Insurance:

The organizer cannot accept responsibility for accidents which might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:

The temperature in Yokohama during the period of the Conference ranges between 5°C and 12°C.

Currency Exchange:

Only Japanese Yen(¥) is accepted at ordinary stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can exchange your currency for Japanese Yen at foreign exchange banks and other authorized money exchange offices with your passport.

Electrical Appliances:

Electrical appliances are supplied on 100 volts in Japan. The frequency is 50 Hz in eastern Japan including Tokyo, Yokohama and 60 Hz in western Japan including Kyoto and Osaka.

Shopping:

The business hours of most department stores are from 10:00 to 20:00. They are open on Sundays and national holidays, but may close on some weekday. Business hours of retail shops differ from one another, but most shops operate from 10:00 to 20:00. Shops are open on Sundays and national holidays.

Sightseeing:

http://www.city.yokohama.jp/ne/info/hotspotE.html

Participants can get sightseeing information at the JTB Travel desk in the Conference site during the Conference period.

Yokohama Bay Sightseeing Cruise

You can ride a cruise boat at Yamashita Park sightseeing Boat Terminal, Minato Mirai Pukarisanbashi Pier (MM21), etc. For more information, reference the home page at:
http://www.welcome.city.yokohama.jp/eng/tourism/walking/1070.html

CHINA TOWN

Being the largest Chinese settlement in Japan, Chinatown is always alive with people who come to enjoy Chinese food. It is also a fun place for shopping or just walking around its many streets and alleys lined with colorful restaurants, shops overflowing with Chinese goods and stores that sell exotic ingredients and Chinese medicines.

LANDMARK TOWER

296 meters high with 70 stories above ground and three levels underground. It is Japan's tallest skyscraper. A 40-second ride on the world's fastest elevator skyrockets you to the 69th floor's Sky Garden, the highest observatory in Japan.

Hours: 10:00-21:00 Admission: ¥1,000
Access: 7min. walk from Sakuragicho station

SANKEIEN GARDEN

A purely Japanese-style landscape garden. Accenting the

main garden is an impressive three-story pagoda and graceful garden bridges. Inside contains several old houses and farm buildings as well as Important Cultural Properties such as Rinshunkaku Villa and Chosukaku House.
Hours:9:00-16:30 Admission:¥500
Access: From Sakuragicho Sta., take Bus NO.8 or No.125 to Honmoku-Sankeien-mae.

MARINE TOWER

106 meters, the tallest inland lighthouse in the world, with an observatory located 100 meters above ground.
Hours: 10:00-21:00 Admission: ¥700
Access: 15min. Walk from JR Ishikawacho station

MARITIME MUSEUM

The site of the previous Nippon Maru, the former training ship for Japan's Maritime Defense Force. The Yokohama Maritime Museum, which specializes in ports and ships, is located next to the Nippon Maru.
Hours: 10:00-17:00 (Closed Monday) Admission: ¥600
Access: 7 min. walk from JR Sakuragicho station

Other Information:

JAPANTOURIST ORGANIZATION
http://www.jnto.go.jp/
YOKOHAMA CONVENTION & VISITORS BUREAU
http://www.welcome.city.yokohama.jp/eng/tourism/
NARITA AIRPORT
http://www.narita-airport.jp/en/
YES ! TOKYO
http://www.tcvb.or.jp/en/index_en.htm

Accommodations

OFFICIAL TRAVEL AGENT

JTB Yokohama Convention Center has been appointed as the official travel agent. Inquiries and applications concerning arrangements should be addressed to:

JTB Tokyo Metropolitan Corp.
JTB Yokohama Convention Center
Address: Dai-6-Yasuda Bldg. 6F, 3-29-1 Tsuruya-cho, Kanagawa-ku, Yokohama 221-0835, Japan
Phone: +81-45-316-4602 Fax:+81-45-316-5701
e-mail: jtb_convention@jtb.jp
Person in charge: Hideo KUMABE (Mr.), Shinji HIDA (Mr.)

HOTEL RESERVATION

JTB Yokohama Convention Center has reserved blocks of rooms at hotels in Yokohama during the period. Please fill in the Hotel Reservation Form and submit it to JTB Yokohama Convention Center by 22nd December, 2006, Japan time. Reservation will be made on a first-come, first-served basis. Please indicate your order of preference in the application form. If your desired hotel is fully booked, JTB Yokohama Convention Center will reserve your second choice or a hotel in the same grade. Hotel charge should be paid to JTB Yokohama Convention Center. When submitting the application, please indicate credit card number, expiry date and card holder's signature. Confirmation of hotel reservation will be sent by fax in 2 weeks or so. Hotel reservation will not be honored without this confirmation.

Cancellation of Hotel Reservation

In the event of cancellation, written notification should be sent to JTB Yokohama Convention Center. The following cancellation fees will be charged to your credit card.

Up to 9 days before the first night of stay	2,000yen
8 to 2 days before	20% of daily room charge (minimum 2,000yen)
one day before or after	100% of daily room charge
No notice given	100% of daily room charge

Hotels

#	Name/Address/Fee per Room per Night/Access
A	**Yokohama Grand Inter-Continental** 1-1-1 Minatomirai, Nishi-ku, Yokohama Tel: +81-45-223-2222, Fax: +81-45-221-0650 **S**:¥18,480, **SB**:¥21,000, **T**:¥20,790, **TB**:¥23,100 Adjacent to Pacifico
B	**Pan Pacific Hotel Yokohama** 2-3-7 Minatomirai, Nishi-ku, Yokohama Tel: +81-45-682-2222, Fax: +81-45-682-2223 **S**:¥15,750, **SB**:¥17,850, **T**:¥18,900, **TB**:¥23,100 2 min. walk to Pacifico
C	**Yokohama Royal Park Hotel** 2-2-1-3 Minatomirai, Nishi-ku, Yokohama Tel: +81-45-221-1111, Fax: +81-45-224-5153 **S**:¥15,225, **SB**:¥16,800, **T**:¥17,850, **TB**:¥21,000 5 min. walk to Pacifico
D	**Nabios Yokohama** 2-1-1, Shinko, Naka-ku, Yokohama Tel: +81-45-633-6000, Fax: +81-45-633-6001 Fri & Sat: **S**:¥9,450, **SB**:¥10,395, **T**:¥17,850, **TB**:¥19,740 Mon–Thu: **S**:¥8,400, **SB**:¥9,345, **T**:¥15,750, **TB**:¥17,640 7 min. walk to Pacifico
E	**Yokohama Sakuragicho Washington Hotel** 1-1-67, Sakuragi-cho, Naka-ku, Yokohama Tel: +81-45-683-3111, Fax: +81-45-683-3112 **S**:¥9,975, **SB**:¥11,025, **T/TB**:Not Available 8 min. walk to Pacifico
F	**Sanai Yokohama Hotel** 3-95, Hanasaki-cho, Naka-ku, Yokohama Tel: +81-45-242-4411, Fax: +81-45-242-7485 **S**:¥8,400, **SB**:¥9,240, **T**:¥14,700, **TB**:¥16,380 15 min. walk to Pacifico
G	**Yokohama Heiwa Plaza Hotel** 5-65, Ohta-machi, Naka-ku, Yokohama Tel: +81-45-212-2333, Fax : +81-45-212-2350 **S**:¥6,830, **SB**:¥7,560, **T**:¥10,290, **TB**:¥11,760 20 min. walk to Pacifico
H	**Hotel Camelot Japan** 1-11-3, Kita-saiwai, Nishi-ku, Yokohama Tel: +81-45-312-2111, Fax: +81-45-312-2143 **S**:¥7,880, **SB**:¥9,140, **T**:¥12,600, **TB**:¥15,120 15 min. walk to Pacifico

* S = Single, SB = Single with breakfast,
T = Twin, TB = Twin with breakfast.

Note: Room charge includes service charge and 5% tax.

Hotel Reservation Form

ASP-DAC 2007
January 23 - 26, 2007, Yokohama Japan

Please complete and return this form to:
JTB Tokyo Metropolitan Corp.
JTB Yokohama Convention Center
Address: Dai-6-Yasuda Bldg. 6F, 3-29-1 Tsuruya-cho, Kanagawa-ku, Yokohama 221-0835, Japan
Phone: +81-45-316-4602 Fax:+81-45-316-5701
e-mail: jtb_convention@jtb.jp

Deadline: Dec. 22, 2006, Japan time
Note: You should send this form by postal mail or fax when you apply.

(Please type or write in block letters.)
Full Name: ( )Prof. ( )Dr. ( )Mr. ( )Ms.

Family Name: _____, First Name: _____

Middle Initial: _____

Affiliation: _____

Mail Stop: _____

Dept./Div.: _____

Mailing Address: _____

City: _____ State: _____

Zip:_____ Country:_____

Phone:_____Fax:_____

E-mail: _____

Please remember to include your country and/or city code for Phone/Fax numbers.

Name of Accompanying Person(s), Family Member(s) if any:
( )Mr. ( )Ms.

Family Name: _____, First Name:_____

Middle Initial: _____

Arrival Schedule:

Arriving at _____(airport) on _____(date)

by _____(flight number)

Hotel Accommodations:
Please select 2 hotels in order of preference and enter the name of the hotel and the hotel number(see hotel list in this program).

1st choice:_____(No.)

2nd choice:_____(No.)

Room Choice: ( )Single ( )Twin

Breakfast: ( )Yes ( )No

Period of Stay: Check-in _____ Check-out _____ for __ nights

Guaranttee of Booking:
Credit Card: ( )AMEX( )VISA( )Master Card

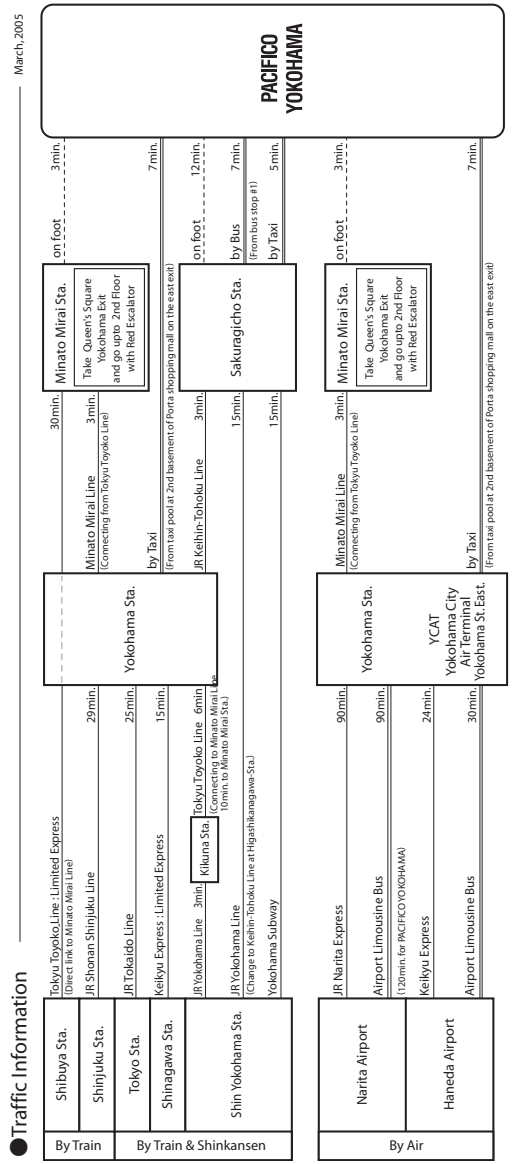
Card Number: _____- _____- _____- _____

Card Holder's Name : _____

Expiration Date: ___/_____(month/year)

Authorized Signature: _____

Access to Pacifico Yokohama



■Driving To Pacifico

[From Tokyo]

Metropolitan Expressway

- Toward Yokohama Park, Yokohane Route ▲ Minato Mirai Ramp,3min.
- Toward Yokohama (over Bay bridge), Wangan Route ▲ Minato Mirai Ramp,3min.

[From Kansai or Chubu]

Tomei Expressway Yokohama Machida IC

- Hodogaya Bypass,20min. ▲ Kariba IC ▲ Toward Yokohama,Metropolitan Expressway,Kariba Route,10min. ▲ Minato Mirai Ramp,3min

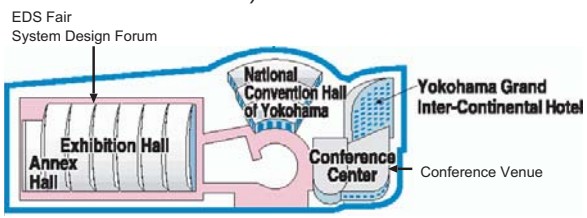
PACIFICO YOKOHAMA

■Parking Lot

Minato Mirai Public Parking Lot +81-45-221-1301	Capacity:1,200 (Standard-sized cars only)	Open 24 hours	Rates:Standard-sized car 260yen/30min. (1,300yen for max. 15hours between 8 and 23 on weekdays.)
Bus/Large Vehicles Parking Lot +81-45-221-1302	Capacity:40	Open 24 hours	Rates:Large vehicle 500yen/30min.

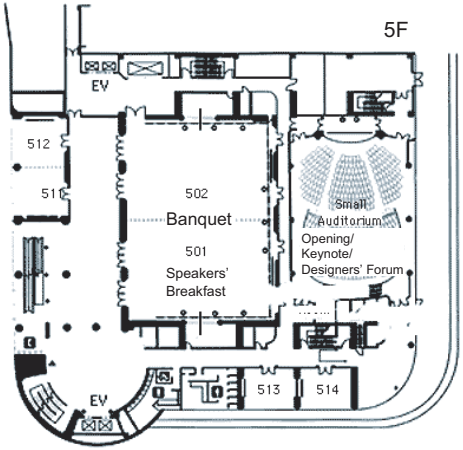
Venue Map/Room Assignment

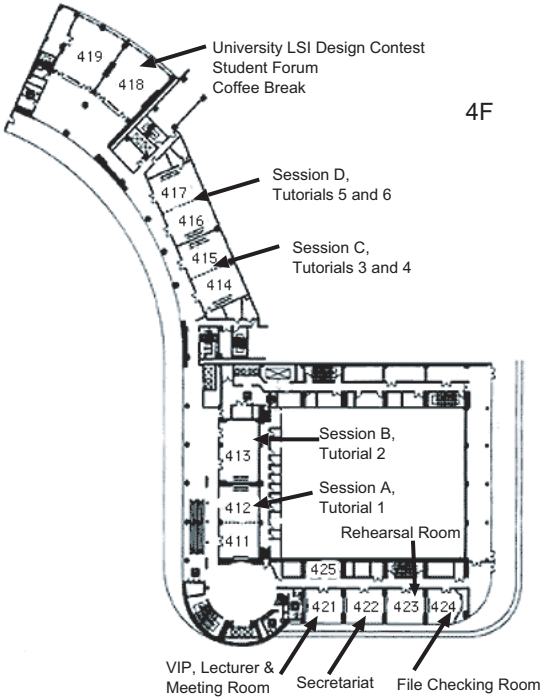
- ASP-DAC Conference is held at “Conference Center.”
- EDS Fair 2007 and System Design Forum 2007 are held at “Exhibition Hall/Annex Hall.” (2min. walk from Conference Center.)

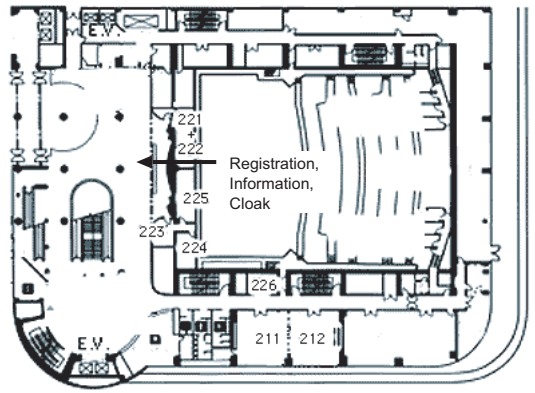


Conference Venue Map

Location	Event
Entrance Hall (2F)	Registration, Information, Cloak
Small Auditorium (5F)	Opening, Keynote, Deginers’ Forum
411+412 (4F)	Session A, Tutorial 1
413 (4F)	Session B, Tutorial 2
414+415 (4F)	Session C, Tutorials 3 and 4
416+417 (4F)	Session D, Tutorials 5 and 6
418 (4F)	Poster Discussion, Student Forum, Coffee Break
423 (4F)	Rehearsal Room
424 (4F)	File Checking Room
501+502 (5F)	Banquet, Speakers’ Breakfast
Exhibition Hall/Annex Hall	EDS Fair, System Design Forum







Conference Center Map

Electronic Design and Solution Fair 2007

The Japan Electronics and Information Technology Industries Association (JEITA) will be hosting the Electronic Design and Solution Fair 2007 at the Pacifico Yokohama on January 25 & 26, 2007. This will be the 14th time that this event has been held, including EDSFair's predecessor, the EDA TechnoFair.

The goal of EDSFair is to introduce and disseminate information about the latest design solutions, design technologies, and EDA technologies required to produce the semiconductors and electronic systems for the IT applications that will form the foundation of the future information society, whose citizens will enjoy a ubiquitous computing environment. The fair thus contributes to the development of electronics and other IT-related industries.

From the second half of last year there have been signs of recovery in Japan's electronics industry, with both production and exports on the rise, and this recovery has been gathering momentum this year. This is especially noticeable in the fields of semiconductors and displays, where a growing number of companies are increasing their capital investment.

JEITA forecasts that this year Japan's electronics industry will achieve a 2.3% increase over last year in its domestic production. Depending on business conditions in the second half, it is possible that the final figure may even exceed ¥20 trillion. Furthermore, this upturn is not limited in scope: everything from components and semiconductors to home IT appliances and mobile phones are expected to benefit from growing demand.

Nevertheless, facing increased competition in the international arena, Japan's industries as a whole need to enhance their competitive power, and this requires innovations on many different levels. It is therefore of critical importance that we foster the industry's human resources — particularly the engineers needed to realize these innovations.

"World-Leading Technologies — Yours to Discover" is the theme of this Electronic Design and Solution Fair 2007. You will find on display world-class, cutting-edge technologies tailored for an age that demands new solutions. There are a variety of seminars and a conference offering a wide range of up-to-date information. There are open sessions catering to young engineers, new zones that bring together both Japanese and foreign venture businesses, as well as initiatives for promoting substantive technical exchanges between industry, academia and government.

It is the fervent desire of all of us in JEITA that EDSFair will contribute to enhancing the design technologies available to Japan's electronic and IT industries, and also that both visitors and exhibitors will be able to make the best use of the opportunities afforded by this event for conducting effective and fruitful exchanges of information, and for generating new business.

We greatly look forward to the participation of many companies and professionals in this upcoming trade show.

Naoyuki Akikusa
Chairman
Japan Electronics and
Information Technology Industries Association

System Design Forum 2007 at EDS Fair

Thursday, January 25, 13:30–15:30, 16:00-18:00
Friday, January 26, 10:00-12:00, 13:30-15:30
Annex Hall, Pacifico Yokohama

Registration: On-line registration will be available from November 2006 at http://www.edsfair.com
Sponsor: Japan Electronics and Information Technology Industries Association (JEITA)
Support: Accellera, Open SystemC Initiative (OSCI)

The EDA Technical Committee (EDA-TC) of JEITA will host System Design Forum 2007 at Pacifico Yokohama, Japan. This year's forum, consisting of 3 sessions, will be held for 2 days, January 25 and 26, 2007.

The first day (Jan.25) will focus on recent trends in Physical Design technologies developed in Japan for overcoming the process variation of DFM (Design for Manufacturing) after the process technologies' migration to 65nm or below.

The second day (Jan.26) will cover system-level design languages (SystemC and SystemVerilog), some effective methods for addressing the design crisis of SoC (System-on-a-Chip). Easy-to-understand explanations of the latest standardization, tutorials and introduction of the cutting-edge design examples will be given for each language.

Session 1: Physical Design Forum, January 25 (13:30–15:30, 16:00–18:00)

Chair: **H. Masuda (JEITA Physical Design Standardization Study Group)**

Within Die (WID) process variation in 45–90nm processes is known to be a major critical issue for timing-closure in SoC design. Recently, Statistical Static Timing Analysis (SSTA) is proposed as a fundamental solution approach to overcome the problems associated with process variation. In this session, the following topics will be presented to overview the current status of variation-aware design methodology: 1) Variation-aware design — present and future, 2) Test-structures for variability measurement & analysis, 3) Modeling technique on variation, 4) Statistical STA — practical applications, and 5) Circuit technique to mitigate variability.

Session 2: SystemC Users Forum 2007, January 26 (10:00-12:00)

Chair: **T. Hasegawa (JEITA SystemC Task Group)**

On December 12, 2005, IEEE approved SystemC (IEEE Std. 1666-2005). Since then, SystemC that is a C-based

language, has been widely used as a standard language for both verification and system-level design flows in the fields of both verification and design. Included in this session are: 1) Update of SystemC current status and road map, presented by OSCI, 2) Result of JEITA SystemC Task Group's research for transaction-level modeling and high-level synthesis, and 3) Examples of design-related SystemC.

Session 3: SystemVerilog Users Forum 2007, January 26 (13:30-15:30)

Chair: **K. Hamaguchi (JEITA SystemVerilog Task Group)**

SystemVerilog, the next-generation language after Verilog HDL (IEEE Std. 1364), has seen rapid adaptation by LSI designers and verification engineers as the Hardware Design and Verification Language (HDVL) since it was approved by IEEE (IEEE Std. 1800-2005) in November 2005.

Included in this session are: 1) Update of next SystemVerilog Standardization and its related activities presented by Accellera, 2) Tutorial on SystemVerilog Testbench and explanations on technical trends presented by the JEITA SystemVerilog Task Group, and 3) Presentation of firsthand experiences by Japanese SystemVerilog users on verification features of SystemVerilog.

Note: Most of the presentations at the System Design Forum 2007 will be given in Japanese.

For more information, visit the following web site:
http://www.edsfair.com.