Meeting with the forthcoming IC design

– The era of power, variability and NRE explosion and a bit of the future –

- Solving issues of IC's by 3D-stacking –

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University of Tokyo
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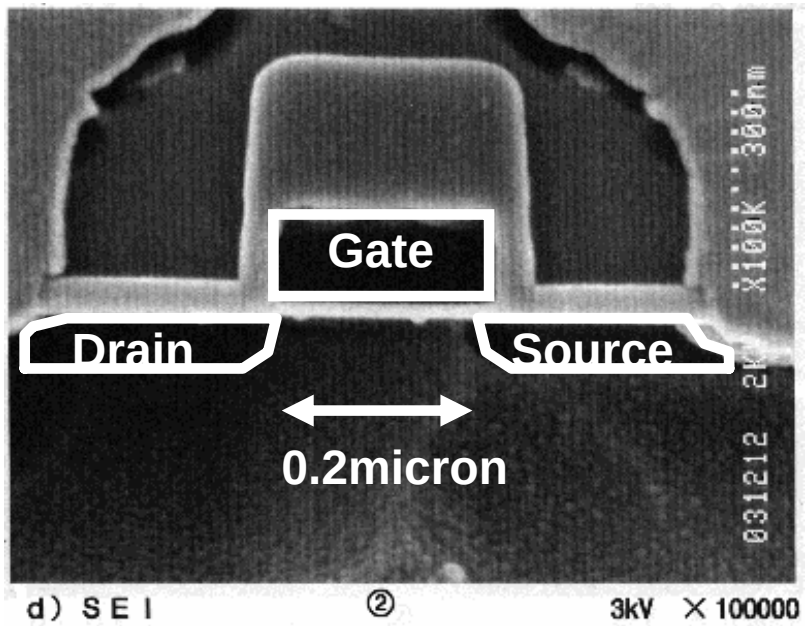
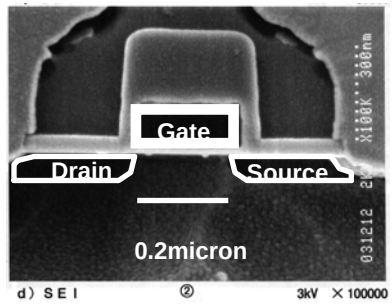
Moore's law continues as a backbone but…



Size 1/2



Favorable effects

Size	x1/2
Voltage	x1/2
Electric Field	x1
Speed	x3
Cost	x1/4

Unfavorable effects

Power density	x1.6
RC delay/Tr. delay	x3.2
Current density	x1.6
Voltage noise	x3.2
Design complexity	x4

Three explosions threat Moore's law

- Explosion of power
- Explosion of integrity attackers
- Explosion of complexity

➔ Explosion of NRE*

*) Non-Recurring Engineering Cost

3D Stacking for solving issues

- **Silicon chips stacking**

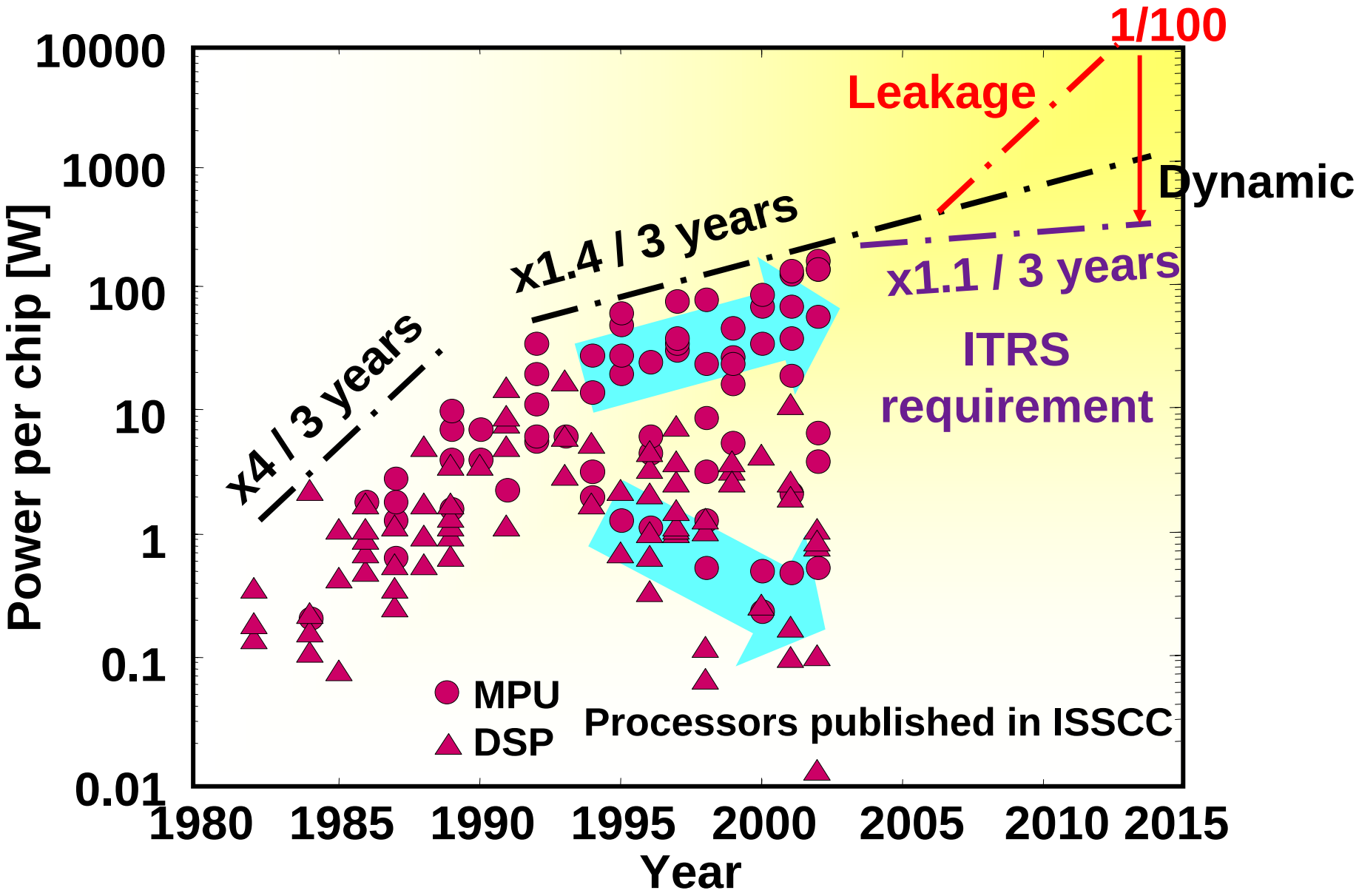
  for lower power & lower NRE

- **Organic sheets stacking**

  for newer applications

With design tool implications

Power is a stumbling block to Moore's law

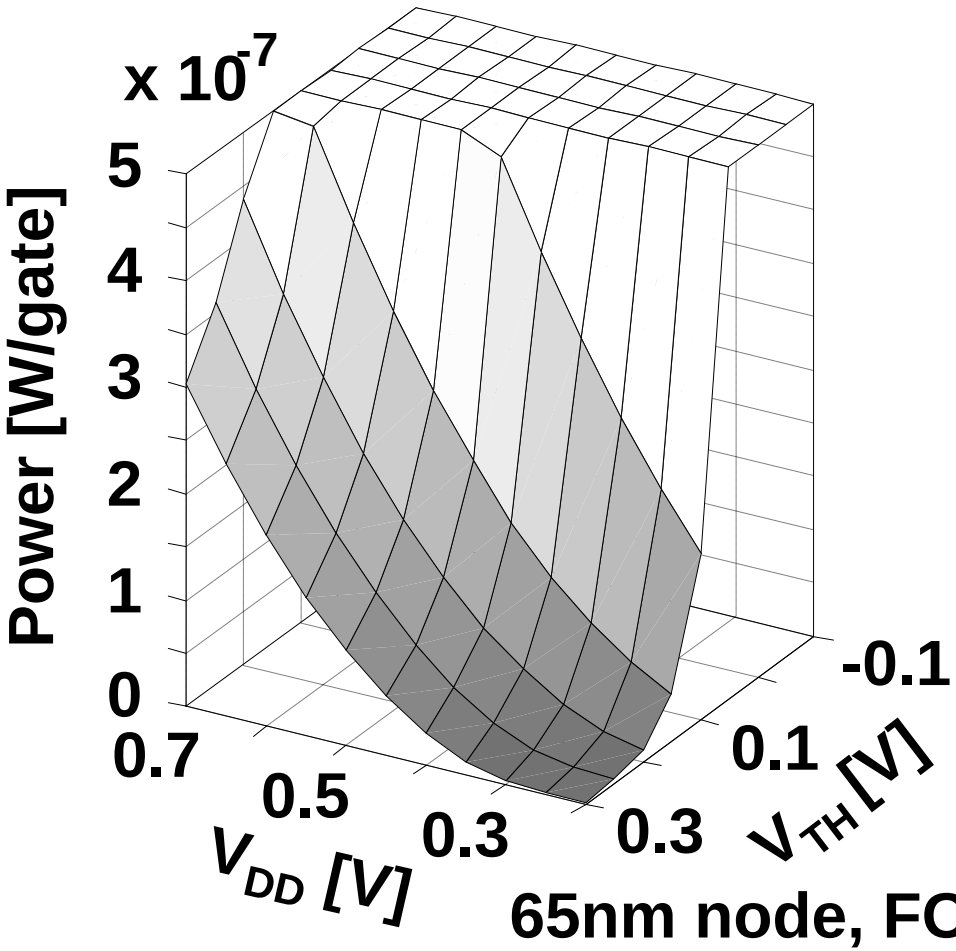


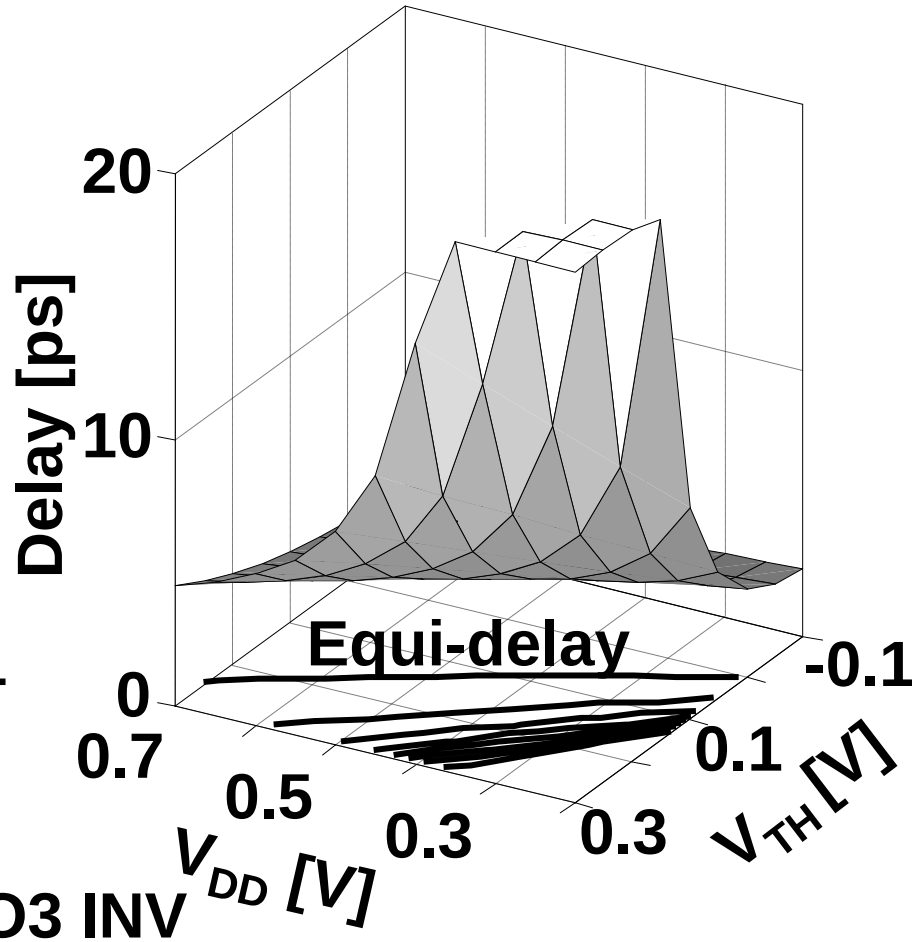
Trade-off between power and delay

$$Power = a \cdot f \cdot C \cdot V_{DD}^2 + I_0 \cdot 10^{-\frac{V_{TH}}{S}} \cdot V_{DD}$$

(+ other leakage)

$$Delay \propto \frac{C \cdot V_{DD}}{(V_{DD} - V_{TH})^{1.3}}$$



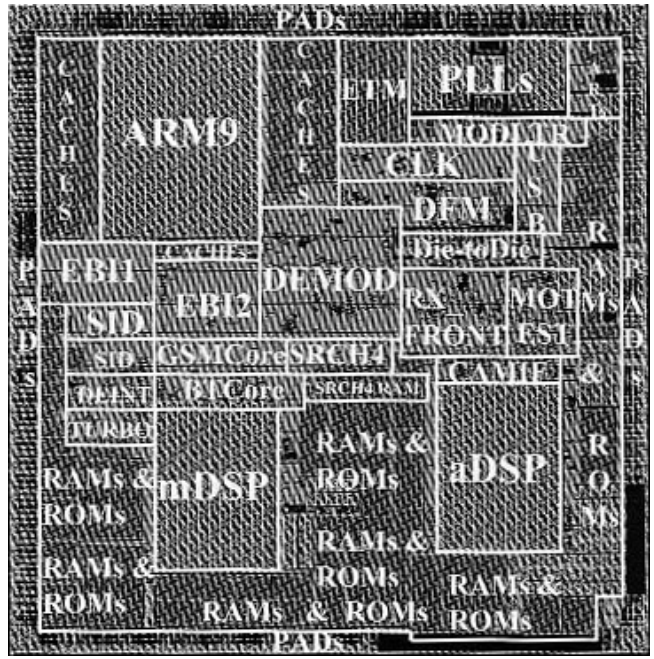


65nm node, FO3 INV

Change power depending on required performance.

Example of power-aware design

Diagram	NAND2(*non-footswitch*)	fs_NAND2(*footswitch*)
SYMBOL	a, b, nz, HVT	a, b, slpb, nz, LVT, HVT
SCHEMATICS	a, b, nz	a, b, slpb, nz, LVT, HVT
LAYOUT	V_{DD}, V_{SS}, a, b, nz, nwell	1.25X, V_{DD}, V_{SS}, a, b, slpb, nz, nwell, LVT Layer

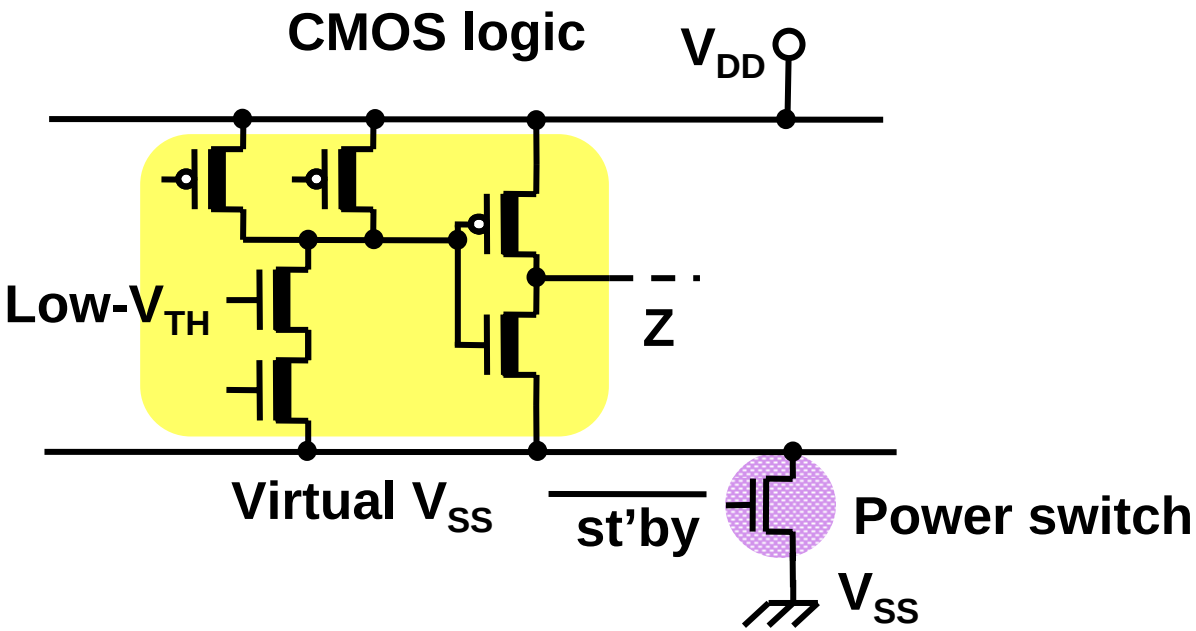


Multi-V_{DD}: Seven V_{DD}'s

Dual-V_{TH}: Two V_{TH}'s for PMOS and NMOS each

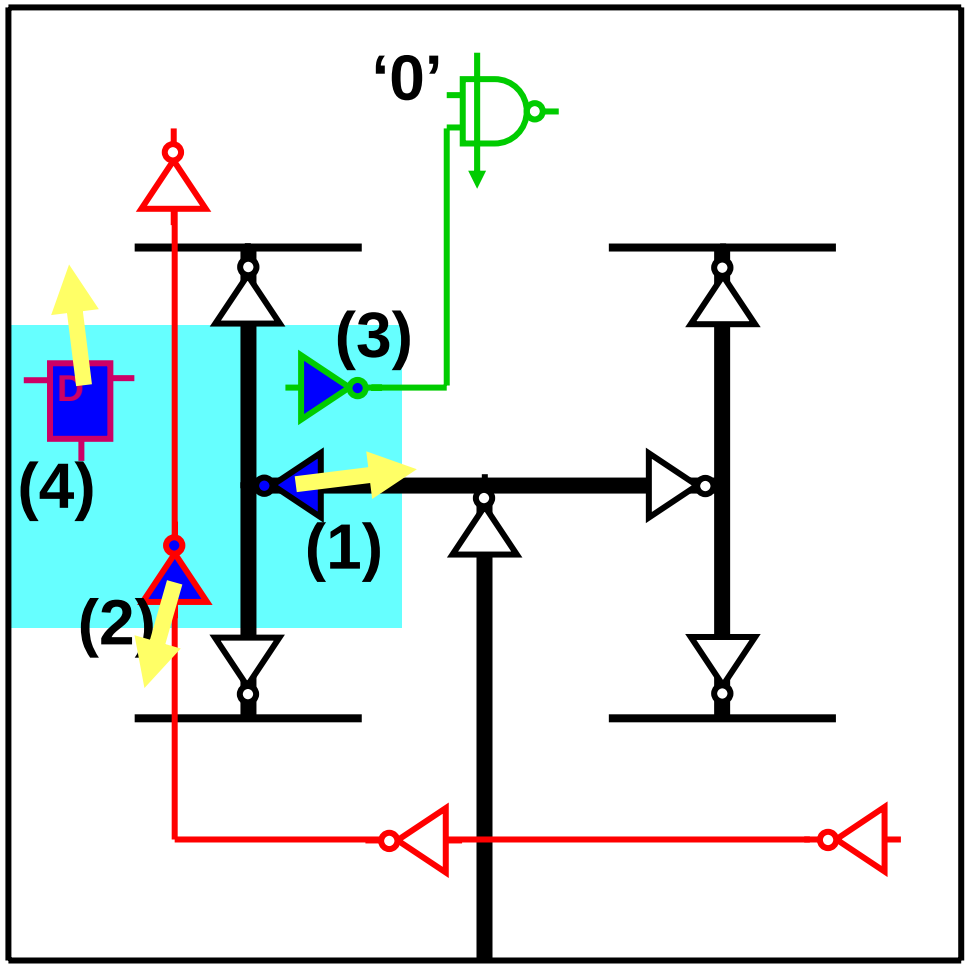
Power gating: Selective MTCMOS reduced standby to 1/3~1/4.

G. Uvieghara, et al., "A Highly-Integrated 3G CDMA2000 1X Cellular-Baseband Chip with GSM/AMPS/GPS/Bluetooth/Multimedia Capabilities and ZIF RF Support," ISSCC paper#23.3, Feb. 2004.



Power-gating to cut-off V_{DD} of inactive blocks is getting a major leakage-aware design style and seems easy but…

Pitfalls in power-gating



1) Clock buffers
2) Repeaters
3) Gates receiving power-gated signals
4) Registers will lose stored info
5) Other common blocks like analog and sleep signal generator

Power-gated block

Big and rather slow (μs-order) noise on power supply line when switched off and on.

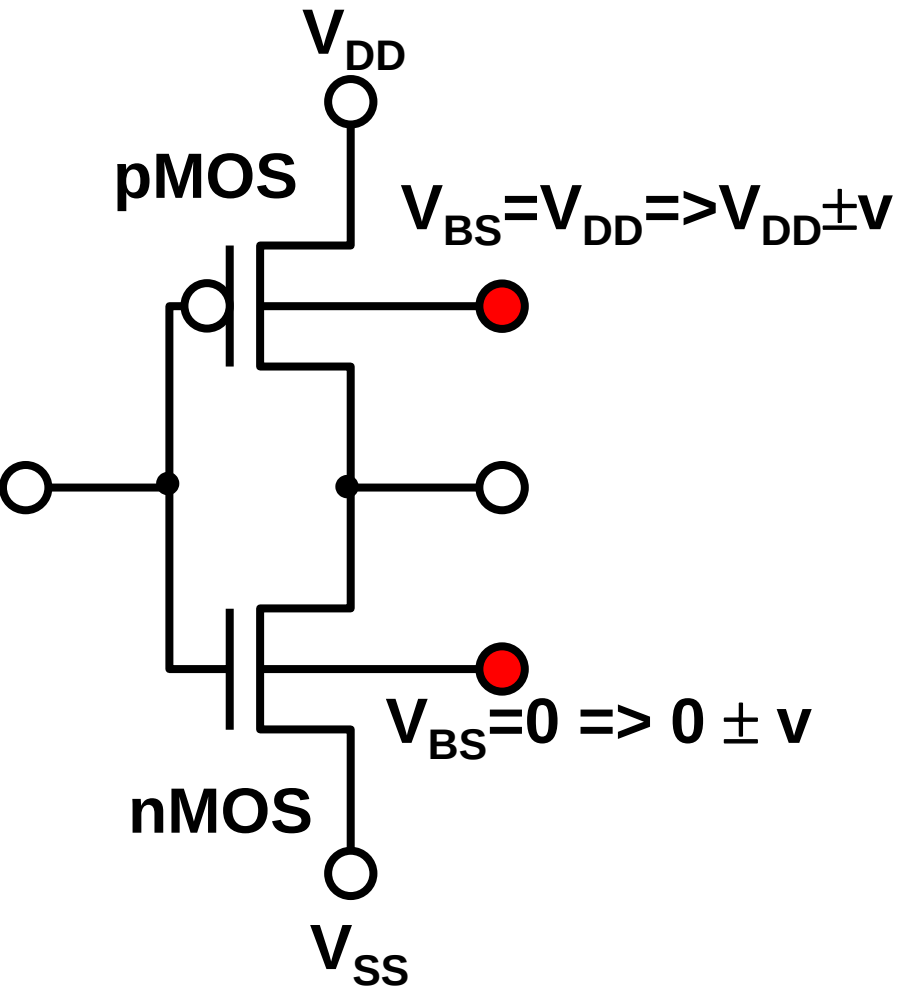
Tool implications of power-gating

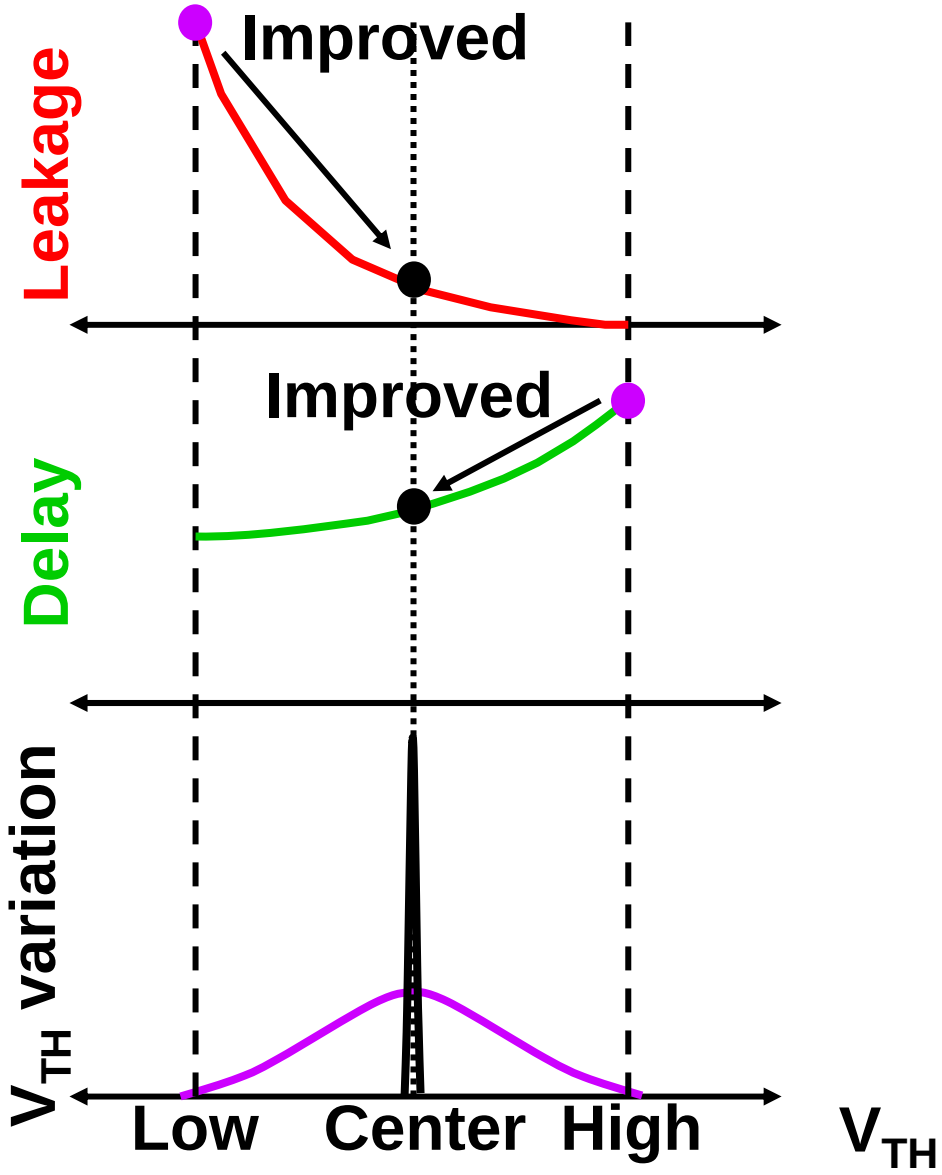
1) High-level description of power-gating
2) Power estimation tool
3) Sizing of power switch
4) Delay estimation under the effect of the power switch
5) Automatic generation of sleep signal
6) Layout level considerations
7) Power line integrity at sleep and wake-up

New tools for each new design approach

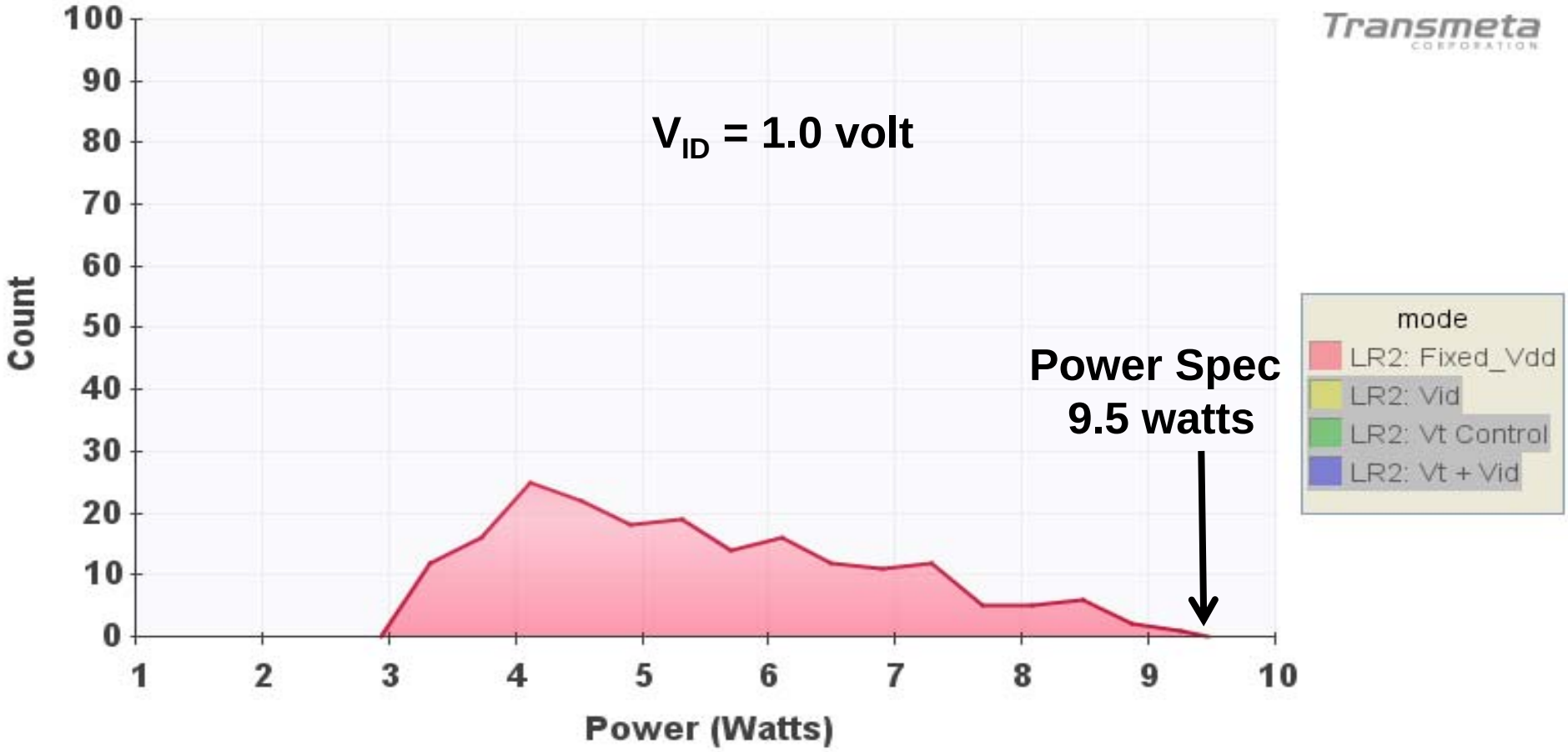
Adaptive V_{DD} & V_{TH} control for lower power with variability

Adaptive voltage for variation control





Transmeta Efficeon 1.5 GHz Fixed V_{DD}



mode	count	min	mean	median	max	stdev
LR2: Fixed_Vdd	196	3.14	5.44	5.18	9.46	1.45
LR2: Vid	196	2.79	3.91	3.74	6.52	0.68
LR2: Vt Control	202	2.52	3.06	3.02	3.98	0.31
LR2: Vt + Vid	202	1.95	2.86	2.85	3.62	0.29

Target: Frequency = 1.5 GHz

Courtesy: Transmeta Corp.

T.Sakurai

Transmeta Efficeon 1.5 GHz with Voltage ID

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LR2: Fixed_Vdd	196	3.14	5.44	5.18	9.46	1.45
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Target: Frequency = 1.5 GHz

Courtesy: Transmeta Corp.

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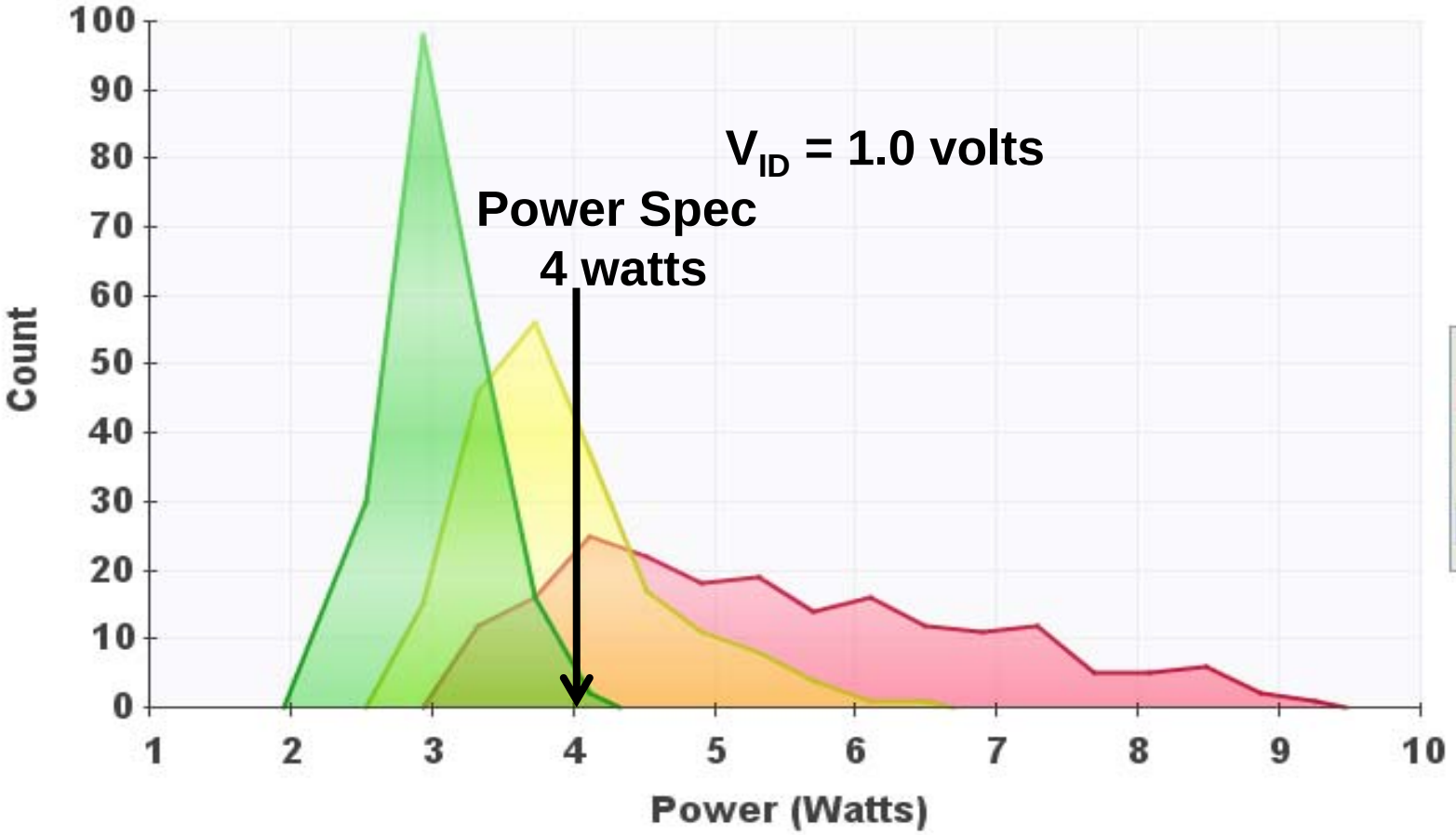
1.5 GHz with V_{TH} Control and Fixed V_{DD}



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Target: Frequency = 1.5 GHz

Courtesy: Transmeta Corp.

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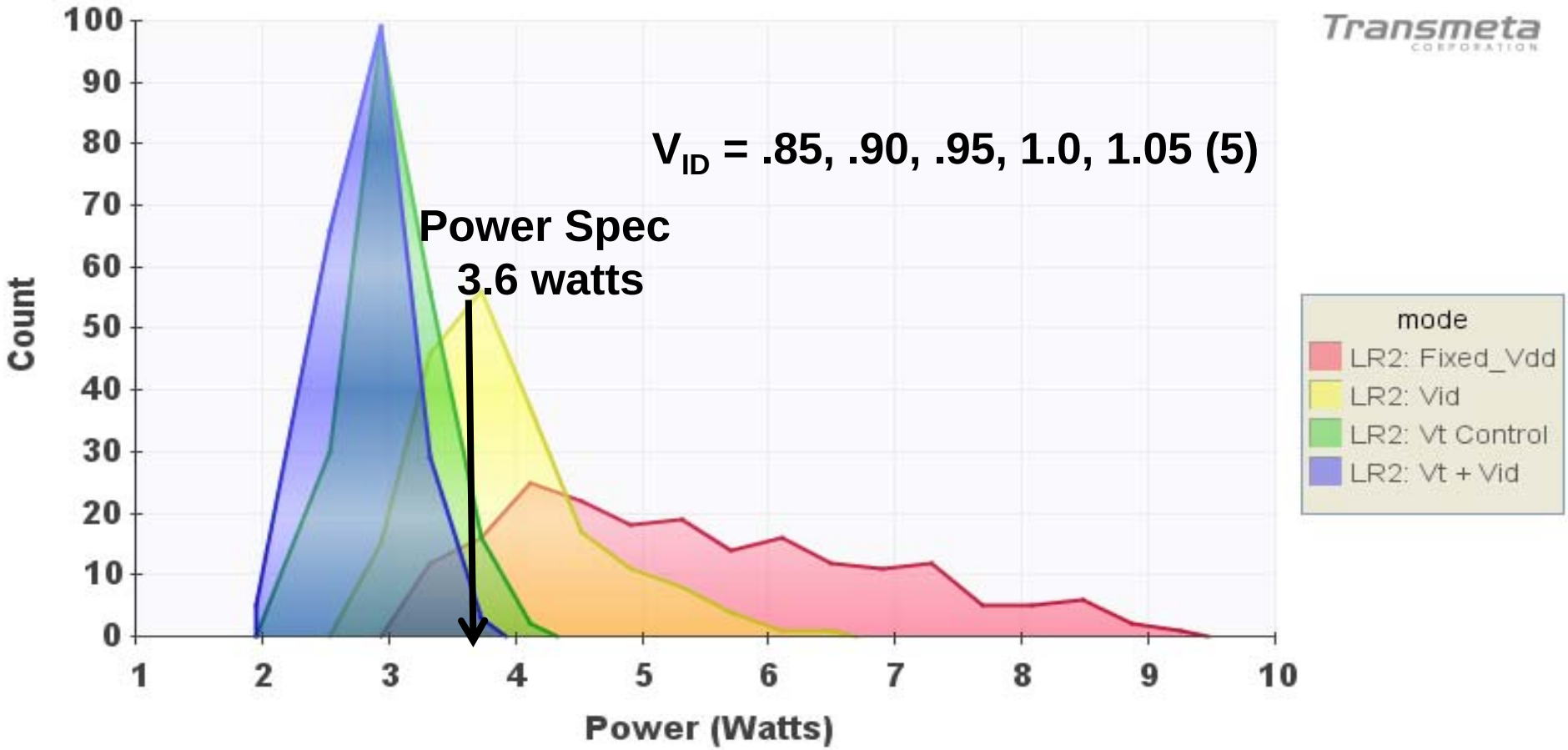
1.5 GHz with V_{TH} and V_{DD} Control



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Statistical simulation tools with V_{DD} and V_{TH} adjustment

Courtesy: Transmeta Corp.

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History and perspective of low-power VLSI systems design

Once upon a time on a peaceful chip of VLSI before the notorious power war …

We were using single V_{DD} and single V_{TH} for an entire chip.

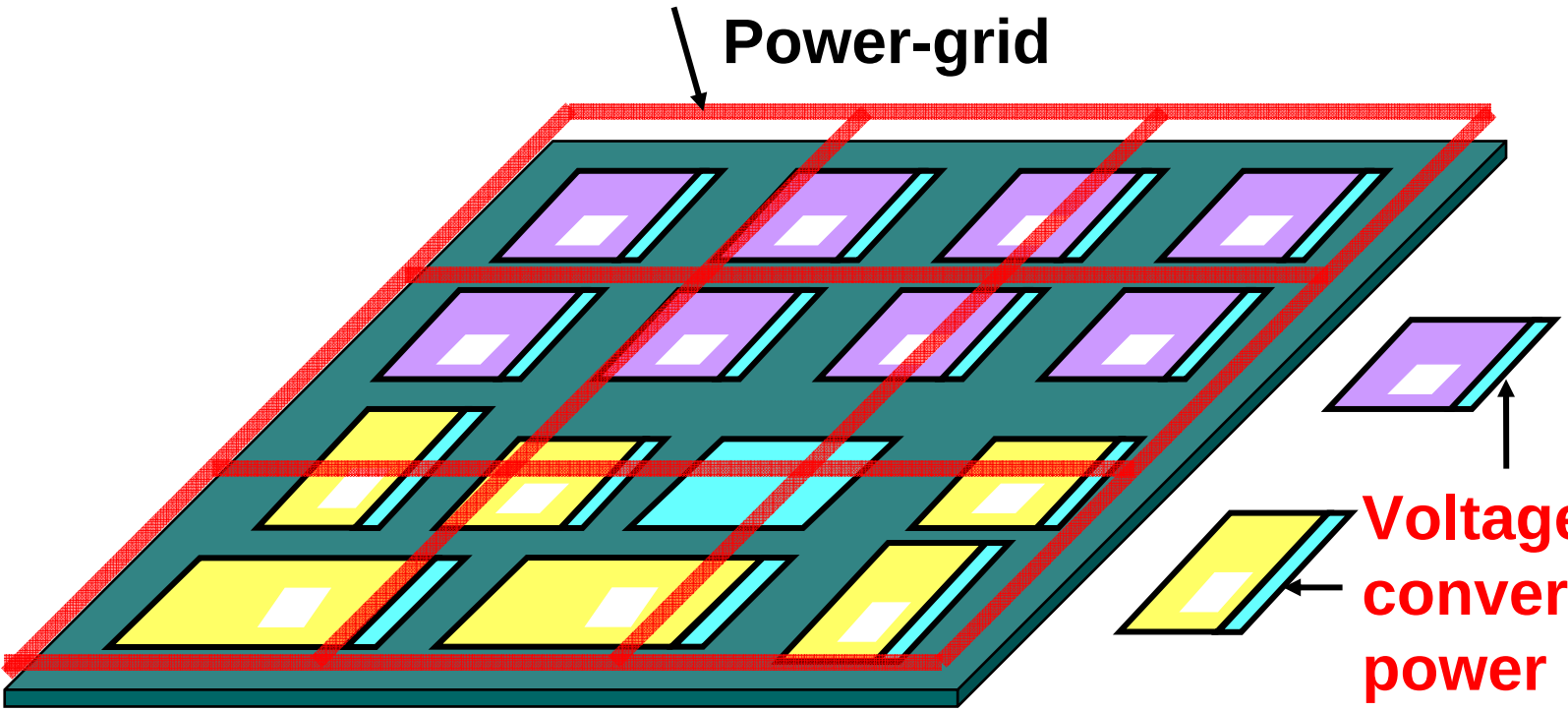
Then, the power war began and we started using multiple V_{TH} and V_{DD} depending on the location on a chip.

Still, the power war gets severer and we started to vary V_{TH} and V_{DD} in time adaptively.

In finer granularity in time and space … with a help from circuit and software.

Future power-aware VLSI

- High-voltage V_{DD} distribution to lower noise issues
- Distributed voltage conv. for fine-grain adaptive V_{DD} & V_{TH}

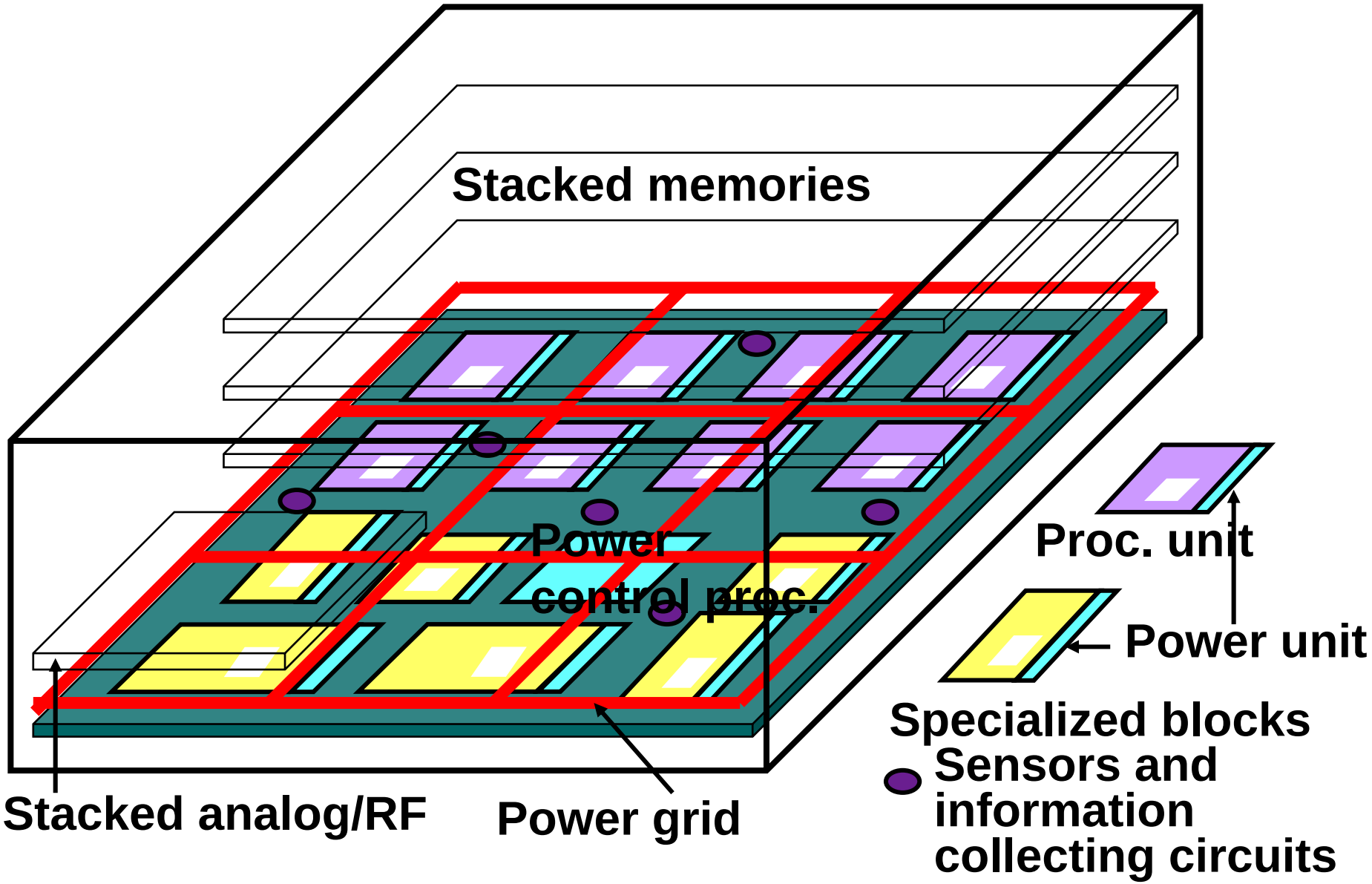


1V 50W → 50A current

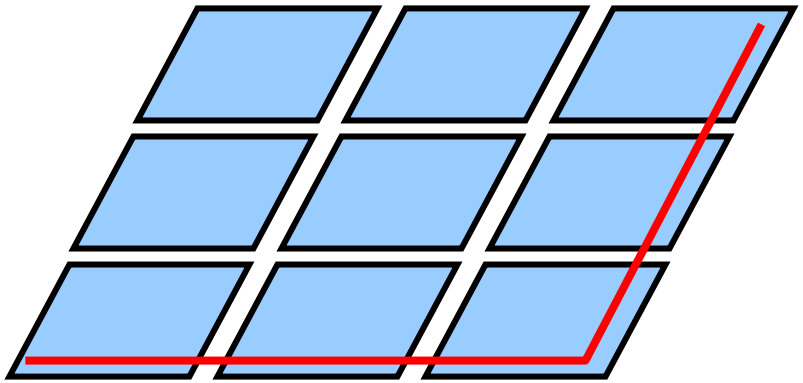
5% noise → 0.05V noise → 1mΩ sheet R → 15μm thick Cu

Thick interconnects on interposer, package or something else

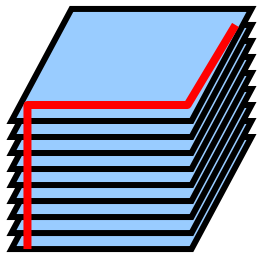
Further power-awareness by 3D stacking



3-D is good for low-power and high-perf.



System-on-a-Chip



Substrate
< 20μm thick

3-D assembly

More devices
in closer vicinity
↓
Less R and C
↓
Lower power
Higher performance
↓

Supporting design tools are the enabling technology.

System simulation & synthesis with 3D, simulation with electro-magnetic interaction

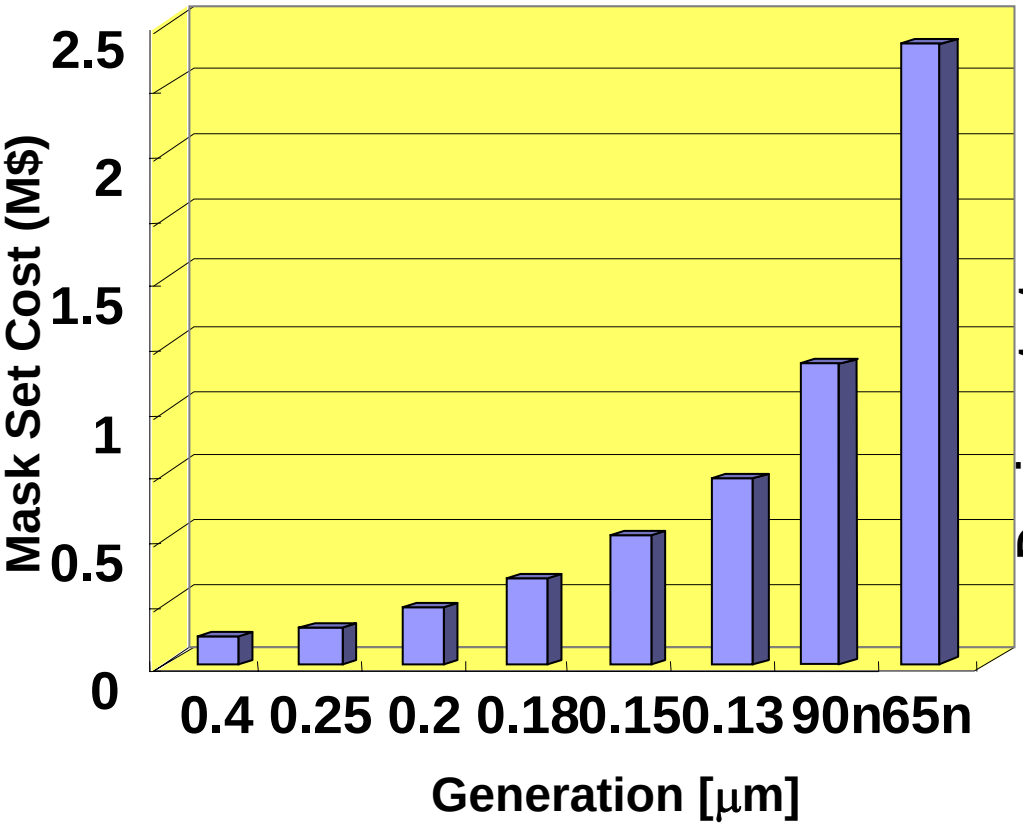
Three explosions threat Moore's law

- Explosion of power
- Explosion of integrity attackers
- Explosion of complexity

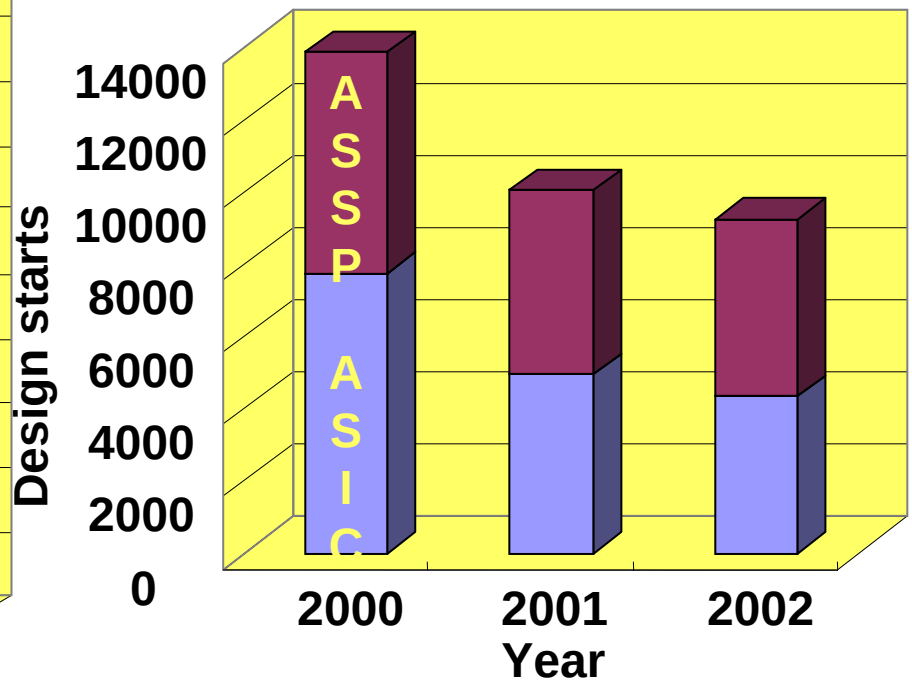
➔ **Explosion of NRE***

*) Non-Recurring Engineering Cost

Exploding NRE (Non-Recurring Eng. Cost)



Source: Rahul Goyal, Intel –Nov 2001 SEMI Mtg

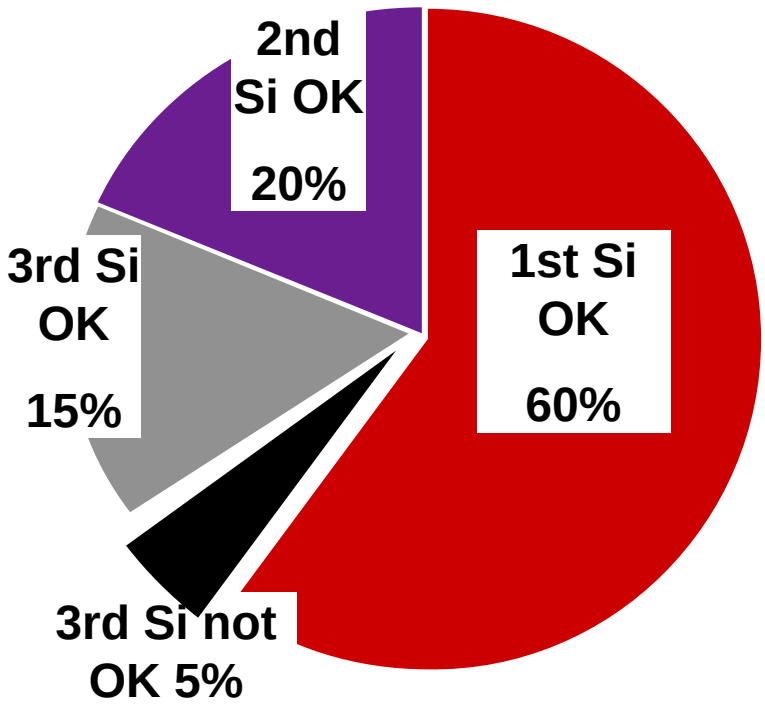


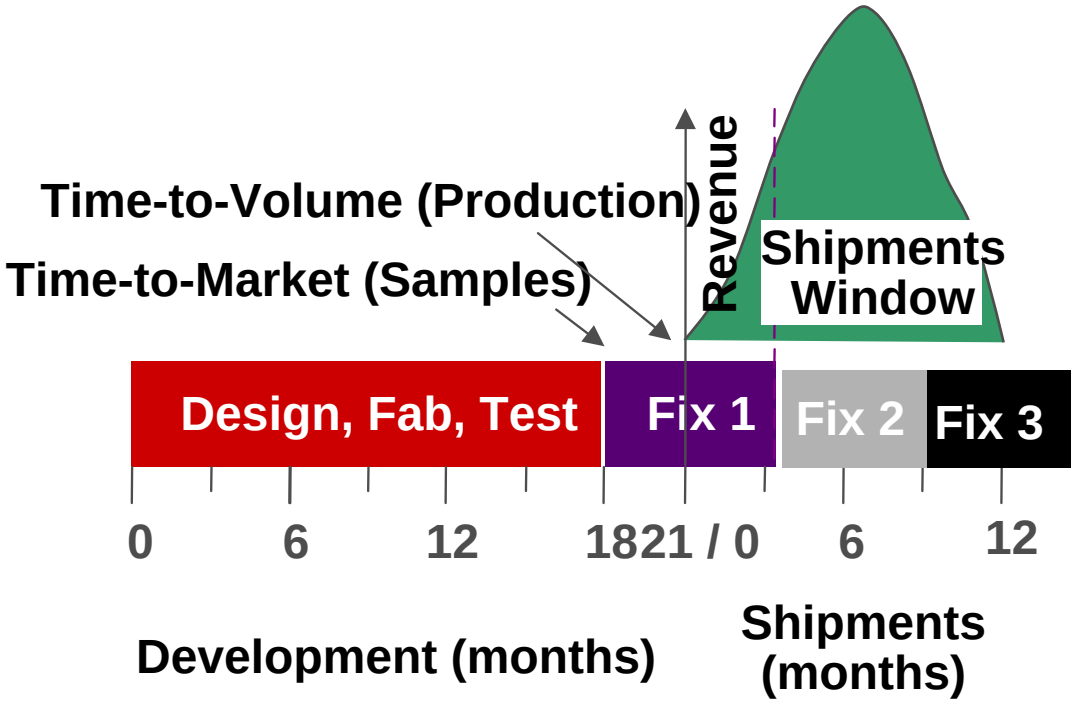
By Rick Merritt, EE Times Oct 25, 2002

http://www.eetimes.com/printableArticle?doc_id=OEG20021025S0052

- NRE for a SoC is getting $5M~10M and without over $20M sales it is difficult to make a SoC. by Bryan Lewis, Gartner Dataquest
- Number of design starts is declining from 1997.

Development is also risky





Dr. Kurt Keutzer, Ahmed Jerraya
Special Session: "How do you design a 10M gate ASIC?" 2002 Design Automation Conference
Dr. Fumiyasu Hirose, Cadence Japan

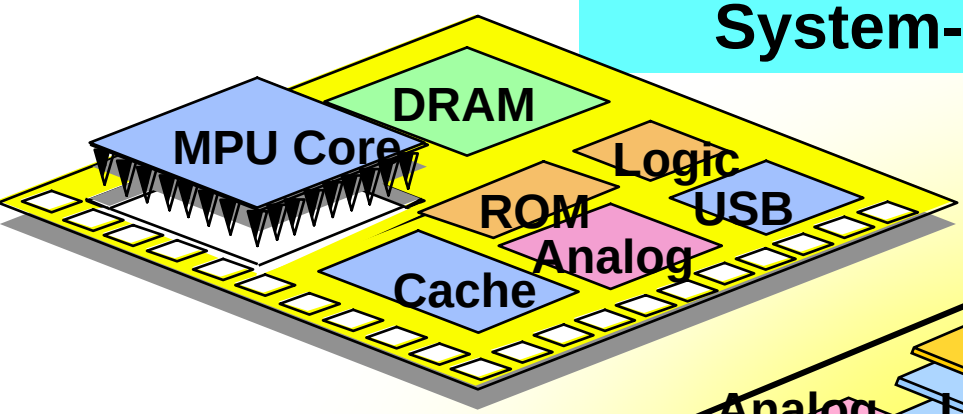
CANDE meeting 2005

The final 5-year predictions (to be reviewed in 2010) were:

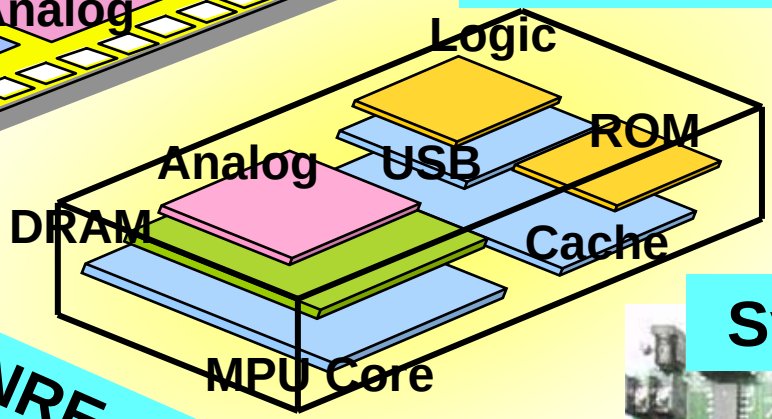
1) **IC-Package CAD will be a part of standard design flow**
2) **India and China will have more EDA startups than U.S.**
3) **Analog Designers will still resist high-level models and languages**
4) **A complete Open Source RTL-GDS tool flow will exist**
5) **Nearly all EDA tools will take advantage of multi-processors**
6) **Fewer than 200 commercial chips released in 45 nm technology**
7) **No practical nanotech computing products**
8) **SPICE-type simulators will still be the workhorse of analog designs**
9) **Moore's law will be dead**
10) **System in Package will boom**

3D stacking of chips/packages will be an assembly style suitable for low-NRE systems

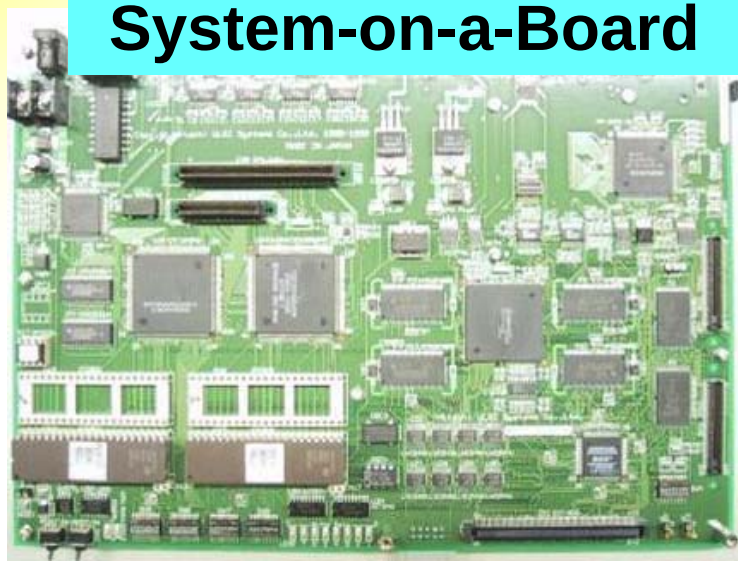
System-on-a-Chip



3D SiP or stacked packages



System-on-a-Board



Lower NRE, QTAT

Higher-perf., lower power

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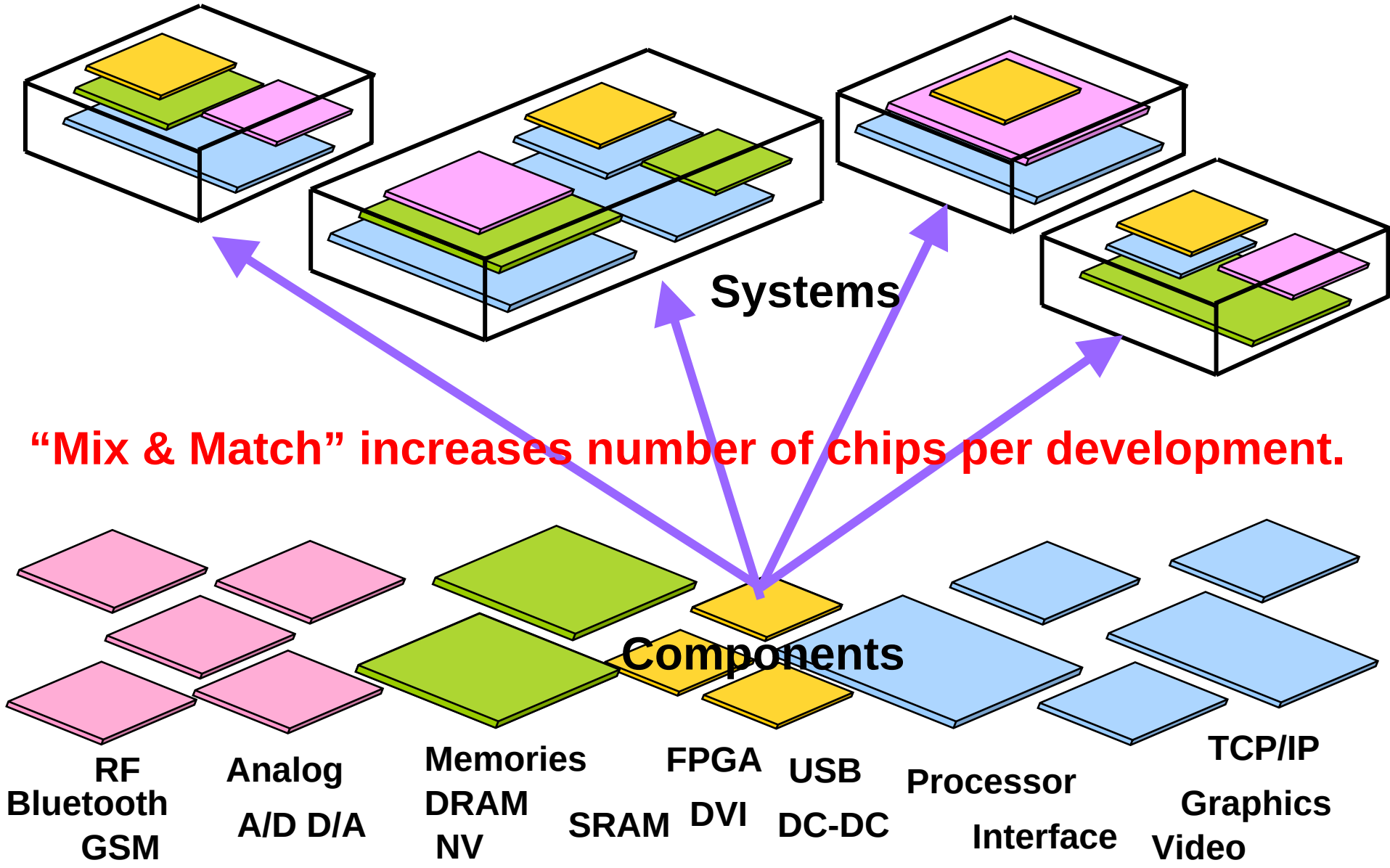
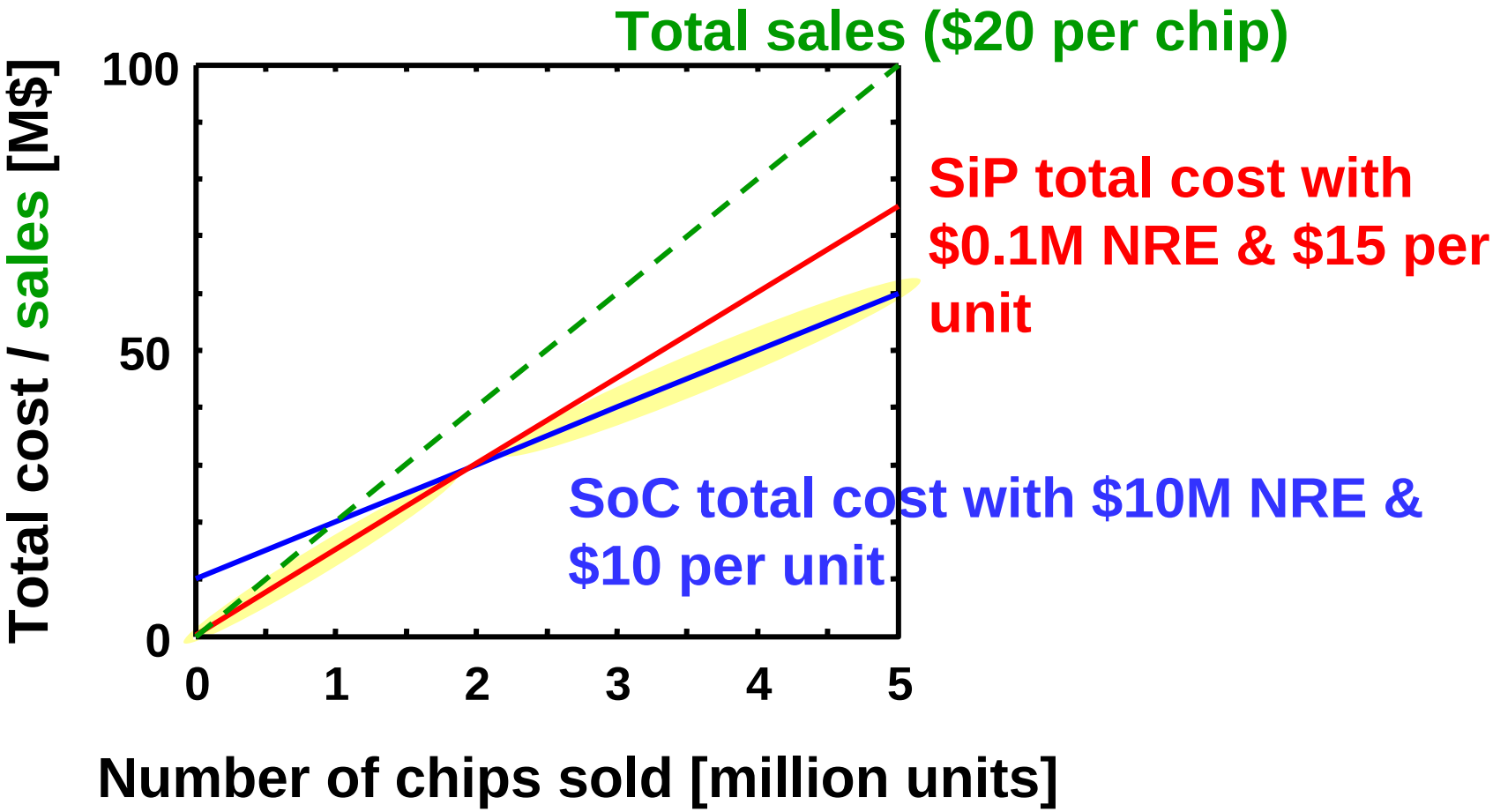
Amortizing NRE by volume production

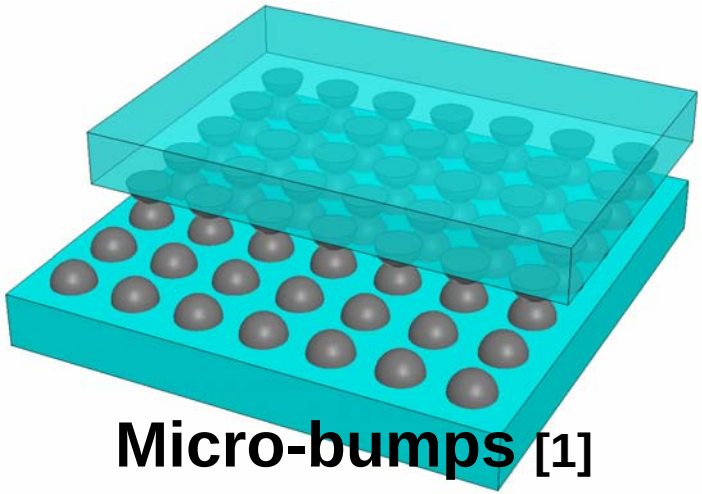
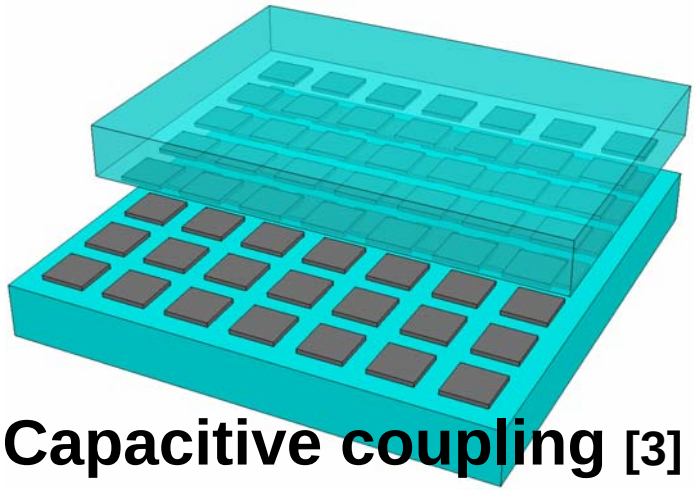
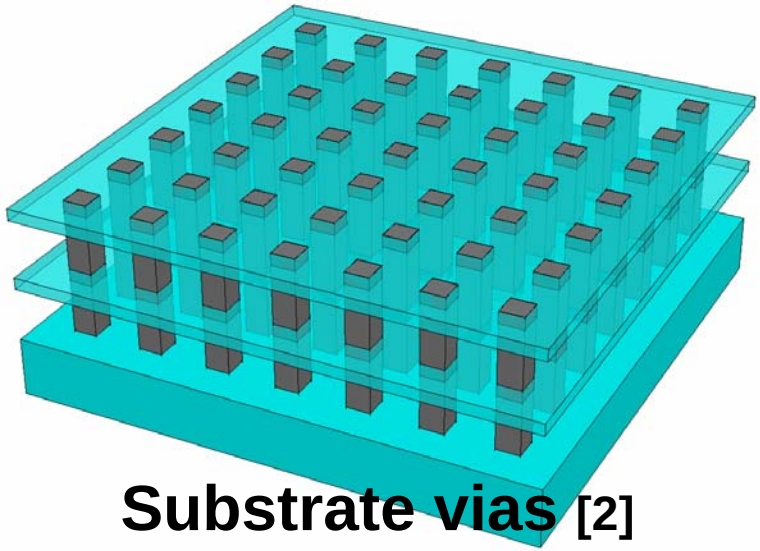
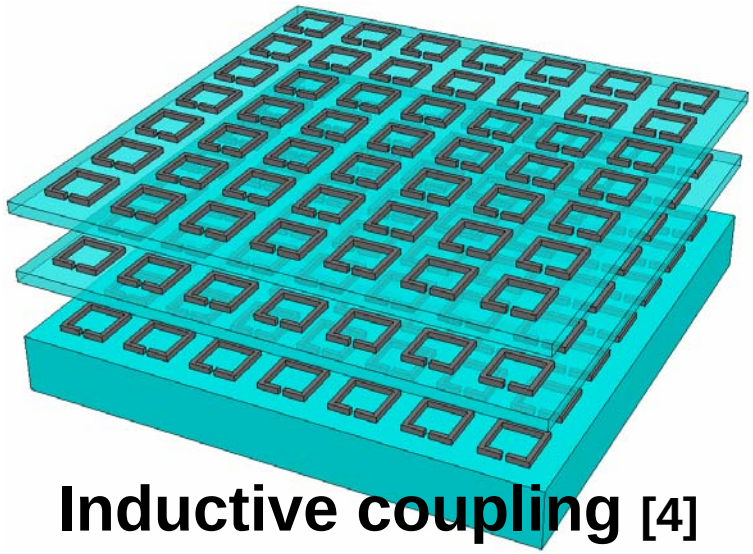


Mixed business model



Design tools from high level to physical level are needed.

Interconnections for new 3D SiP's

	Wired	Wireless
Face to face	 Micro-bumps [1]	 Capacitive coupling [3]
More than 3chips	 Substrate vias [2]	 Inductive coupling [4]

[1] T.Ezaki [2] J.Burns [3] K.Kanda [4] D.Mizoguchi, (ISSCC'04, '01, '03, '04)

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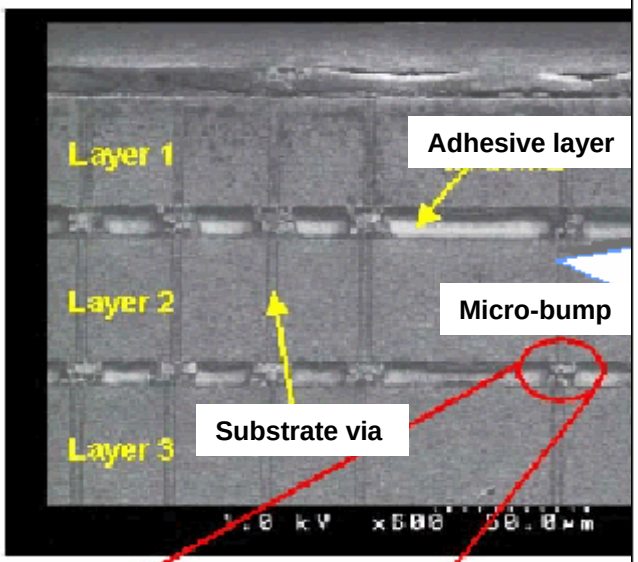
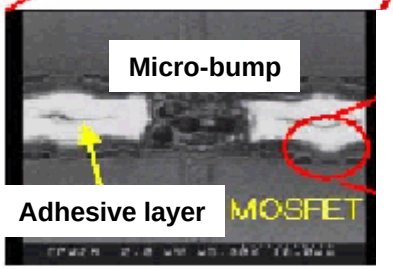
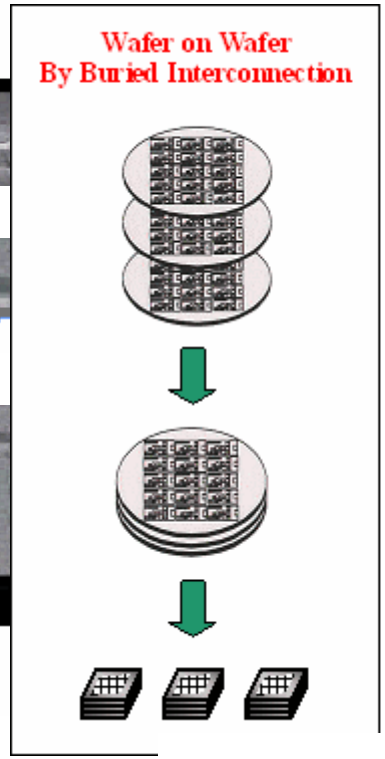
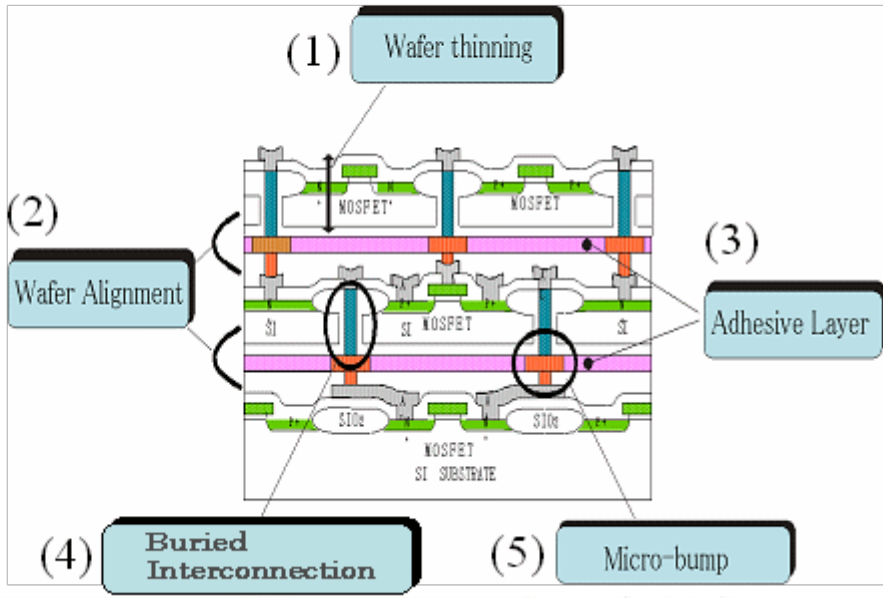
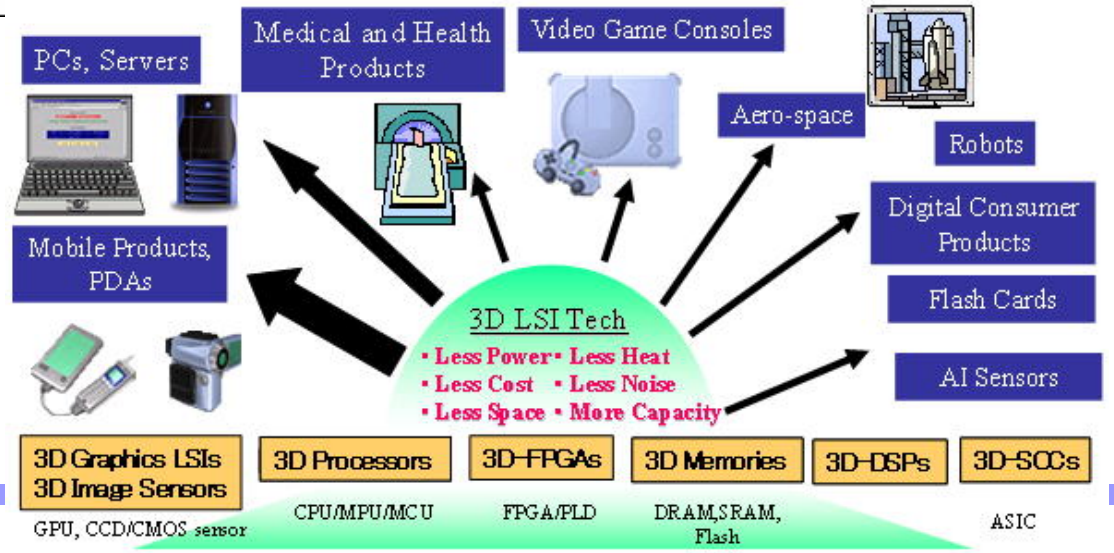
Through substrate via (TSV)





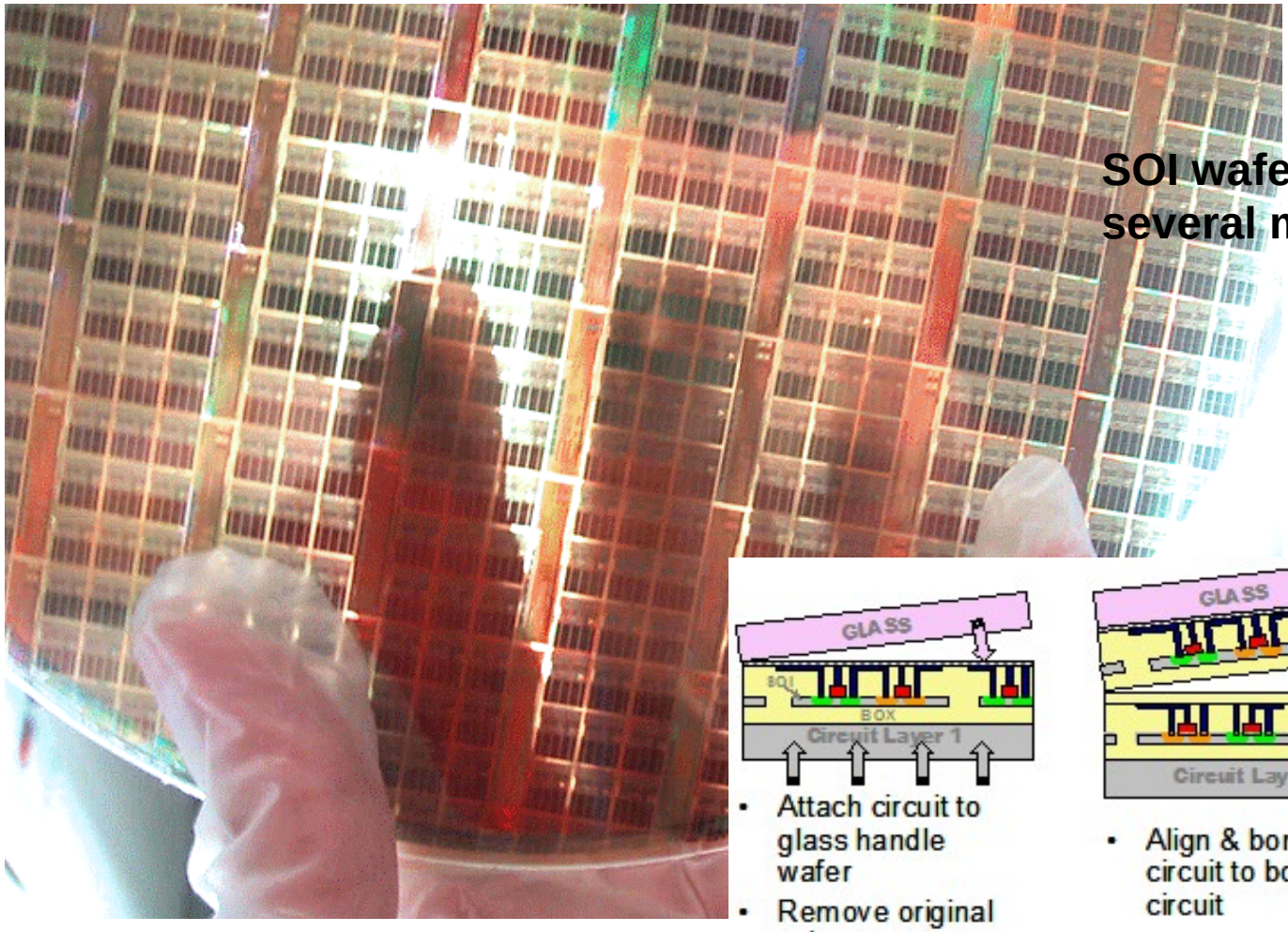






By ZyCube

3D wafer stacking for high performance

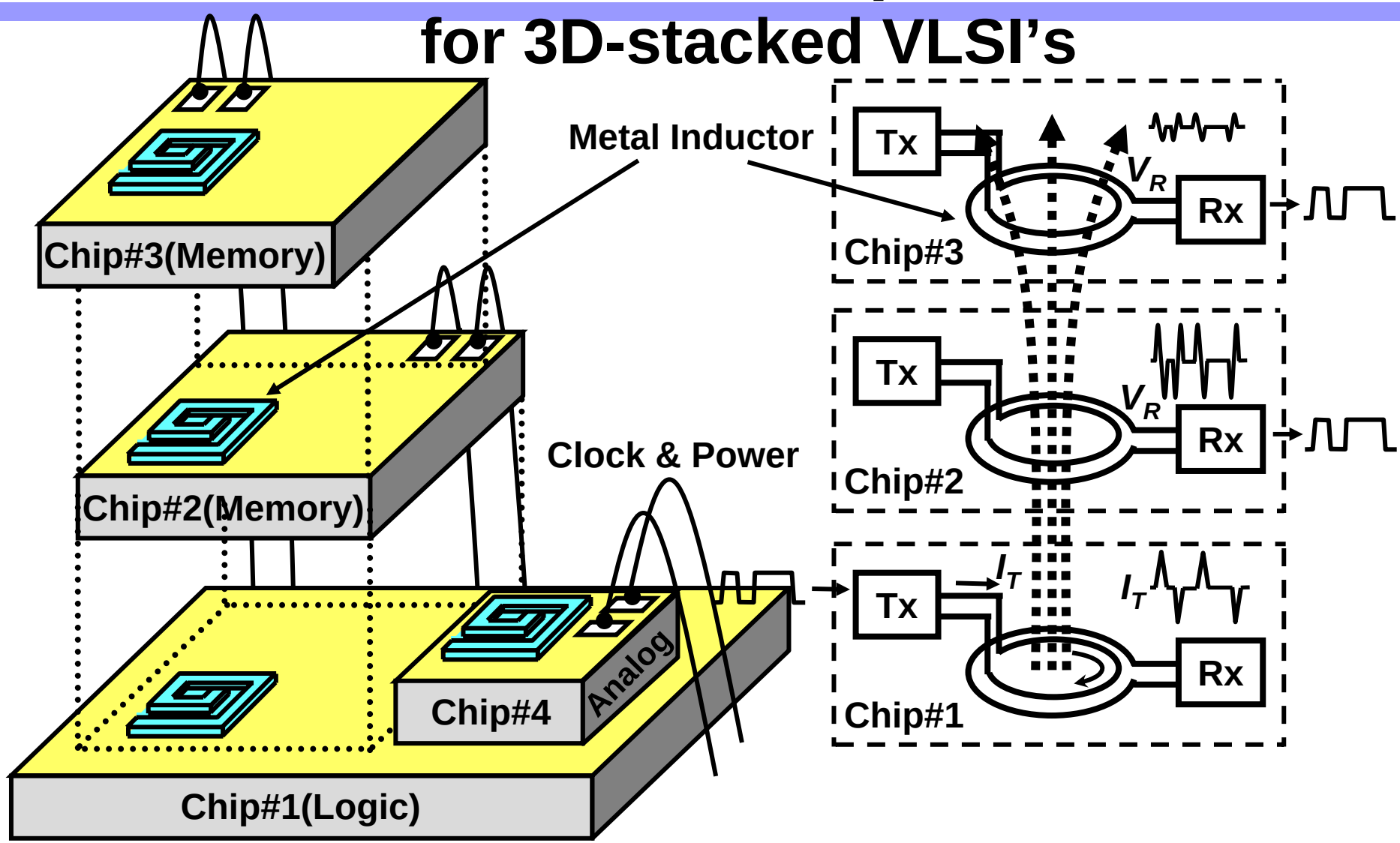


SOI wafer is thinned down to several microns.

Via size is 0.2 microns diameter at the top, and 0.14 microns at the bottom.

Courtesy of Kerry Bernstein, IBM T.J. Watson Research Center **T.Sakurai**

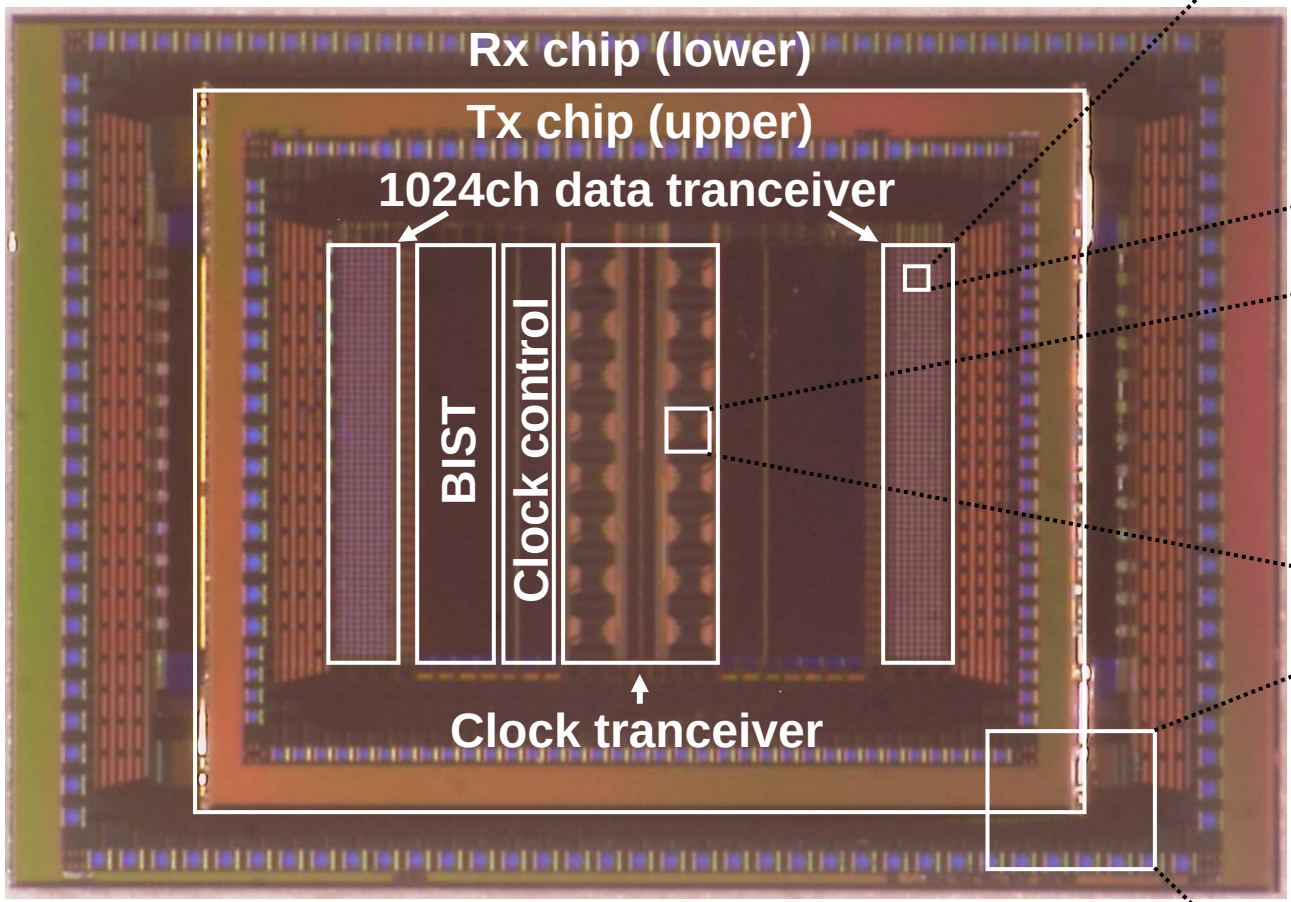
Inductive wireless superconnect for 3D-stacked VLSI's



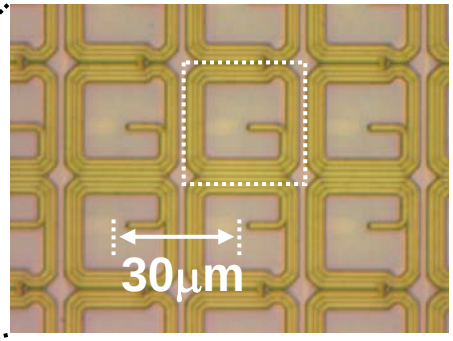
D. Mizoguchi, Y. Yusof, N. Miura, T. Sakurai, T. Kuroda, "A 1.2Gb/s/pin Wireless Superconnectbased on Inductive Inter-chip Signaling (IIS) ,"ISSCC'04, pp. 142-143, Feb. 2004. N. Miura, D. Mizoguchi, Y. B. Yusof, T. Sakurai, and T. Kuroda, "Analysis and Design of Transceiver Circuit and Inductor Layout for Inductive Inter-chip Wireless Superconnect,"*Symp. on VLSI Circuits*, pp. 246-249 June 2004.

1Tbps inter-chip wireless by 30μm coils

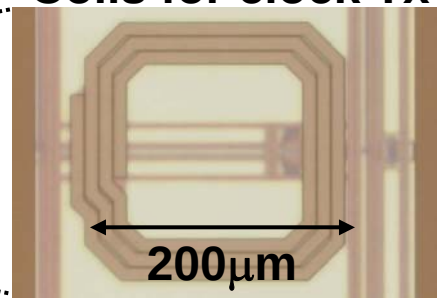
Low-loss interconnects are preferable for micro transformers.



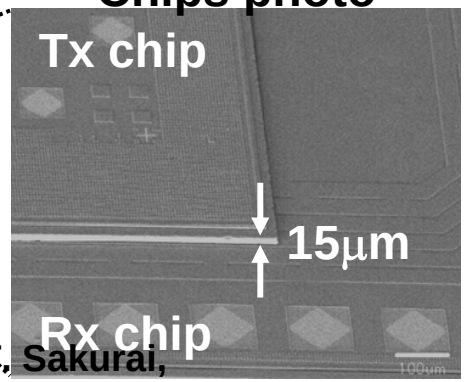
Coils for data Tx



Coils for clock Tx



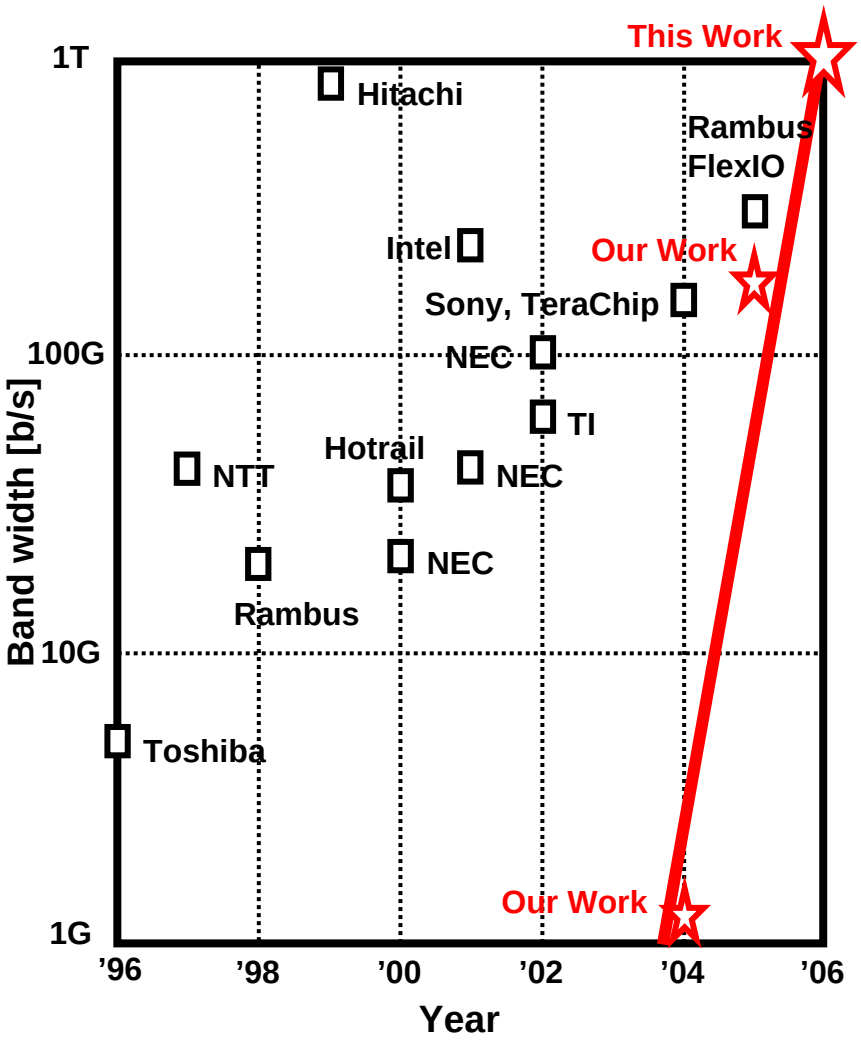
Chips photo

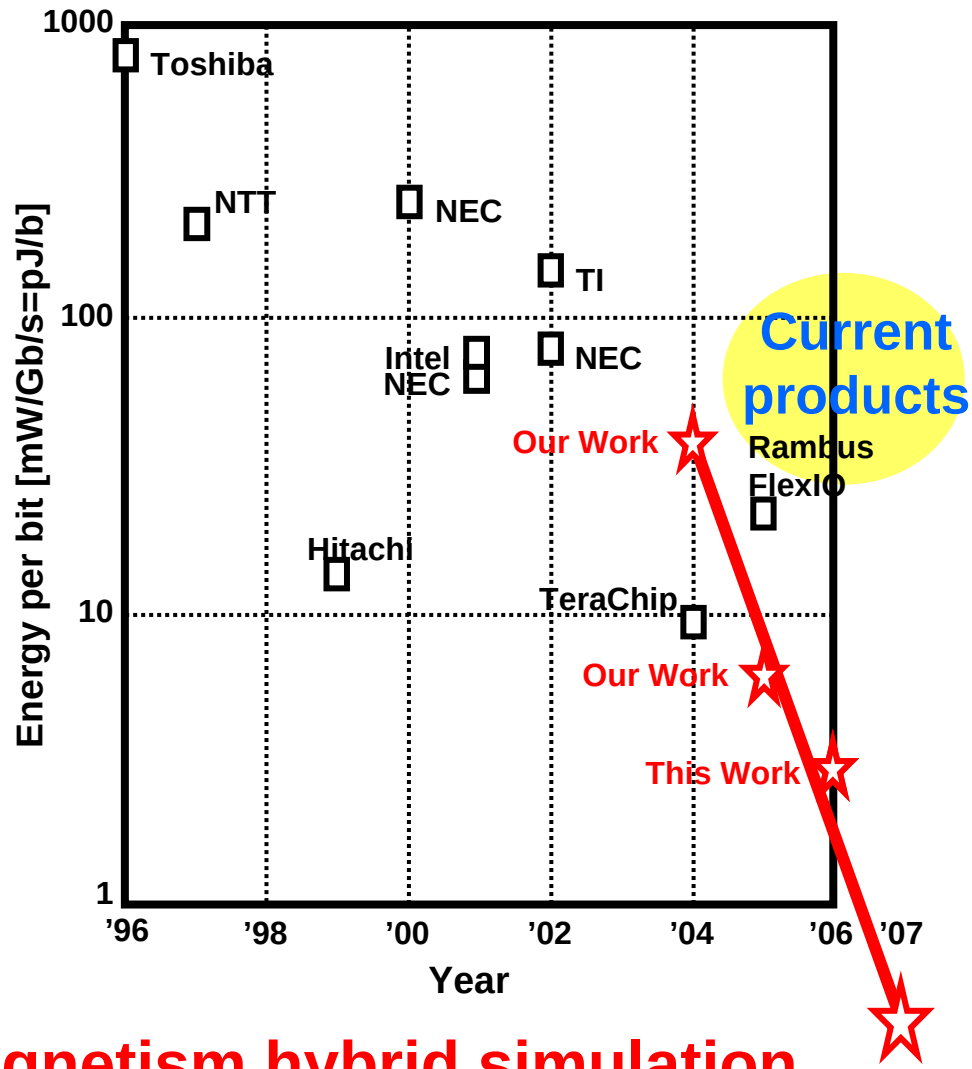


0.18μm CMOS, 3fJ/bit energy

N.Miura, D.Mizoguchi, M.Inoue, K.Niitsu, Y.Nakagawa, M.Tago, M.Fukaishi, T. Sakurai, T. Kuroda, "A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link," ISSCC'06, Paper#23.4, Feb. 2006.

Inductively-coupled inter-chip communication



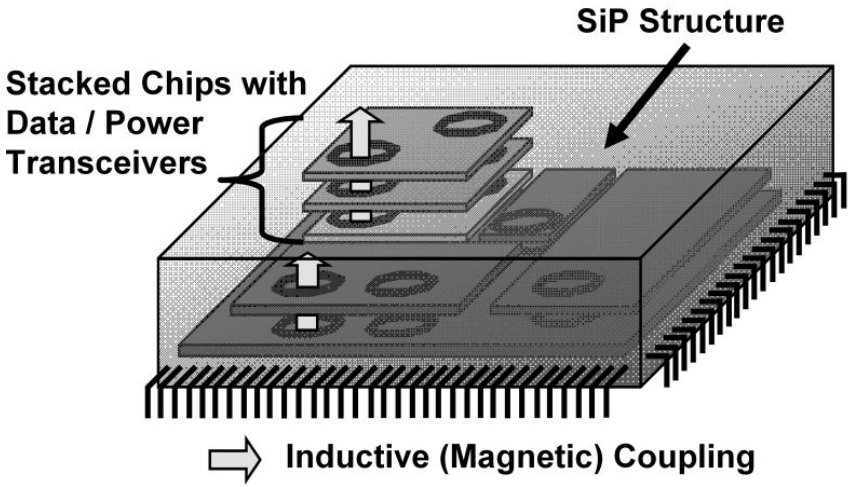


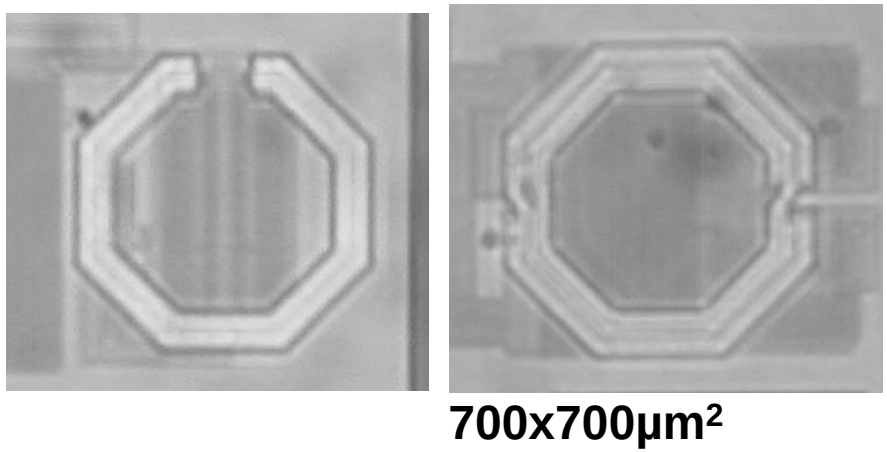
Circuits and electro-magnetism hybrid simulation.

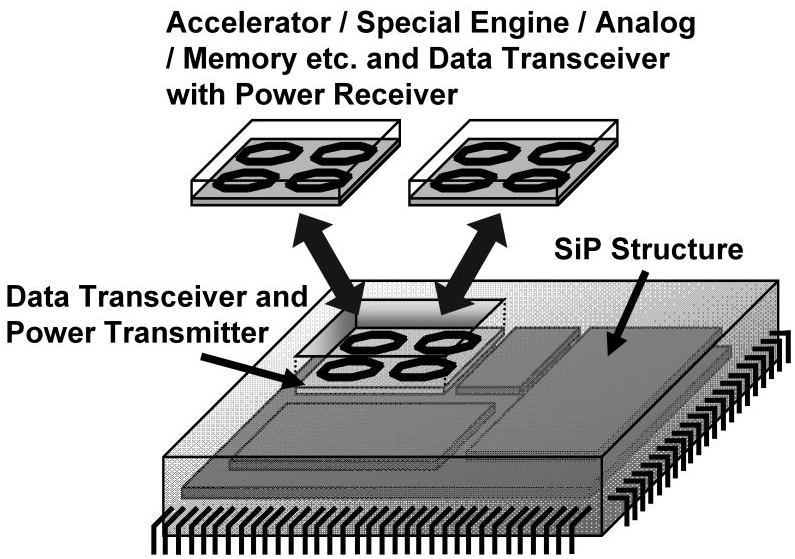
N.Miura, H.Ishikuro, T.Sakurai, T.Kuroda, "A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping," Paper#20.2, ISSCC, Feb.2007.

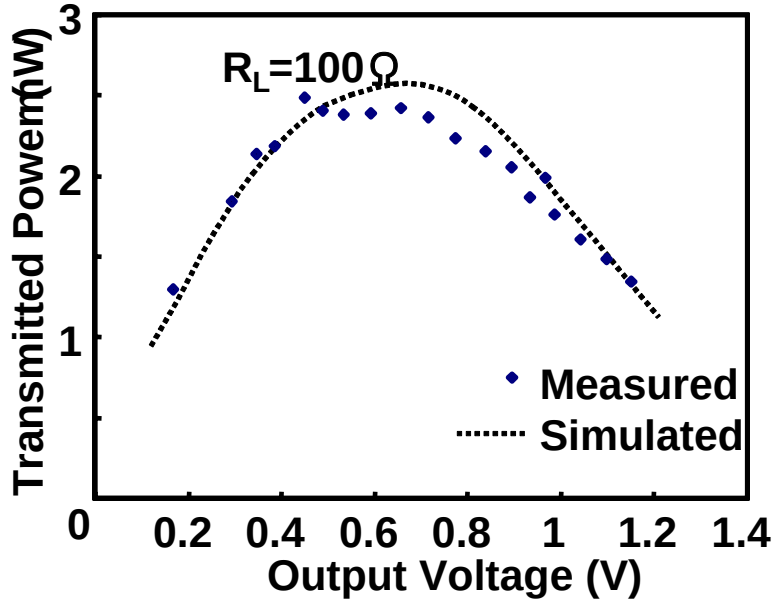
T.Sakurai

Even wireless power transmission



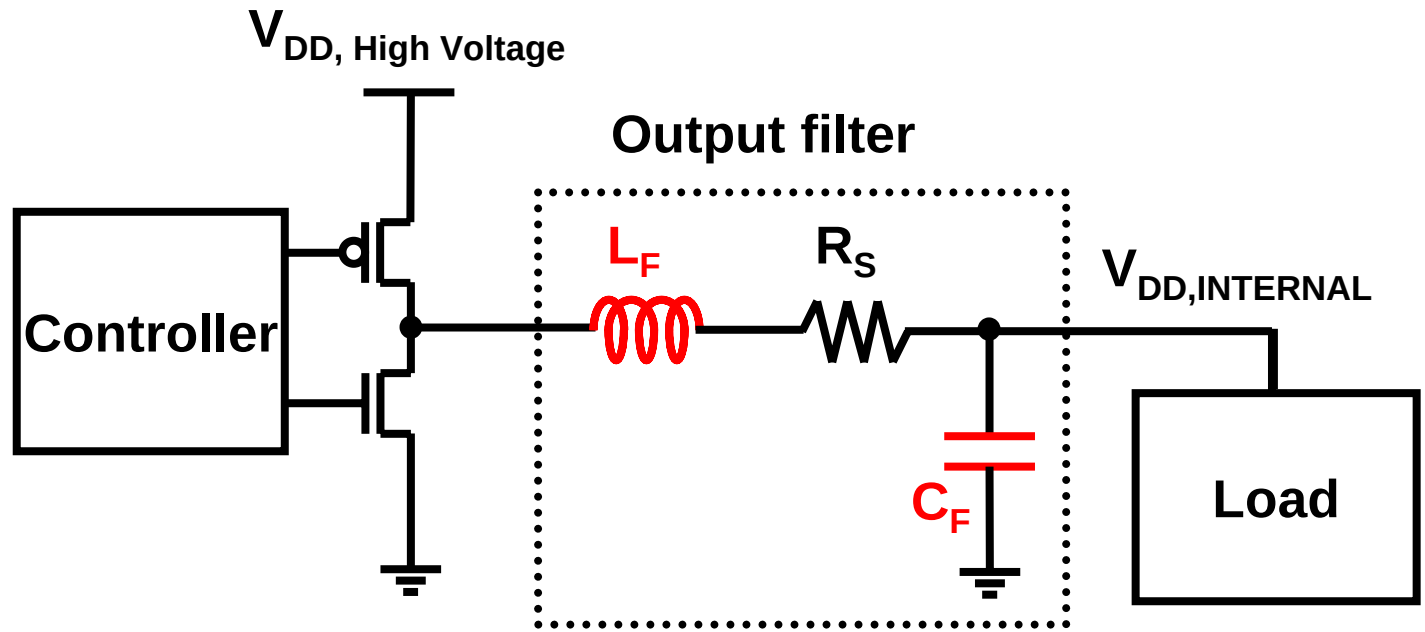






K.Onizuka, H. Kawaguchi, M. Takamiya, T. Kuroda and T. Sakurai, “Chip-to-Chip Inductive Wireless Power Transmission System for SiP Applications,”Paper#15.1, CICC, Sept. 2006.

On-chip distributed DC-DC converter

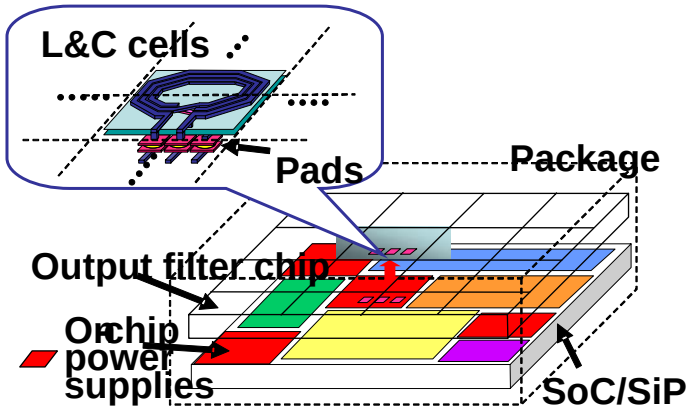


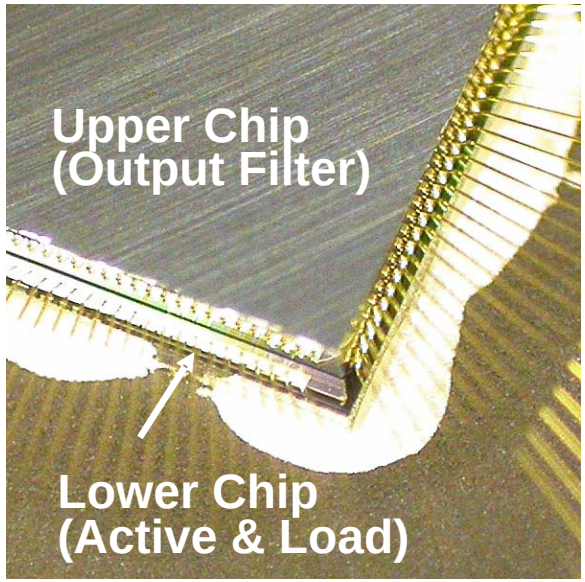
Chopping frequency > 300MHz

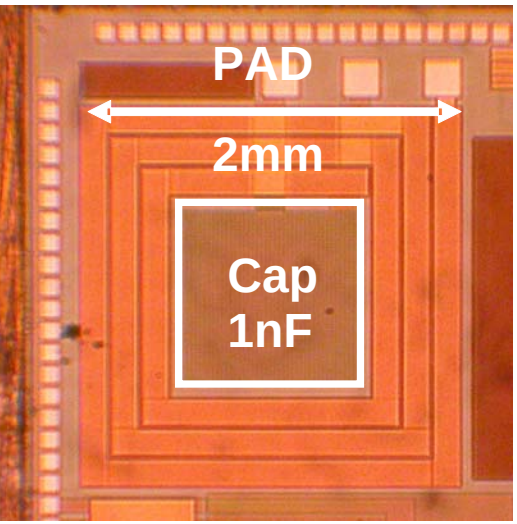
Need good low-resistive L & high-capacitive C.
They are also needed for low-power RF circuits.

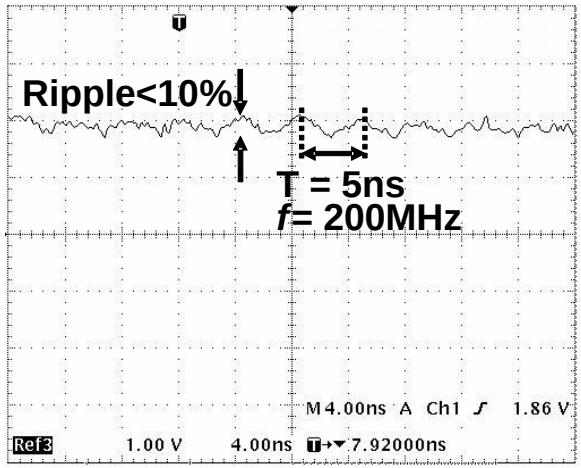
➔ Si with L and C

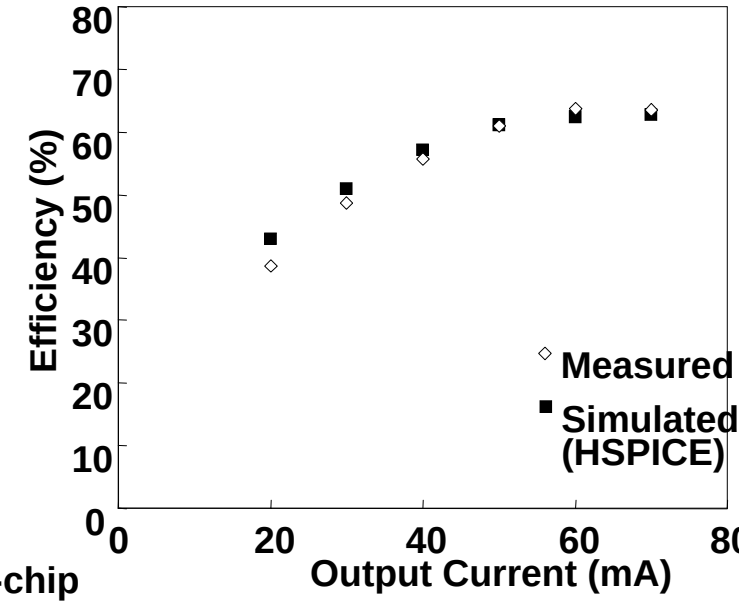
Distributed DC-DC converter by 3D stacking





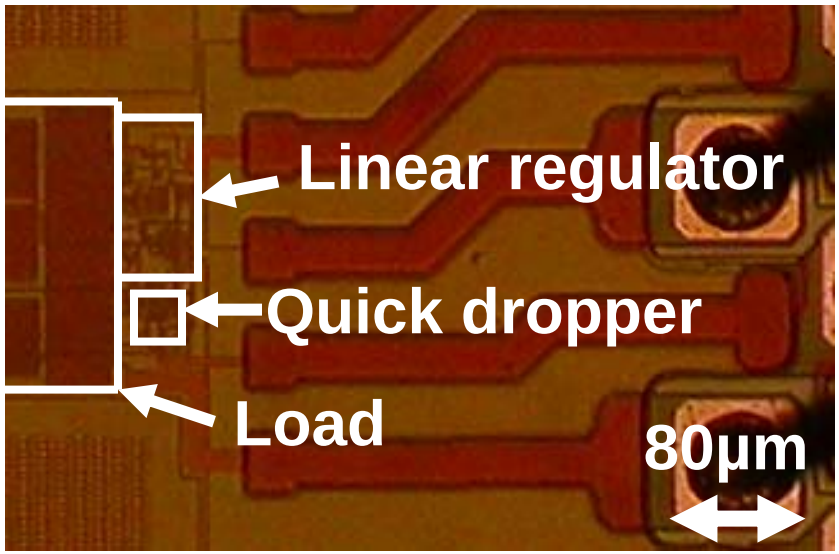




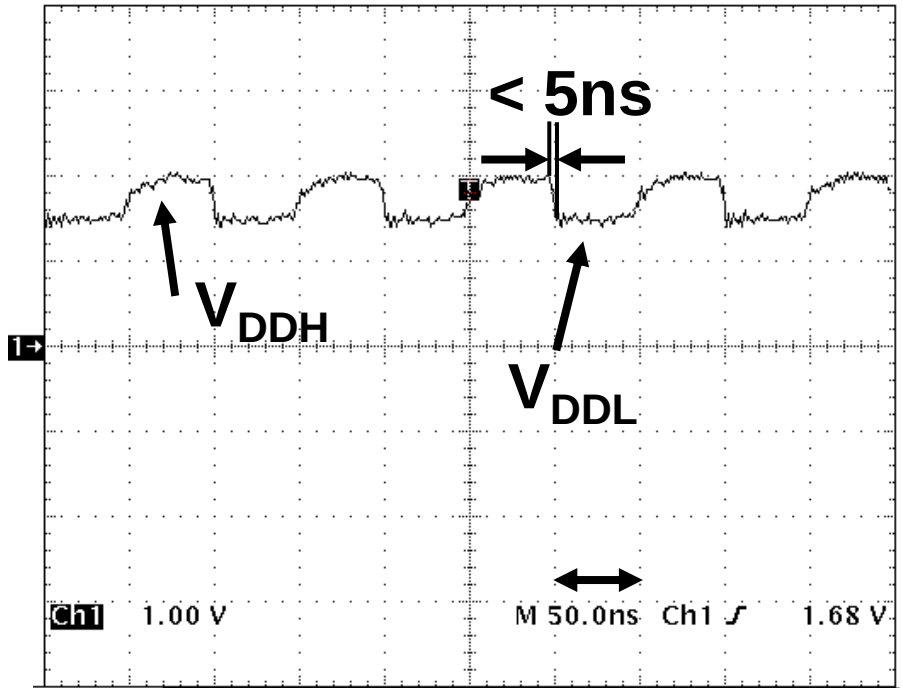


K.Onizuka, H. Kawaguchi, M. Takamiya, and T. Sakurai, “Stacked-chip Implementation of On-Chip Buck Converter for Power-Aware Distributed Power Supply Systems,” A-SSCC, Nov. 2006.

5ns transition on-chip power supply



Measurement



For 25k-gates equivalent load

@ 0.18μm CMOS

Transition time smaller than 5ns

K.Onizuka and T.Sakurai, "VDD-Hopping Accelerator for On-Chip Power Supplies Achieving Nano-Second Order Transient Time," A-SSCC'05, Paper#6.1, Nov. 2005.

3D Stacking for solving issues

- **Silicon chips stacking**

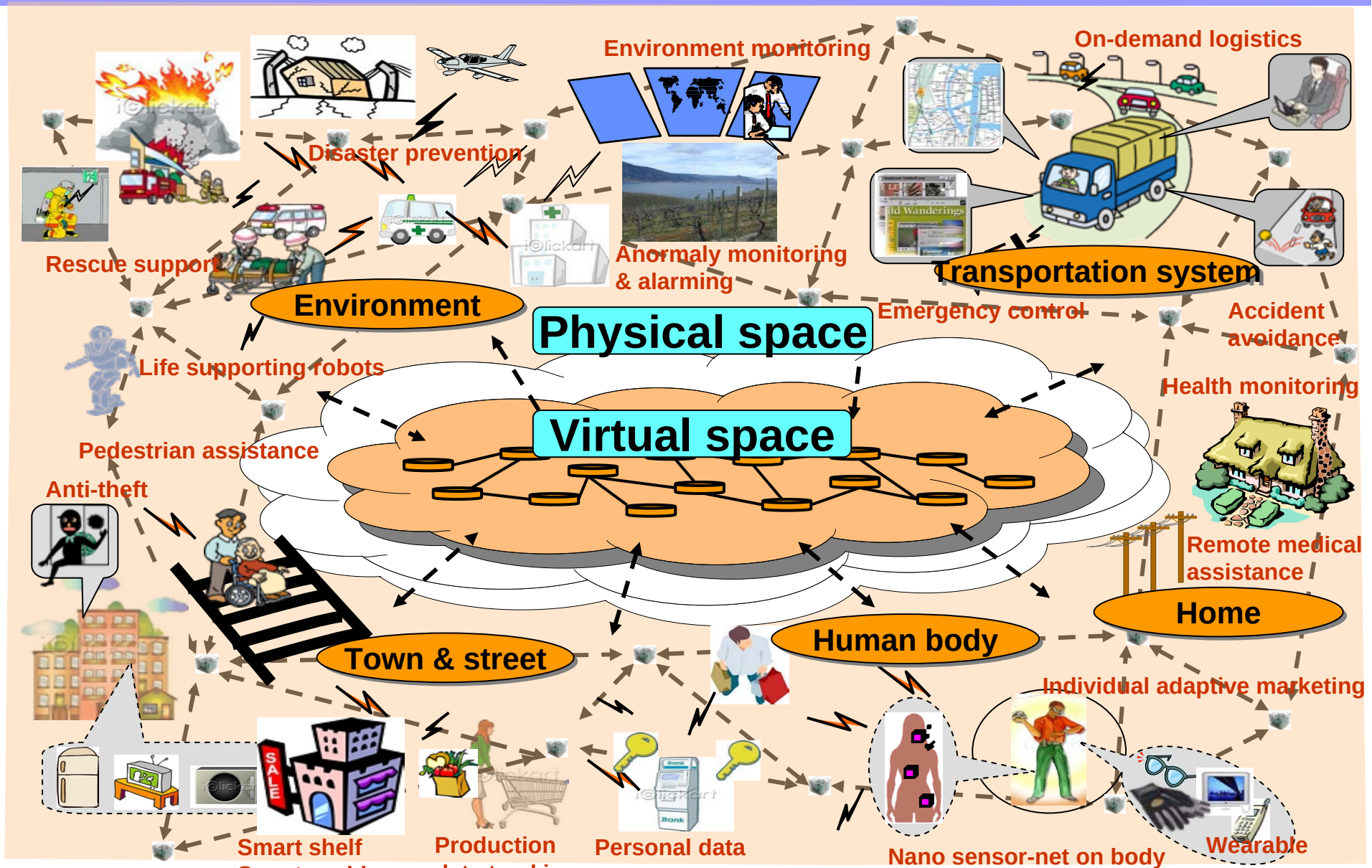
  for lower power & lower NRE

- **Organic sheets stacking**

  for newer applications

With design tool implications

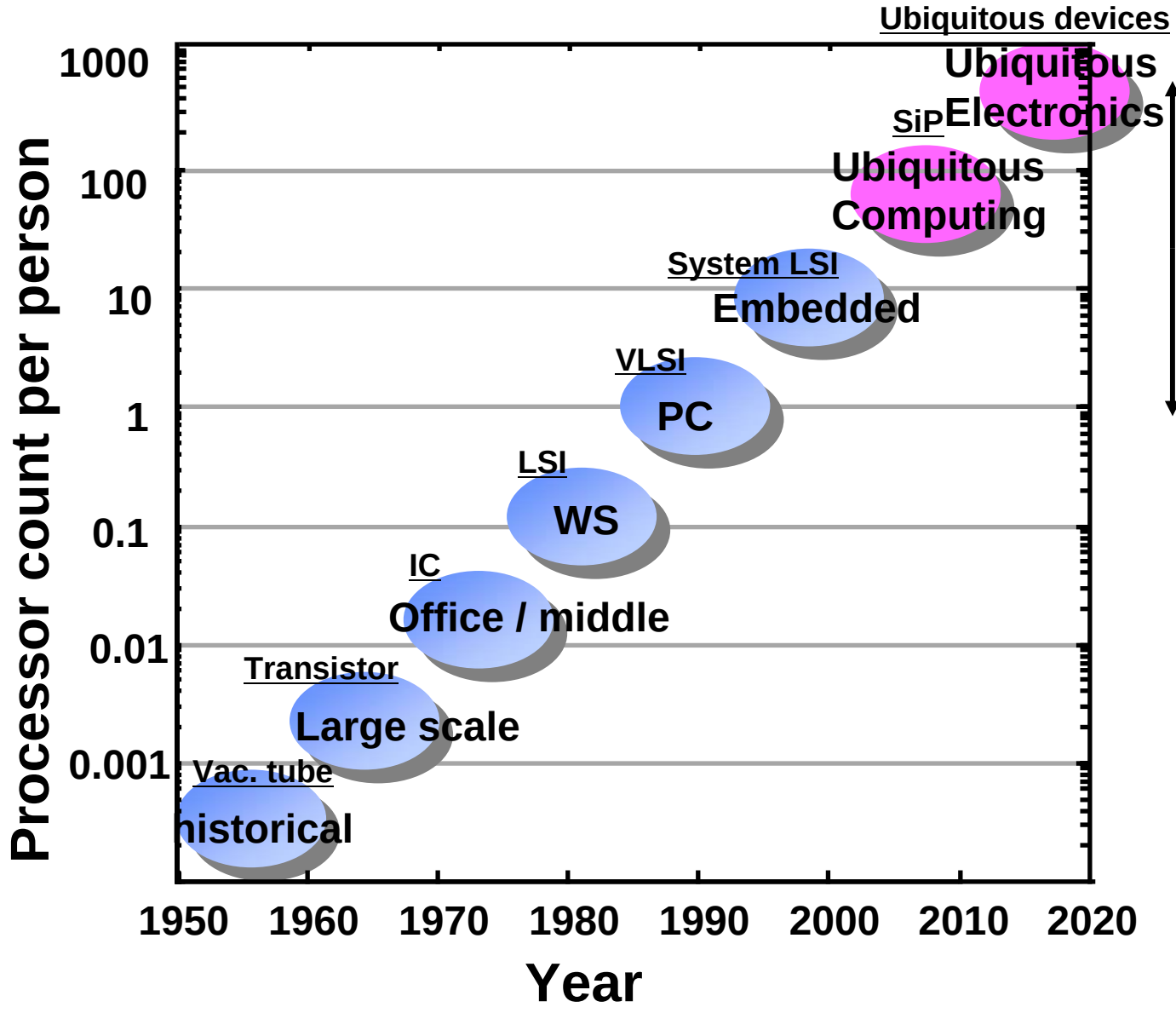
New electronics targets physical space



Original drawing: Courtesy of Prof. Morikawa, Univ. of Tokyo

T.Sakurai

Increasing VLSI penetration into people's life

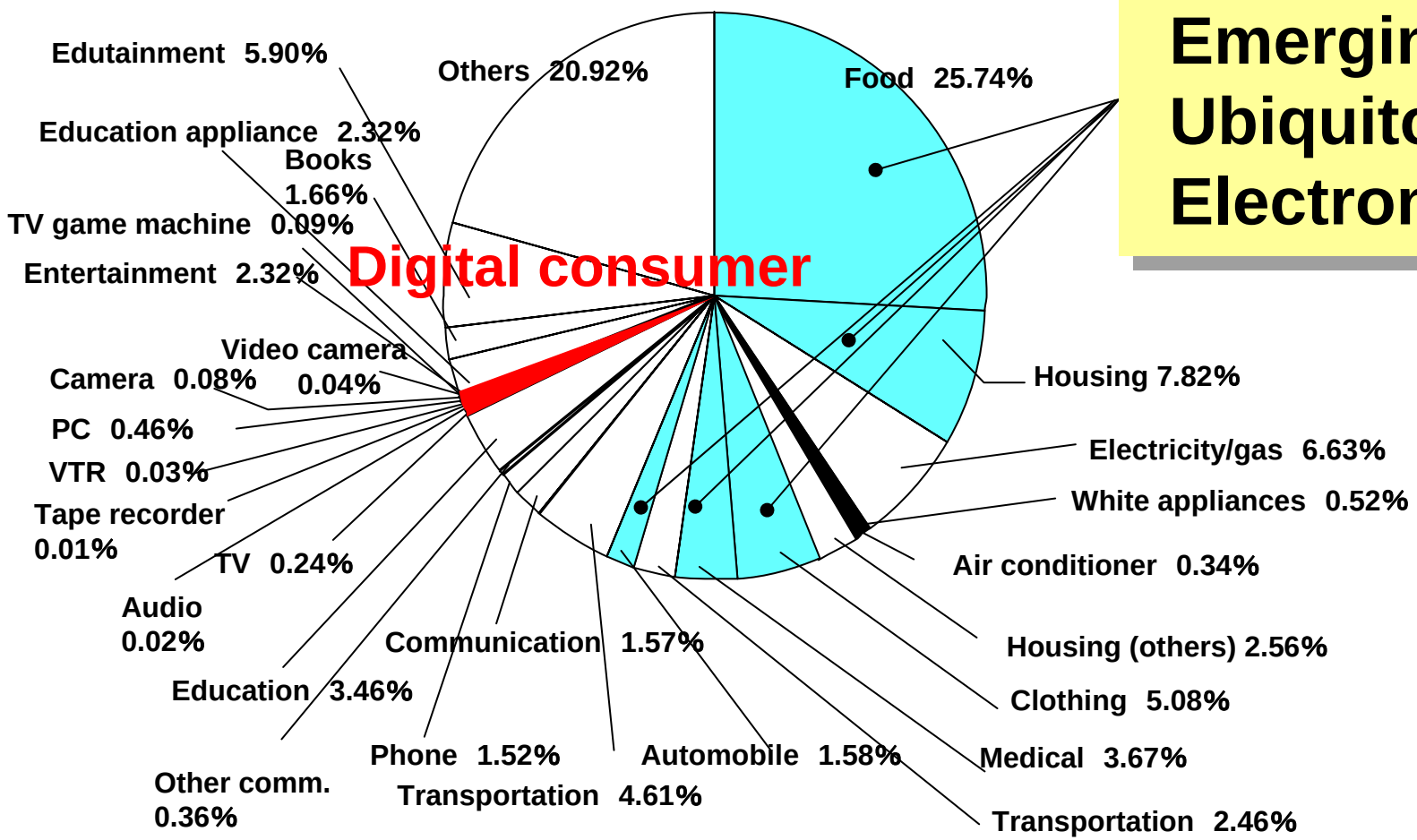


Electronics is part of environments enhancing convenience and security of daily life.

People use electronics consciously.

T.Sakurai

Expenditure distribution of Japanese household



Emerging App.: Ubiquitous Electronics

Ubiquitous electronics is required to provide physical applications.

Required innovations for ubiquitous electronics

Huge number of devices

- ➔Extremely low power (3D SiP)
- ➔Low cost (3D SiP)

Everywhere

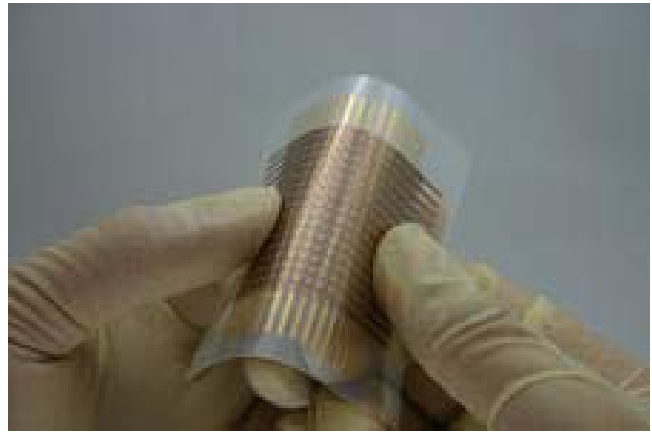
- ➔Very short distance communication (L & C stacked)
- ➔Ubiquitous energy source (Large-area electronics)

Interfaces to real-world

- ➔Sensors & actuators (Large-area electronics)
- ➔Heterogeneous systems (Heterogeneous ICs stack)

Design tool needs for 3D hybrid systems synthesis and simulation

Features of organic IC's



- **Advantages**

  Low-cost manufacturing
  Mechanical flexibility

- **Disadvantages**

  Low speed (<10^{-5} of Si VLSI)
  Low density (<10^{-4} of Si VLSI)

Organic electronics

Flat Panel Display

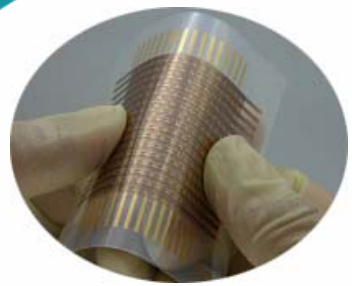
Samsung

Flexible Displays

Polymer Vision

Gyricon

Kennedy group



Smart Cards

Infineon

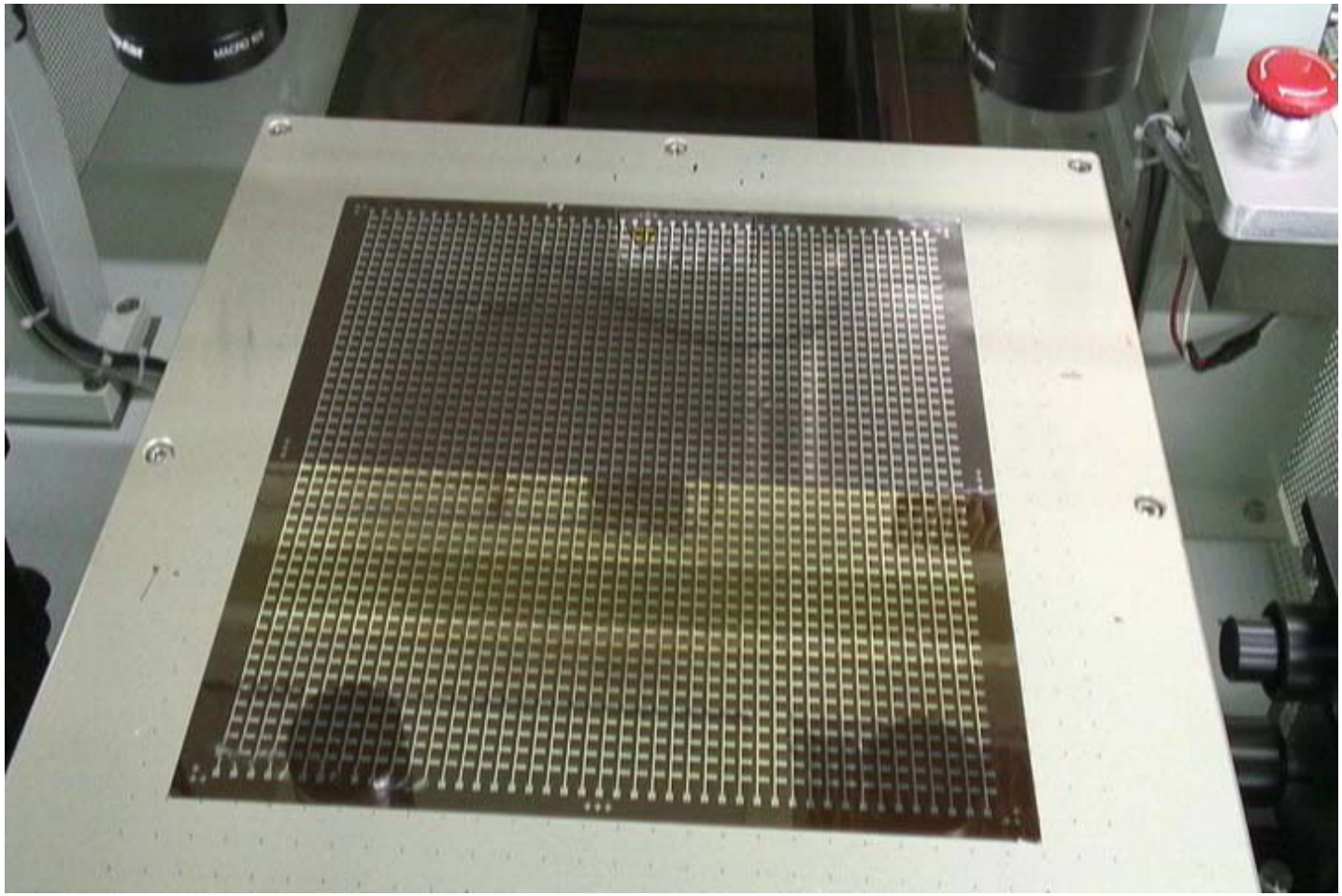
University of Tokyo

Pioneer

Studio Del Sole

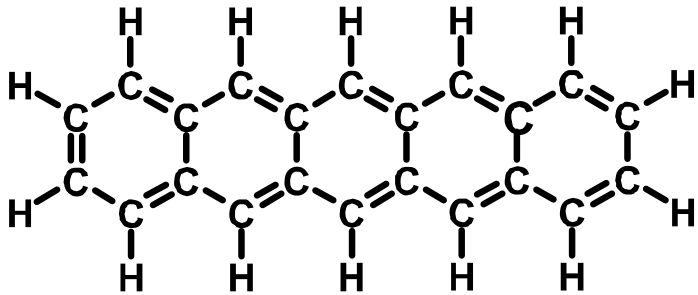
T.Sakurai

Printable electronics

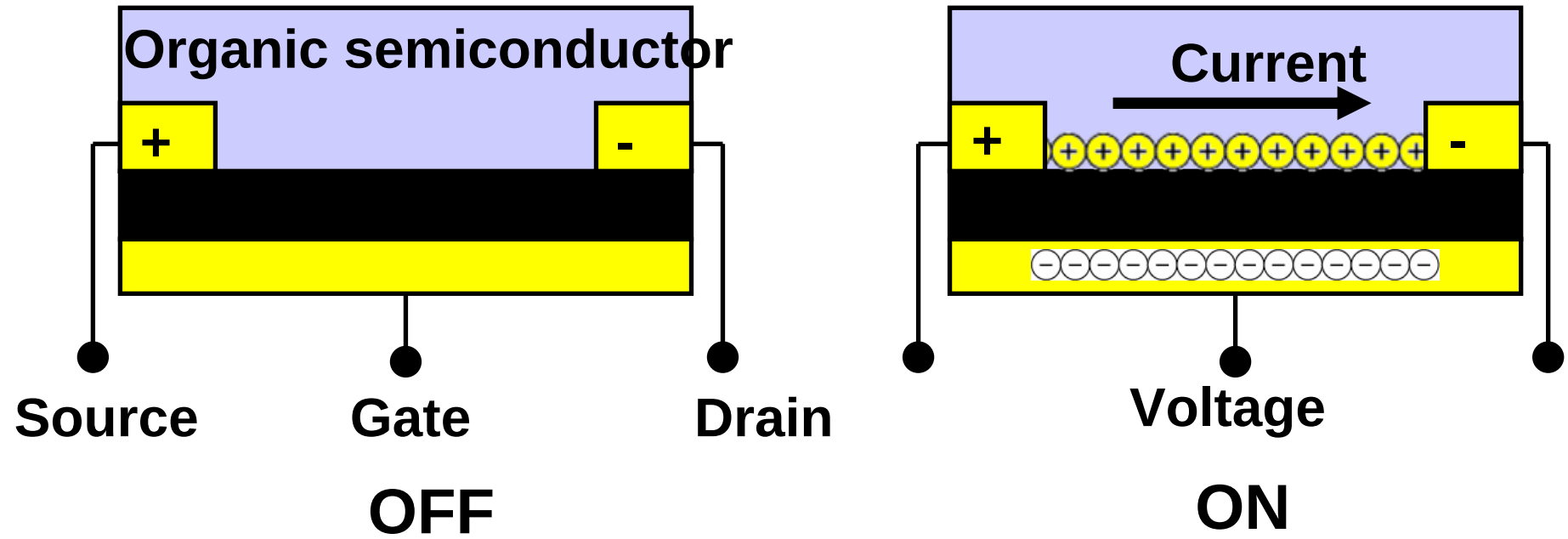


Organic transistors

Organic semiconductors: main elements --- C & H
Slow but flexible and low-cost manufacturing

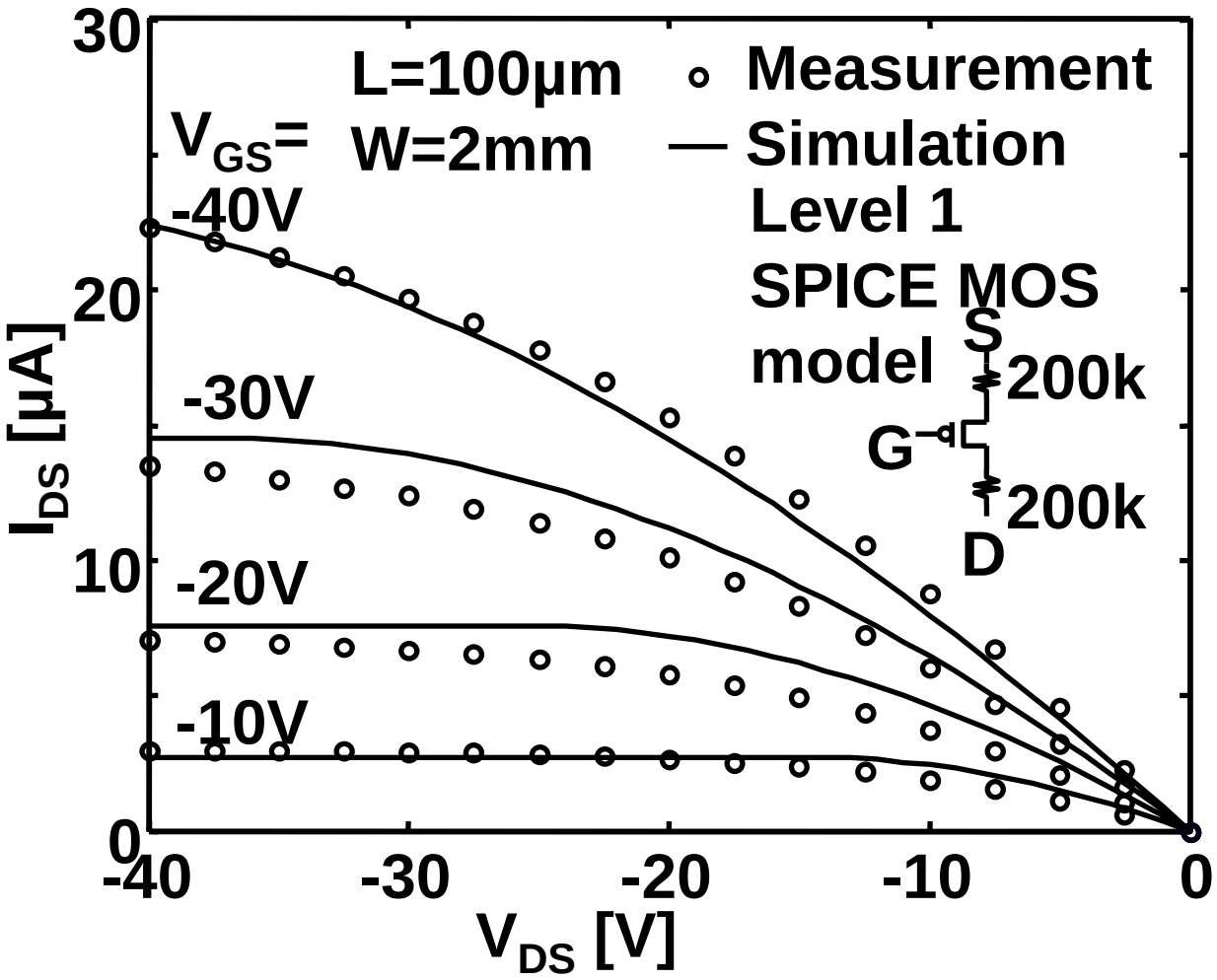


Pentacene



SPICE still works

- Match level 1 SPICE MOS model with 200kΩ



Mobility
0.5 ~ 1.4cm²/Vs
Ion/Ioff >10⁶

Bending proof

Preferably new model like $\mu \propto (V_{GS}-V_{TH})^{\gamma}$ $(0<\gamma<1)$

Large-area electronics by stacked sheets

Slow but low-cost for large-area (Si can't cover)

Braille display

E-skin

Sheet scanner

IEDM'03
ISSCC'04
Pressure sensors + OFETs

IEDM'04
ISSCC'05
Photodetectors + OFETs

IEDM'05
ISSCC'06
Actuators + OFETs

IEDM'06
ISSCC'07
Coils + MEMS + OFETs

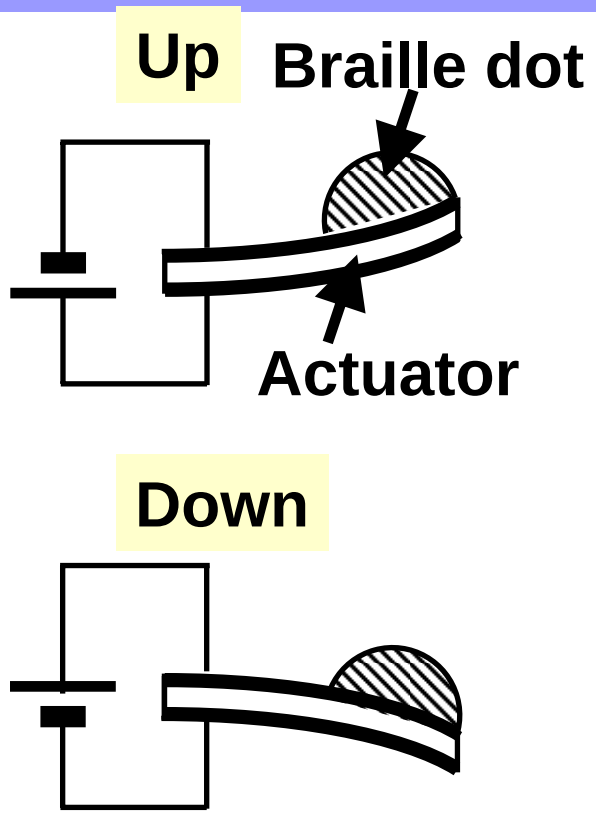
T.Sakurai

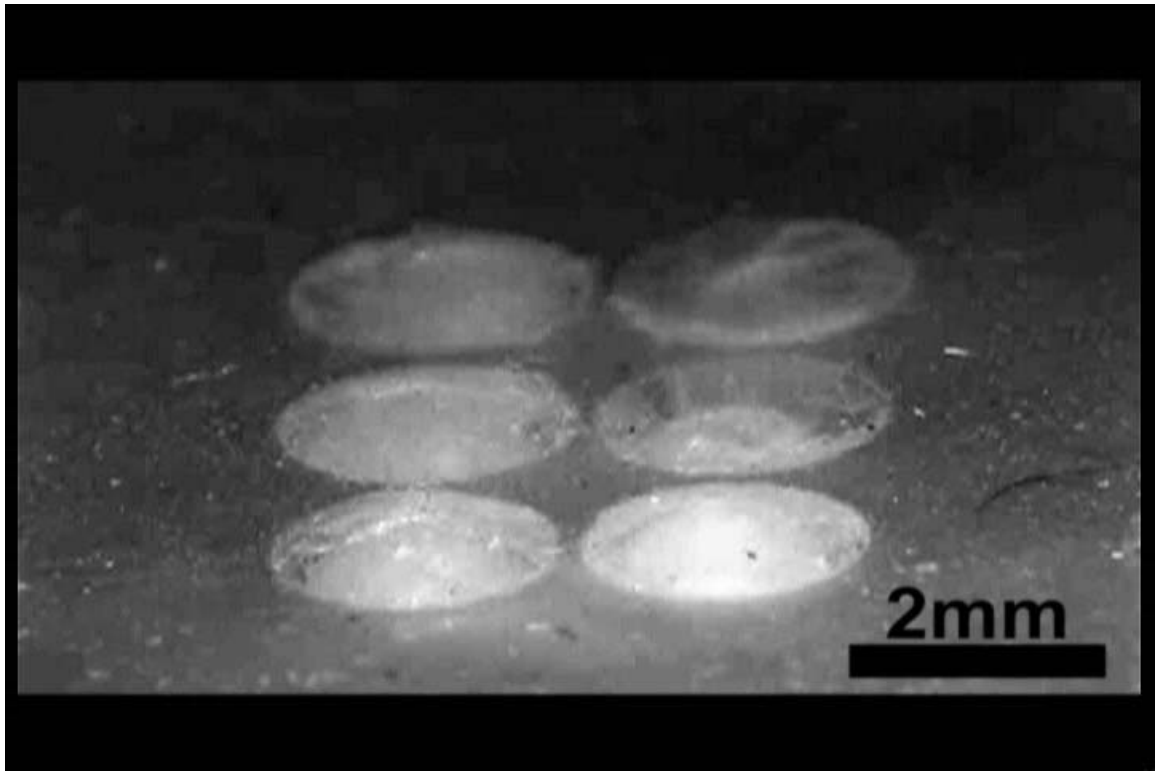
Braille display by organic FETs

Y.Kato, S.Iba, T.Sekitani, Y.Noguchi, K.Hizu, X.Wang, K.Takenoshita, Y.Takamatsu, S.Nakano, K.Fukuda, K.Nakamura, T.Yamaue, M.Doi, K.Asaka, H.Kawaguchi, M.Takamiya, T.Sakurai, and T.Someya, "A Flexible, Lightweight Braille Sheet Display with Plastic Actuators Driven by An Organic Field-Effect Transistor Active Matrix," IEDM'05, Paper #5.1, Dec.2005.

M.Takamiya, T.Sekitani, Y.Kato, H.Kawaguchi, T.Someya, and T.Sakurai, “An Organic FET SRAM for Braille sheet display with back gate to increase the static noise margin,” ISSCC’06, Paper #15.4, Feb. 2005.

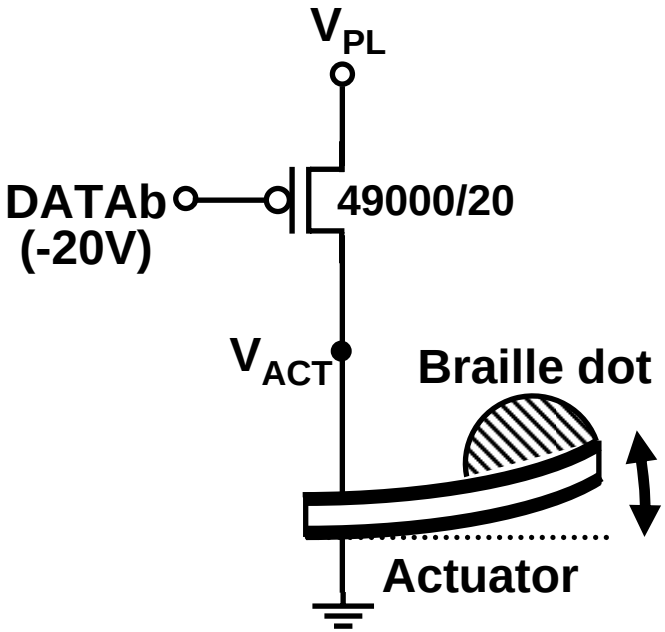
Plastic actuators

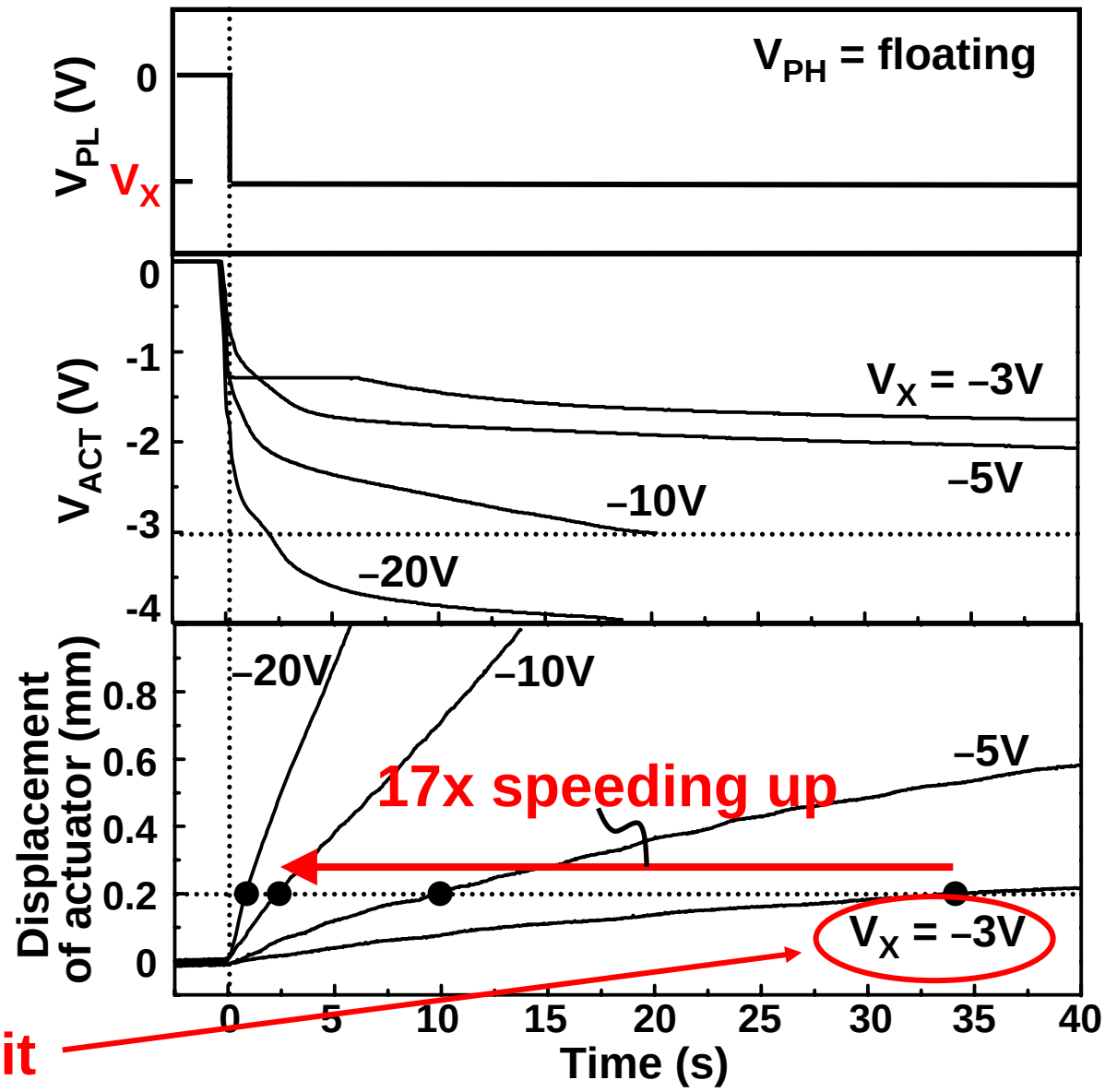




- The displacement of the actuators to read Braille is 0.2 mm.

Speed up by higher-voltage drive





Reliability limit

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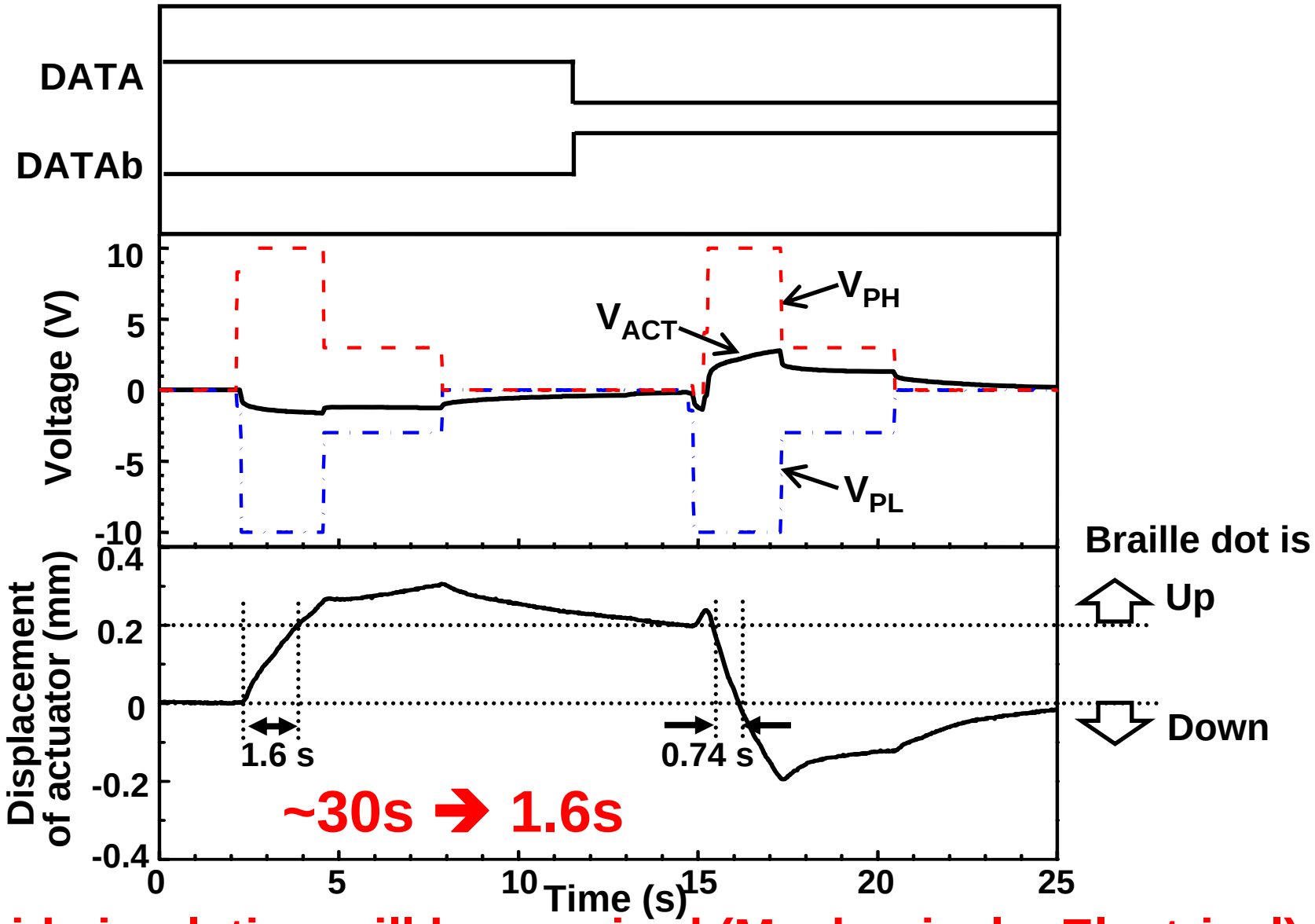
Overdrive for speed and reliability



Hybrid simulation will be required (Mechanical – Electrical)

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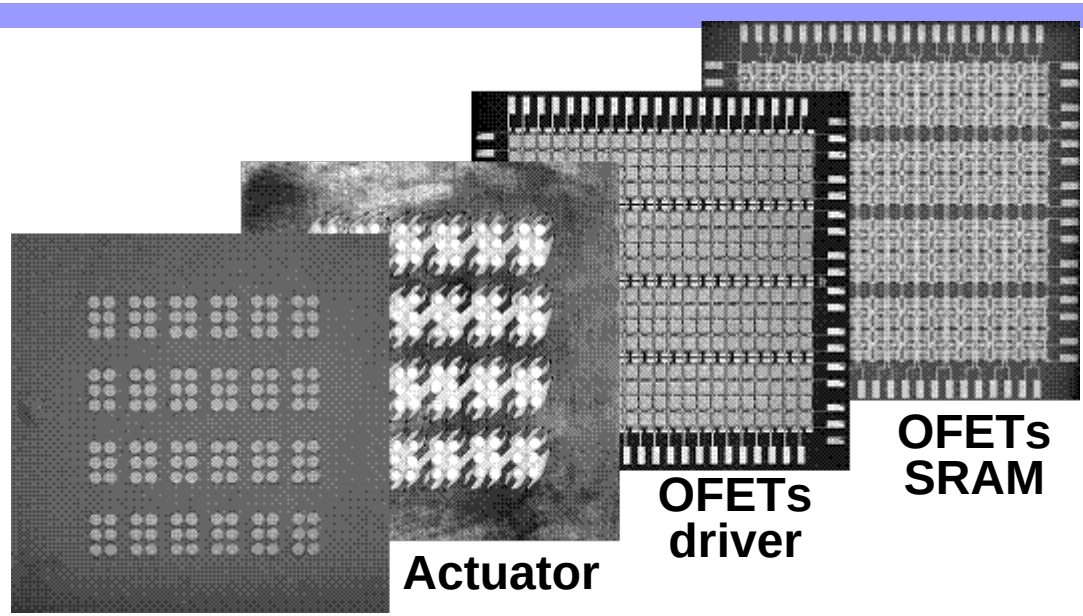
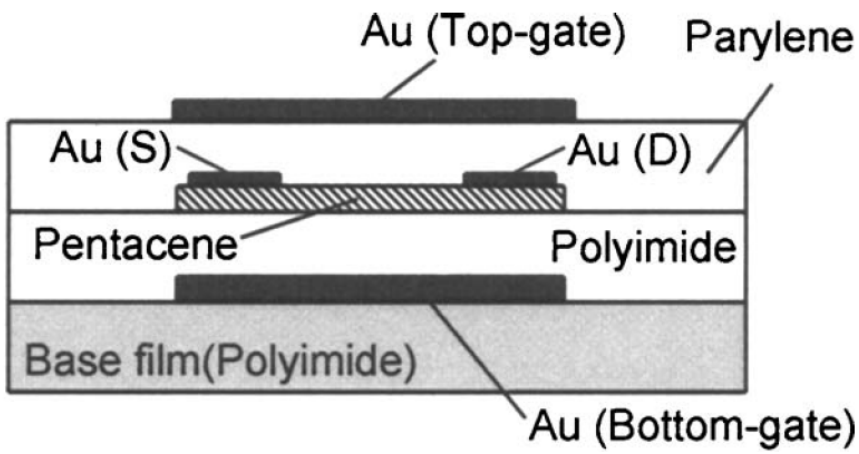
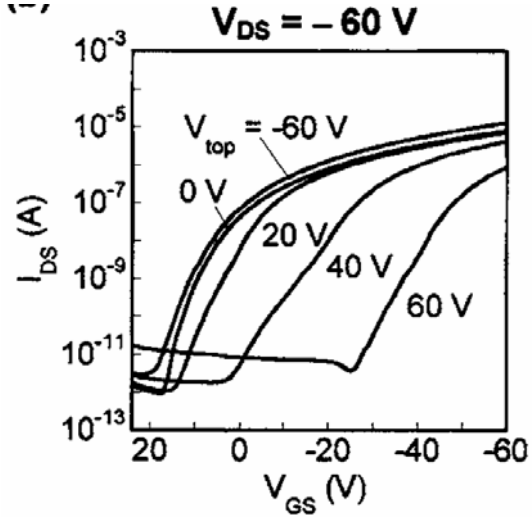
Braille sheet display stacking four sheets

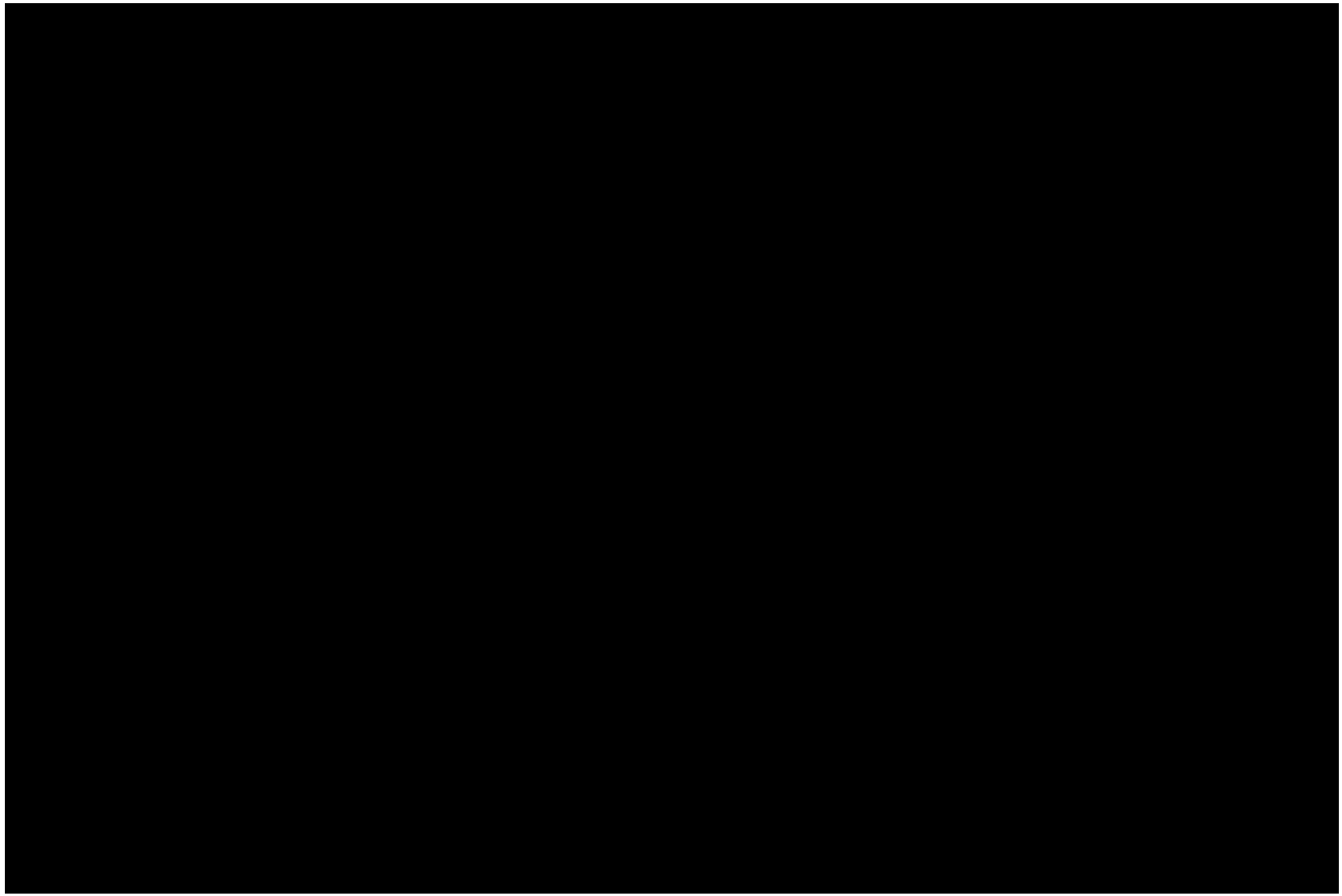






M.Takamiya, T.Sekitani, Y.Kato, H.Kawaguchi, T.Someya, and T. Sakurai, "An Organic FET SRAM for Braille Sheet Display with Back Gate to Increase Static Noise Margin," ISSCC'06, Paper#15.4, Feb. 2006.

Braille reading test



All of 4 blind subjects can read our Braille correctly.

Wireless power transmission sheet with plastic MEMS switches and OFETs

T.Sekitani, M.Takamiya, Y.Noguchi, S.Nakano, Y.Kato, K.Hizu, H.Kawaguchi, T.Sakurai, and T.Someya, "A large-area flexible wireless power transmission sheet using printed plastic MEMS switches and organic field-effect transistors," Paper#11.1, IEDM 2006, Dec. 2006.

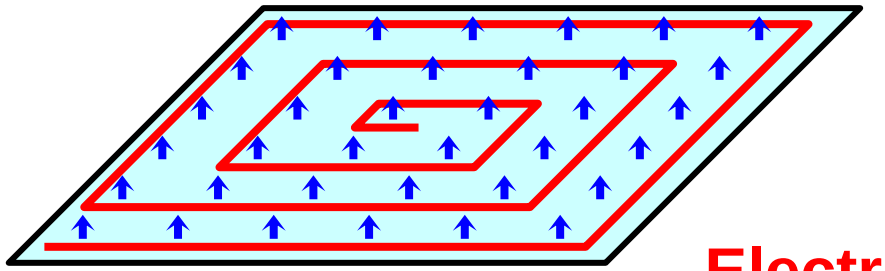
M.Takamiya, T.Sekitani, Y.Miyamoto, Y.Noguchi, H.Kawaguchi, T.Someya and T.Sakurai, "Design Solutions for a Multi-Object Wireless Power Transmission Sheet Based on Plastic Switches," Paper#20.4, ISSCC, Feb. 2007.

Position-sensing and selective activation

Large coil

Receiver coil

1 inch²



30x30 cm² X 1 coil

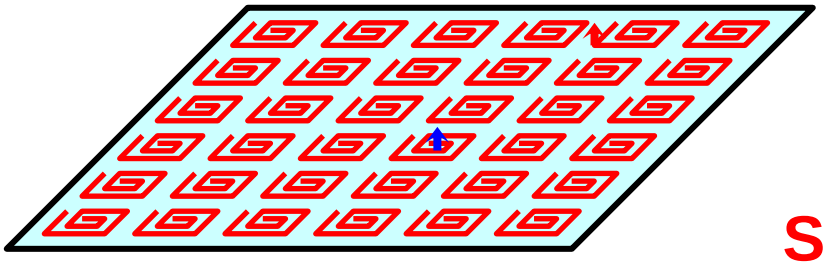
Efficiency ~ 0.1%

Electro- magnetic induction works

Many coils & one selected

Receiver coil

1 inch²

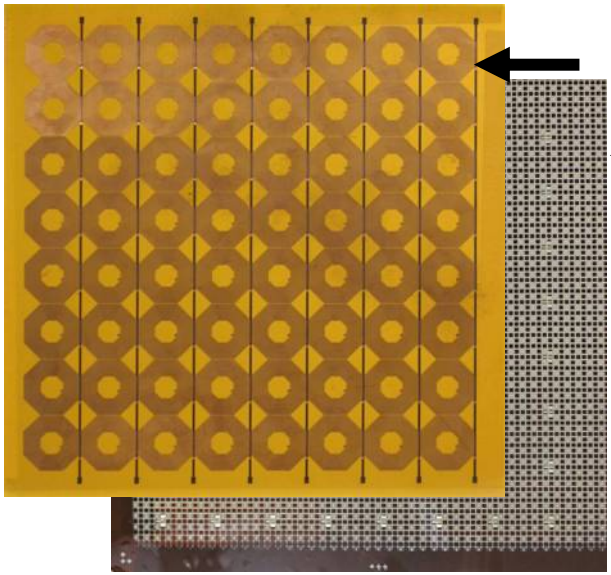


1 inch² X 64 coils

Efficiency > 60%

Selective activation is the key.

Stacking sheets for MEMS and Organic FETs



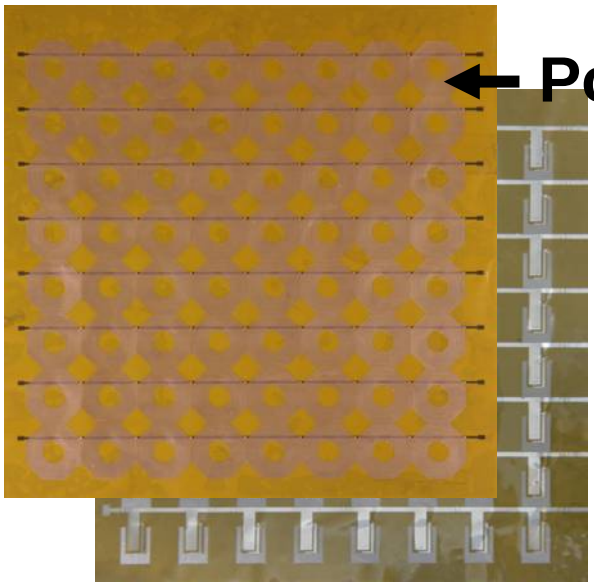
Position-sensing coils

Organic FETs

Resistive
Faster < ms
# of switching unlimited

Contactless position-sensing system

21 x 21 cm^2 (8 x 8 cells)



Power transmission coils

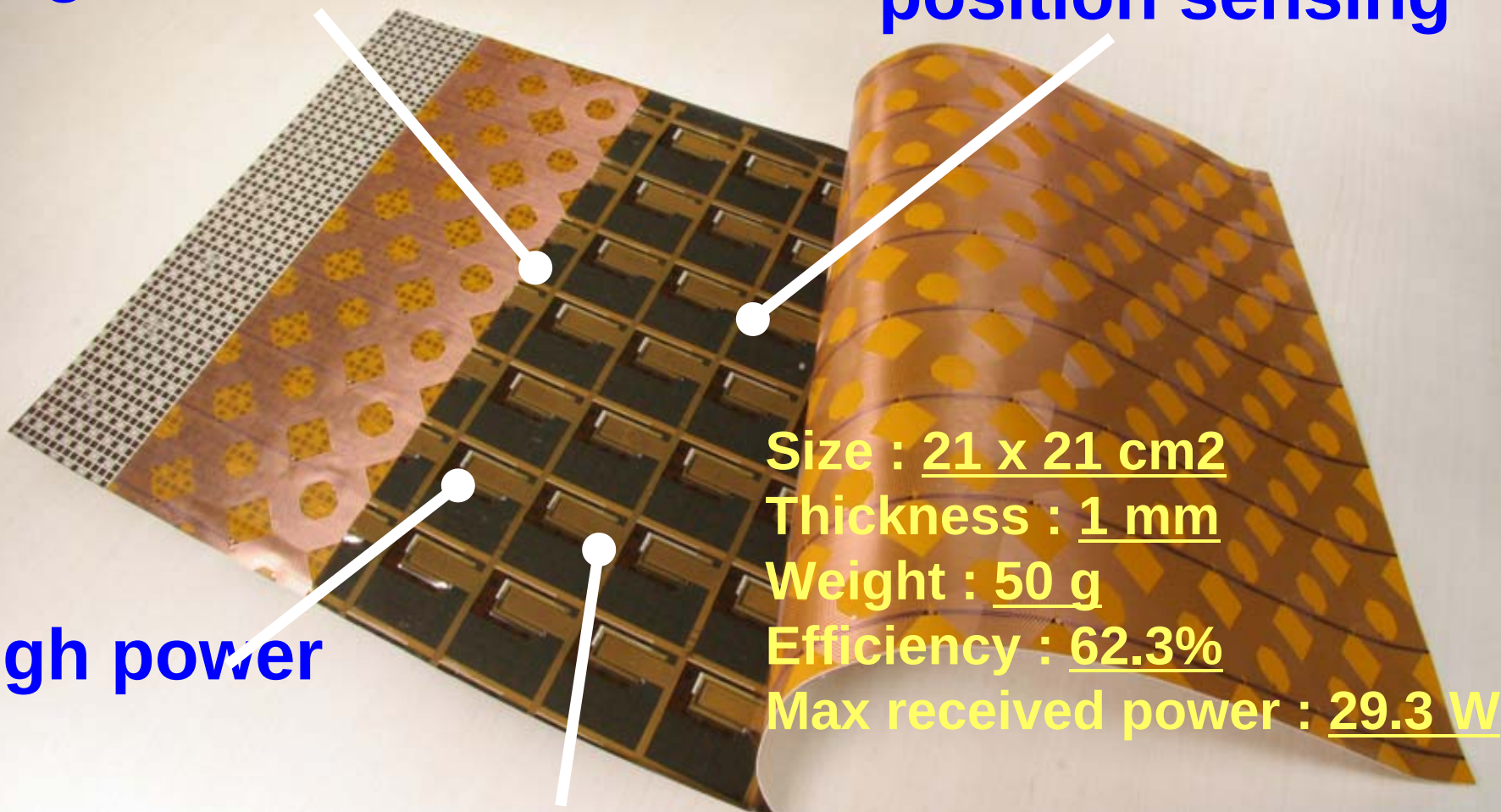
Plastic MEMS switches

Low loss
Slow ~ 0.1s
# of switching limited

Wireless power transmission system

Hybrid simulation of IC, mechanics and electro-magnetism

Wireless power transmission sheet (3D-stacked)



X’mas tree w/o a battery wirelessly powered

21 LEDs

13.56 MHz

Received power : 2 W

No electrical shock

I touched it by my hand. No problem ☺


Wirelessly powered room in the future
Providing infrastructure ubiquitous electronics
In the wall
TV on a wall
Mobile phone & PC & e-accessories
(data can be wireless but USB's wire delivers power)
In the table
Ambient illumination
Vacuum cleaner
Home-care robot
In the floor

Summary

- 3-D stacking, new frontier of integrated circuits, is opening up new electronics.
- Solving issues for higher performance, lower power, lower cost and newer functions
- New design tools for hybrid simulation and synthesis to fully enjoy 3-D stacking