ASP-DAC 2008 <mark>Jan</mark>uary 21 - 24, 2008

COEX, Seoul, Korea

Final Program



ASP-DAC 2008

13th Asia and South Pacific Design Automation Conference



January 21 - 24, 2008 COEX, Seoul, Korea 29.8

art

2D: Special Session Tackling Manufacturability/ Variability for 45nm and Below

Exhibition

Conference Secretariat

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Web Site: http://www.aspdac.com



Monday, January 21								
Time	#310A	#310BC	#311A	#311BC				
09:00 -12:30	Tutorial 1: System-Level Synthesis: Functions, Architectures,	Tutorial 1: Tutorial 2: Cross-Layer em-Level Synthesis: Approaches to tions, Architectures, Designing Reliable		Tutorial 4: Improvements in 65/45nm Physical Implementation Flow and Methodology				
14:00-17:30	and Communications	System's Using Unreliable Chips	Tutorial 5: On-Chip Network: State-of-the- Art Industrial Solution and Academic Research					
		Tuesd	lay, January 22					
Time	#310A	#310BC	#311A	#311BC	#320ABC			
08:30-10:00		Opening & Keyno	te Address I (Room 401)				
10:00-10:15	Coffee Break							
10:15-12:20	1A: New Challenges in High Level Synthesis	1B: Power and Thermal Modeling and Optimization	1C : Emerging Technologies	1D: Univ. LSI Design Contest				
12:20-13:30	Lunch / Univ. LSI Design Contest Discussion (Room 321A)							

2C : Floorplanning

3D: Special Session (Panel)

The Tears and Joy of Sowing and Reaping

Complex SoC's

ffee Break

2B: Interconnect

Modeling and

Simulation Techniques

3B: Interconnect,

NoCs, and MPSoCs

2A: Advanced Topic

in Logic Synthesis

3A: Routing

13:30-15:35

15:35-15:50

15:50-17:55

Wednesday, January 23									
Time	#310A #310BC		#311A	#311BC	#320ABC				
09:00-10:00	Keynote Address II (Room 401)								
10:00-10:15		C	offee Break						
10:15-12:20	4A: Variability Issues in Timing	4B: Memory and Processor Optimization	4C: New Techniques for Physical Design Optimization	4D: Designers' Forum New Emerging Application Areas for Future SoC					
12:20-13:30	Lunch / Student Forum (Room 321A)								
13:30-15:35	5A: Techniques for Formal and Simulation- Based Verification	5B: Power and for Performance optimization for Embedded Systems SC: Thermal Analysis and DFM		5D: Designers' Forum(Panel) Are System Level EDA Tools/Methodologies Coming?	Exhibition				
15:35-15:50	Coffee Break								
15:50-17:55	6A: Trends in Timing	6B: Statistical Modeling and Yield Prediction	6D: Special Session (Panel) How to Design Cool Chips for Hot Products						
18:30-20:30 Banquet (Room 103)									

Thursday, January 24									
Time	#310A #310BC		#311A	#311BC					
09:00-10:00		Keynote Address III (Room 401)							
10:00-10:15		Co	offee Break						
10:15-12:20	7A: Reliable/Testable Design Techniques	7B: Communication and Interfaces	7C: Power: Delivery and Reduction	7D: Special Session (Panel) Concurrent SoC and SiP Designs					
12:20-13:30		Lunc	h						
13:30-15:35	8A: Test Generation and Test Power	8B: Design Space Exploration	8C: Reliability and Power Management	8D: Designers' Forum Low Power Chips					
15:35-15:50	Coffee Brea								
15:50-17:55	9A: Analog/RF/ Mixed Signal CAD	9B: Architecture Exploration	9D: Designers' Forum (Panel) Best Ways to Use Billions of Devices on a Chip						

It is our great pleasure and honor to welcome you to the 13th ASP-DAC, January 21 - 24, 2008 held in Seoul, Korea. Astounding growth of economy in Asia for the last quarter century is based on the zeal and quest for the development of industry and information technology at its base. Ever-growing interactions among countries and among heterogeneous technologies are where the potential for unrelenting growth lies. This is happening in Asia, where the role of semiconductor and systems industry is truly critical.

ASP-DAC 2008 will encourage all participants from all parts of the planet earth to meet with each other and exploit the best opportunities in the future regarding information technology embedded systems design and design automation technologies. We look forward to having a precious time to share the active exchange of ideas and experiences through this conference.

ASP-DAC 2008 received 350 papers from 27 countries and selected 122 papers as a result of thorough review. ASP-DAC conference will be a stimulating and challenging conference through academic exchange of up-to-date ideas. We have one-day for tutorials comprising two full-day lectures and four half-day lectures, followed by technical sessions in three days including Special Sessions, Designers' Forum, Student Forum, and University LSI Design Contest. ASP-DAC 2008 will help you steer into the vision of 2008 and beyond with messages from three excellent keynote speeches, to be addressed by Professor Jan Rabaey, Univ. of California on Tuesday, Dr. Ki-Soo Hwang, CEO of Core Logic, top fabless in Korea on Wednesday, and Dr. F. C. Tseng, Vice Chairman of TSMC on Thursday.

We hope you enjoy every minute during your stay in Seoul, dynamic capital city of Korea with over 12 million people and 600 years of history.

> Chong-Min Kyung General Chair ASP-DAC 2008

Kiyoung Choi Technical Program Co-Chair ASP-DAC 2008

Soonhoi Ha Technical Program Co-Chair ASP-DAC 2008

Hijoing Choi Ha, foorhor



Table of Contents

Conference Highlights 3
Sponsorship 6
Organizing Committee 7
Technical Program Committee 8
Steering Committee 11
University LSI Design Contest
Designers' Forum 14
Student Forum
ASP-DAC 2008 Best Papers 16
ASP-DAC 2008 Design Contest Award 17
Invitation to ASP-DAC 2009
Keynote Addresses ······ 19
Technical Program ······22
Tutorials ······ 41
Conference Information 46
Venue Information 47
ASP-DAC 2008 Exhibition
Conference Site



Conference Highlights

Opening & Keynote Address I

Tuesday, January 22, 8:30-10:00, Room 401 Jan M. Rabaey (*Univ. of California, Berkeley, USA*) **A Brand New Wireless Day**

Keynote Address II

Wednesday, January 23, 9:00-10:00, Room 401 Ki-Soo Hwang (*Core Logic, Korea*) **The Evolution of SoC Platform According to the New Mobile Paradigm**

Keynote Address III Thursday, January 24, 9:00-10:00, Room 401 F. C. Tseng (*TSMC, Taiwan*) The Future of Semiconductor Industry - A Foundry's Perspective

Special Sessions

2D: Tuesday, January 22, 13:30-15:35, Room 311BC Tackling Manufacturability/Variability for 45nm and Below Chair: Dale Edwards (Semiconductor Research., USA) Speakers: Yao-Ching Ku (TSMC, Taiwan) Nishath Verghese (Cadence Design Systems, USA) Sani Nassif (IBM, USA) David Z. Pan (Univ. of Texas, Austin, USA)

3D: Tuesday, January 22, 15:50-17:55, Room 311A+311BC
The Tears and Joy of Sowing and Reaping Complex SoC's
Moderator: Ing-Jer Huang (*Nat'l Sun Yat-Sen Univ., Taiwan*)
Panelists: Youn-Long Lin (*Nat'l Tsing Hua Univ./Global UniChip, Taiwan*)
Hoonmo Yang (*Core Logic, Korea*)
Toshihiro Hattori (*Renesas Technology, Japan*)
Ahmed Jarraya (*CEA-LETI, MINATEC, France*)
Xu Cheng (*Peking Univ., China*)

6D: Wednesday, January 23, 15:50-17:55, Room 311A+311BC
How to Design Cool Chips for Hot Products
Moderator: Massoud Pedram (Univ. of Southern California, USA)
Panelists: Giovanni De Micheli (EPFL, Switzerland) Jan M. Rabaey (Univ. of California, Berkeley, USA) Soo-Kwan Eo (Samsung Electronics, Korea)

7D: Thursday, January 24, 10:15-12:20, Room 311BC **Concurrent SoC and SiP Designs**Moderator: Wei-Chung Lo (*ITRI, Taiwan*)
Panelists: C. P. Hung (*ASE, Taiwan*)
Lung Chu (*Cadence Design Systems, USA*)
Joungho Kim (*KAIST, Korea*)
Epan Wu (*VIA Technologies, Taiwan*)

Designers' Forum

4D: Wednesday, January 23, 10:15-12:20, Room 311BC
New Emerging Application Areas for Future SoC
Chair: Sungjoo Yoo (Samsung Electronics, Korea)
Speakers: JuneHee Lee (Samsung Electronics, Korea)
Shorin Kyo (NEC, Japan)
Doug Pulley (picoChip, UK)
Tatsuo Nakagawa (Hitachi, Japan)

5D: Wednesday, January 23, 13:30-15:35, Room 311BC
Are System Level EDA Tools/Methodologies Coming?
Moderator: Ren-Song Tsay (Nat'l Tsing Hua Univ., Taiwan)
Panelists: Raul Camposano (Xoomsys, USA) Toshihiro Hattori (Renesas Technology, Japan) Austin Kim (Samsung Electronics, Korea) Howard Mao (Springsoft, Taiwan) Sri Parameswaran (Univ. of New South Wales, Australia)

8D: Thursday, January 24, 13:30-15:35, Room 311BC Low Power Chips

Chair: Kang Yi (*Handong Global Univ., Korea*) Speakers: T. W. Williams (*Synopsys, USA*) Hiroaki Shikano (*Hitachi, Japan*) Hock Chen (*Global Unichip, Taiwan*) Shuichi Kunie (*NEC, Japan*)

9D: Thursday, January 24, 15:50-17:55, Room 311A + 311BC
Best Ways to Use Billions of Devices on a Chip
Moderator: Grant Martin (*Tensilica, USA*)
Panelists: Deming Chen (*Univ. of Illinois, Urbana-Champaign, USA*)
Nikil Dutt (*Univ. of California, Irvine, USA*)
Joerg Henkel (*Karlsruhe Univ., Germany*)
Kyungho Kim (*Samsung Electronics, Korea*)

Kazutoshi Kobayashi (Kyoto Univ., Japan)



Tutorials

[Full-Day Tutorials]

1: Monday, January 21, 09:00-17:30, Room 310A

System-Level Synthesis: Functions, Architectures, and Communications

Speakers: Alberto Sangiovanni Vincentelli (Univ. of California, Berkeley, USA)

Jason Cong (Univ. of California, Los Angeles, USA) Radu Marculescu (Carnegie Mellon Univ., USA) Clas A. Jacobson (United Technologies Research Center, USA)

2: Monday, January 21, 09:00-17:30, Room 310BC

Cross-Layer Approaches to Designing Reliable Systems Using Unreliable Chips

Speakers: Nikil Dutt (Univ. of California, Irvine, USA) Fadi Kurdahi (Univ. of California, Irvine, USA) Ahmed Eltawil (Univ. of California, Irvine, USA) Sani Nassif (IBM, USA)

[Half-Day Tutorials]

 Monday, January 21, 09:00-12:30, Room 311A
 Latest Advances and Future Opportunities on CAD for FPGAs
 Speakers: Deming Chen (Univ. of Illinois, Urbana-Champaign, USA) Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, USA)

4: Monday, January 21, 09:00-12:30, Room 311BC Improvements in 65/45nm Physical Implementation Flow and Methodology Speaker: Andrew B. Kahng (Univ. of California, San Diego, USA)

5: Monday, January 21, 14:00-17:30, Room 311A

Speakers: David Gwilt (ARM, UK) Axel Jantsch (Royal Inst. of Tech., Sweden)

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6

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*Jin-Young Choi
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Thomas Kropf
Bosch, Germany
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Posdata, USA
Igor Markov
Univ. of Michigan, USA
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*Martin D. F. Wong Univ. of Illinois, Urbana-Champaign, USA Charles Chiang Synopsys, USA Sung Kyu Lim Georgia Inst. of Tech., USA Hyunchul Shin Hanyang Univ., Korea Atsushi Takahashi Tokyo Inst. of Tech., Japan Ting-Chi Wang Nat'l Tsing Hua Univ., Taiwan

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[8] Interconnect, Device and **Circuit Modeling and Simulation** *Hideki Asai Shizuoka Univ., Japan Charlie Chung-Ping Chen Nat'l Taiwan Univ., Taiwan Yungseon Eo Hanyang Univ., Korea Parthasarathy Ramaswamy Intel, India Takashi Sato Tokyo Inst. of Tech., Japan Sheldon Tan Univ. of California, Riverside, USA Wenjian Yu Tsinghua Univ., China

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The University LSI Design Contest was conceived as a unique program of ASP-DAC Conference. The purpose of the Contest is to encourage education and research in LSI design, and its realization on chips at universities, and other educational organizations by providing opportunities to present and discuss innovative and state-of-the-art designs at the conference. Application areas and types of circuits include (1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, and (4) Custom Application Specific Circuits and Memories. Methods or technologies used for implement -tation includes (a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices, including FPGA/PLDs.

This year, thirteen designs will be disclosed in Session 1D with short presentations followed by live discussions in front of posters. Submitted designs were reviewed by the members of the University Design Contest Committee based on the following criteria: Reliability of the design and implementation, Quality of the implementation, Performance of the design, Novelty, and Additional special features. In the selection process, emphasis was placed more on reliability, quality, and performance. As a result, the thirteen designs were selected. In addition, we have instituted one outstanding design award and one special feature award.

It is with great pleasure that we acknowledge the contributions to the Design Contest, and it is our earnest belief that it will promote and enhance research and education in LSI design in academic organizations. It is also our hope that many people not only in academia but also in industry will attend the contest and enjoy the stimulating discussions.

Date, Time, and Locations:

Oral Presentation 10:15 - 11:55, January 22, 2008, Room 311BC Poster Presentation 12:20 - 13:30, January 22, 2008, Room 321A (Light meal will be served.)

University LSI Design Contest Committee Chair In-Cheol Park Incheal Dark (KAIST, Korea)

University LSI Design Contest Committee

Chair In-Cheol Park KAIST, Korea

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Masanori Hariyama Tohoku Univ., Japan Kenichi Okada Tokyo Inst. of Tech., Japan Chih-Wei Liu Nat'l Chiao Tung Univ., Taiwan Chi-ying Tsui The Hong Kong Univ. of Science & Technology, Hong Kong Xiaoyang Zeng Fudan Univ., China

Designers' Forum was conceived as a unique program that shares design experience and solutions of real product designs of the industries among SoC designers and EDA academia/developers.

It consists of these four special sessions. Oral Sessions: 4D New Emerging Application Areas for Future SoC 8D Low Power Chips Panel Discussions: 5D Are System Level EDA Tools/Methodologies Coming? 9D Best Ways to Use Billions of Devices on a

Chip

Here, designs will be presented focusing on design styles, design issues, new technologies, and ways to tackle design issues. Panel discussions will also be held for the latest design issues and EDA methodologies. Detailed information of each session is as follows.

Session 4D (10:15-12:20, January 23)

[New Emerging Application Areas for Future SoC]

▶ This session deals with new emerging industries. Four speakers will present on future home, automotive, mobile, and environmental electronics. Presenters are from Samsung (future DTVs), NEC (in-vehicle vision processors), Picochip (multi-core DSP for base stations), and Hitachi (wireless sensor networks).

Session 5D (13:30-15:35, January 23)

[Are System Level EDA Tools/Methodologies Coming?]

► After more than 10 years of studies by many researchers, system level EDA is still not popular. However, some success stories are reported recently. Issues on modeling/ synthesis/verification and platform-based designs can be discussed in this panel.

Session 8D (13:30-15:35, January 24) [Low Power Chips]

▶ In this session, low power chips designed recently will be presented. Static and dynamic power reduction techniques will also be discussed. The speakers are from Hitachi (heterogeneous multi-cores), Synopsys (low power design techniques), NEC (low power application processors for mobile handsets), and Global UniChip.

Session 9D (15:50-17:55, January 24)

[Best Ways to Use Billions of Devices on a Chip] ■ Issues on effective use of billons of devices on a chip are the theme of this panel. What to integrate (processors, memories, DSPs, programmable circuits)? How to integrate (buses, networks, protocols, buffers)? Defect tolerant designs and error recovery designs can also be discussed.

Designers' Forum Chair Hyunchul Shin (Hanyang Univ., Korea)

Idymacht Shin

Student Forum

The Student Forum at the ASP-DAC 2008 is a poster session for graduate students to present and discuss their research with people in the EDA community. A professional review committee selected quality posters among the submissions. Please join the poster session and give feedbacks to the presenters and also have discussion with people from academia and industry.

Date and Time: 12:20 - 13:30, January 23, 2008 Location: Room 321A (Light meal will be served.)

We would like to give special thanks to the ASP-DAC 2008 sponsors that also support ASP-DAC 2008 Student Forum

Student Forum Chair Naehyuck Chang (Seoul Nat'l Univ., Korea)

N. Ung

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- Best Paper Award
- 1A-1 Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning Feng Wang, Xiaoxia Wu, and Yuan Xie (*Pennsylvania State* Univ., USA)
- 9A-1 An Efficient, Fully Nonlinear, Variability-Aware Non-Monte-Carlo Yield Estimation Procedure with Applications to SRAM Cells and Ring Oscillators

Chenjie Gu and Jaijeet Roychowdhury (Univ. of Minnesota, USA)

Best Paper Candidates

- 1A-1 Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning Feng Wang, Xiaoxia Wu, and Yuan Xie (Pennsylvania State Univ., USA)
- 2C-1 Symmetry-Aware Placement with Transitive Closure Graphs for Analog Layout Design Lihong Zhang (*Memorial Univ. of Newfoundland, Canada*), Richard Shi (*Univ. of Washington, USA*), and Yingtao Jiang (*Univ. of Nevada, USA*)
- 3A-5 MeshWorks: An Efficient Framework for Planning, Synthesis and Optimization of Clock Mesh Networks Anand Rajaram and David Z. Pan (Univ. of Texas, Austin, USA)
- 5B-1 Hybrid Solid-State Disks: Combining Heterogeneous NAND
 Flash in Large SSDs
 Li-Pin Chang (Nat'l Chiao Tung Univ., Taiwan)
- 6A-1 Pessimism Reduction in Coupling Aware Static Timing Analysis Using Timing and Logic Filtering Debasish Das (Northwestern Univ., USA), Kip Killpack, Chandramouli Kashyap, Abhijit Jas (Intel, USA), and Hai Zhou (Northwestern Univ., USA)
- 6B-2 Within-Die Process Variations: How Accurately Can They Be Statistically Modeled? Brendan Hargreaves, Henrik Hult, and Sherief Reda (*Brown Univ.*, USA)
- 8A-1 Circuit Lines for Guiding the Generation of Random Test Sequences for Synchronous Sequential Circuits Irith Pomeranz (*Purdue Univ., USA*), Sudhakar M. Reddy (*Univ.* of Iowa, USA)
- 8B-1 ReSP: A Non-Intrusive Transaction-Level Reflective MPSoC Simulation Platform for Design Space Exploration Giovanni Beltrame (*European Space Agency, The Netherlands*), Cristiana Bolchini, Luca Fossati, Antonio Miele, and Donatella Sciuto (*Politecnico di Milano, Italy*)
- 9A-1 An Efficient, Fully Nonlinear, Variability-Aware Non-Monte-Carlo Yield Estimation Procedure with Applications to SRAM Cells and Ring Oscillators

Chenjie Gu and Jaijeet Roychowdhury (*Univ. of Minnesota, USA*) 9B-1 SPKM : A Novel Graph Drawing Based Algorithm for Application Mapping onto Coarse-Grained Reconfigurable Architectures

Jonghee W. Yoon (Seoul Nat'l Univ., Korea), Aviral Shrivastava (Arizona State Univ., USA), Sanghyun Park, Minwook Ahn (Seoul Nat'l Univ., Korea), Reiley Jeyapaul (Arizona State Univ., USA), and Yunheung Paek (Seoul Nat'l Univ., Korea)

Best Design Award

1D-1 A 1.2GHz Delayed Clock Generator for High-Speed Microprocessors Inhwa Jung, Moo-Young Kim, Chulwoo Kim (Korea Univ., Korea)

Special Feature Award

1D-7 Dynamic Supply Noise Measurement Circuit Composed of Standard Cells Suitable for In-Site SoC Power Integrity Verification Yasuhiro Ogasahara, Masanori Hashimoto, Takao Onoye (*Osaka Univ., Japan*) On behalf of the Organizing Committee, it is my great pleasure and honor to invite all of you to ASP-DAC 2009, which is the 14th event of this conference series.

ASP-DAC is now well stabilized in its position as the premier annual event of Electronic Design Automation and Design community in Asian and South Pacific region.

ASP-DAC 2009 will be held from January 19 to 22, 2009 at Pacifico Yokohama, Japan. Technical Program Chair of this conference is Professor Ren-Song Tsay from National Tsing Hua University, Taiwan. Technical Program Vice Chair is Professor Shinji Kimura from Waseda University, Japan. Under their strong leadership, internationally organized Program Committee will structure ASP-DAC as a high-quality conference that emphasizes original contributions that open up new vistas in the field with significant theoretical and practical impact.

The conference will include a technical program, keynote talks, tutorials, and special sessions highlighting the latest issues and development in IC design technology and automation.

I would like to invite you to actively participate in ASP-DAC by submitting cutting edge research results for publication, by proposing interesting topics for tutorials and special sessions, or simply by dropping by in January to enjoy a lively ASP-DAC event.

Expecting to see you in Yokohama in 2009!

Kazutoshi Wakabayashi General Chair ASP-DAC 2009

Lagu Wakabayashi

Keynote Addresses

Keynote Address I

Tuesday, January 22, 9:00-10:00, Room 401

A Brand New Wireless Day

bound for some very exciting times.

Jan M. Rabaey Professor, Univ. of California, Berkeley, USA



The wireless communications field has experienced a truly amazing growth since the early 1990's. Wireless connectivity slowly but surely has become pervasive. One would expect that by now this revolution must be losing some steam, but the truth is far from that. If anything, it is gathering even more speed. In the coming decades, introduction of innovative wireless technologies will enable a broad range of exciting applications to come to fruition, and reshape the way we interact with our daily living environment. Underlying it all is a threetiered environment consisting of a large number of huge data and compute centers, billions of mobile compute and computation devices. and potentially trillions of tiny sensors and actuators. Making this happen will require some important wireless roadblocks to be either overcome or circumvented. A short list of those includes spectrum scarcity, reliability, complexity, security and obviously power. In this presentation, a number of innovative and even revolutionary solutions to address these will be discussed. Examples are collaborative cognitive networks, wireless in the mm-wave region of the spectrum, and miniature wireless. Each of these approaches pushes some part of the design technology to its limits, and may even require a totally novel approach towards design, all this while semiconductor technology is trying to cope with the uncertainty of design in the nanometer regime. One thing is for sure - the wireless designer of the next decade is

Keynote Address II Wednesday, January 23, 9:00-10:00, Room 401

The Evolution of SoC Platform According to the New Mobile Paradigm Ki-Soo Hwang CEO, Core Logic, Korea



Mobile business has grown rapidly over the last five years. With multimedia technology being applied quickly to the mobile environment, we are seeing a greater variety of mobile devices from mobile phones to MP3 players, cameras, and navigation devices, and as technology develops at a faster pace, truly innovating mobile multimedia technology is being witnessed. This innovative change can only be sustained upon a deep understanding of the evolution of SoC platforms according to the change in mobile paradigm.

In the early mobile phone market, call quality was the greatest issue. Afterwards as functions leveled off to a certain degree, manufacturers competed for better design in the aspects of high speed / stability, convergence, and slim form factors according to the introduction of the 2.5 generation mobile network in the early 2000s. At this stage, camera (photo), MP3 (music) and now even TV (video) functions have been converged into mobile phones giving momentum to the evolution of multimedia functions in mobile handsets. Until now the innovation of mobile handsets were centered around technology, but with 3G technology changing the focus from telephony to video telephony, the evolution of handsets is changing to the perspective of marketing and technology. In addition, with the emergence of the smart phone, not

only is Internet easily accessible, but the wireless connection of mobile phones with other mobile devices has become important which is leading to a state of multi-networks.

As witnessed, the innovation of mobile handsets was led by faster development speed and convergence. In this kaleidoscope of handset development, SoC platform technology was at the foundation. The camera hefunction of mobile phones grew with the development of ASIC/SoC technology and the evolution of MPEG 2.4 technology which is the global standard for video multimedia. Now, the Multimedia Application Processor (MAP) which enables various multimedia applications such as music phone,

movie phone, and TV (video) will evolve into a multimedia-centric Application Processor (AP) and will lead the transformation of multimedia along with other various operating systems.

In the new mobile environment which emphasizes Internet and connectivity, SoC technology and market -ing will be the cornerstones of the mobile multimedia network and in order to efficiently support this we must understand the new mobile paradigm and evolve the SoC platform to accommodate this change. Keynote Address III Thursday, January 24, 9:00-10:00, Room 401

The Future of Semiconductor Industry - A Foundry's Perspective F. C. Tseng Vice Chairman, TSMC, Taiwan



The semiconductor industry is in an extended period of moderate and steady growth. In this stage, many technologies are made to work together to deliver benefits that are greater than the sum of their individual parts. Economy of scale provides for steady cost reduction and constantly widening markets. The adoption of communication, computer and consumer products is spreading across the world in both advanced and developing economies. Opportunities are global and not concentrated on any one specific region. New applications and technologies now globally serve billions of people.

Meantime, the semiconductor industry is facing several economic, design and technology challenges. Solutions need to be developed in order to continue the industry growth. Foundry and IC companies must develop a much deeper and broader partnership. With end-to-end collaboration from design, wafer manufacturing to assembly and test, IC companies could fully leverage foundry's new technology offerings and capacity support in order to create the product differentiation in their end market. TSMC is committed to the long-term investment in leading edge technology development and GigaFab capacity expansion needed to enable the industry growth.

Technical Program

Tuesday, January 22, 08:30-10:00 Opening & Keynote Address I Room 401

Chair: Kiyoung Choi (Seoul Nat'l Univ., Korea)

A Brand New Wireless Day

Jan M. Rabaey (Univ. of California, Berkeley, USA)

Tuesday,	January 22,	10:15-12:20			Ro	oom	310A
	1A: New	Challenges	in Hiah	Level	Svnthesis		

- Chairs: Taewhan Kim (Seoul Nat'l Univ., Korea), Kazutoshi Wakabayashi (NEC, Japan)
- 1A-1 Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning Feng Wang, Xiaoxia Wu, and Yuan Xie (Pennsylvania State Univ., USA)
- 1A-2 Behavioral Synthesis with Activating Unused Flip-Flops for Reducing Glitch Power in FPGA Cheng-Tao Hsieh (Nat'l Tsing Hua Univ., Taiwan), Jason Cong, Zhiru Zhang (Univ. of California, Los Angeles, USA), and Shih-Chieh Chang (Nat'l Tsing Hua Univ., Taiwan)
- 1A-3 A Multicycle Communication Architecture and Synthesis Flow for Global Interconnect Resource Sharing Wei-Sheng Huang, Yu-Ru Hong, Juinn-Dar Huang, and Ya-Shih Huang (Nat'l Chiao Tung Univ., Taiwan)
- 1A-4 Scheduling with Integer Time Budgeting for Low-Power Optimization Wei Jiang, Zhiru Zhang, Miodrag Potkonjak, and Jason Cong (Univ. of California, Los Angeles, USA)
- 1A-5(\$) REWIRED Register Write Inhibition by Resource Dedication Pushkar Tripathi, Rohan Jain (Indian Inst. of Tech. Delhi, India), Srikanth Kurra (Oracle, India), and Preeti Ranjan Panda (Indian Inst. of Tech. Delhi, India)
- 1A-6(\$) An Efficient Performance Improvement Method Utilizing Specialized Functional Units in Behavioral Synthesis Tsuyoshi Sadakata and Yusuke Matsunaga (Kyushu Univ., Japan)



Room 310BC

1B: Power and Thermal Modeling and Optimization

Chair: Joerg Henkel (Karlsruhe Univ., Germany) Eui-Young Chung (Yonsei Univ., Korea)

Tuesday, January 22, 10:15-12:20

- 1B-1 Predictive Power Aware Management for Embedded Mobile Devices Young-Si Hwang, Sung-Kwan Ku, Chan-Min Jung, and Ki-Seok Chung (Hanyang Univ., Korea)
- **1B-2** A Dynamic-Programming Algorithm for Reducing the Energy Consumption of Pipelined System-Level Streaming Applications N. Liveris, H. Zhou (Northwestern Univ., USA), and P. Banerjee (HP Labs., USA)
- 1B-3 Temperature-Aware MPSoC Scheduling for Reducing Hot Spots and Gradients Ayse Kivilcim Coskun, Tajana Simunic Rosing (Univ. of California, San Diego, USA), Keith A. Whisnant, and Kenny Gross (Sun Microsystems, USA)
- 1B-4 Run-Time Power Gating of On-Chip Routers Using Look-Ahead Routing Hiroki Matsutani (Keio Univ., Japan), Michihiro Koibuchi (Nat'l Inst. of Informatics, Japan), Daihan Wang, and Hideharu

Inst. of Informatics, Japan), Dainan Wang, and Hidenaru Amano (Keio Univ., Japan)

1B-5(\$) Automated Techniques for Energy Efficient Scheduling on Homogeneous and Heterogeneous Chip Multi-Processor Architectures

Sushu Zhang and Karam S. Chatha (Arizona State Univ., USA)

1B-6(\$) Statistical Power Profile Correlation for Realistic Thermal Estimation Love Singhal (Univ. of California, Irvine, USA), Sejong Oh (KAIST, Korea), and Eli Bozorgzadeh (Univ. of California, Irvine, USA)

Tuesday, January 22, 10:15-12:20 Room 311A

1C: Emerging Technologies

Chairs: Li Shang (Queen's Univ., Canada)

- Chao Huang (Virginia Tech., USA)
- 1C-1 Reconfigurable RTD-Based Circuit Elements of Complete Logic Functionality

Yexin Zheng and Chao Huang (Virginia Tech., USA)

- 1C-2 MBARC: A Scalable Memory Based Reconfigurable Computing Framework for Nanoscale Devices Somnath Paul and Swarup Bhunia (Case Western Reserve Univ., USA)
- 1C-3 Moving Forward: A Non-Search Based Synthesis Method Toward Efficient CNOT-Based Quantum Circuit Synthesis Algorithms Mehdi Saeedi, Morteza Saheb Zamani, and Mehdi Sedighi (Amirkabir Univ. of Tech., Iran)

1C-4 A CAD Tool for RF MEMS Devices Rajesh Pande and Rajendra Patrikar (Visvesvaraya Nat'l Inst. of Tech., India)

Tuesday, January 22,	10:15-12:20	Room 311BC
1D:	University LSI Design Contes	t

- Chairs: Kenichi Okada (Tokyo Inst. of Tech., Japan) Hiroshi Kawaguchi (Kobe Univ., Japan)
- 1D-1 A 1.2GHz Delayed Clock Generator for High-Speed Microprocessors Inhwa Jung, Moo-Young Kim, and Chulwoo Kim (Korea Univ., Korea)
- 1D-2 LVDS-Type On-Chip Transmission Line Interconnect with Passive Equalizers in 90nm CMOS Process Akiko Mineyama, Hiroyuki Ito, Takahiro Ishii, Kenichi Okada, and Kazuya Masu (Tokyo Inst. of Tech., Japan)
- 1D-3 A Slew-Rate Controlled Output Driver with One-Cycle Tuning Time Young-Ho Kwak, Inhwa Jung, and Chulwoo Kim (Korea Univ., Korea)
- 1D-4 A Low-Leakage Current Power 180-nm CMOS SRAM Tadayoshi Enomoto and Yuki Higuchi (Chuo Univ., Japan)
- 1D-5 A CMOS Direct Sampling Mixer Using Switched Capacitor Filter Technique for Software-Defined Radio Hong Phuc Ninh, Takashi Moue, Takashi Kurashina, Kenichi Okada, and Akira Matsuzawa (Tokyo Inst. of Tech., Japan)
- 1D-6 Small-Area CMOS RF Distributed Mixer Using Multi-Port Inductors Susumu Sadoshima, Satoshi Fukuda, Tackya Yammouch, Hiroyuki Ito, Kenichi Okada, and Kazuya Masu (Tokyo Inst. of Tech., Japan)
- 1D-7 Dynamic Supply Noise Measurement Circuit Composed of Standard Cells Suitable for In-Site SoC Power Integrity Verification Yasuhiro Ogasahara, Masanori Hashimoto, and Takao Onoye (Osaka Univ., Japan)
- 1D-8 Duo-Binary Circular Turbo Decoder Based on Border Metric Encoding for WiMAX Ji-Hoon Kim and In-Cheol Park (KAIST, Korea)
- 1D-9 Area and Power Efficient Design of Coarse Time Synchronizer and Frequency Offset Estimator for Fixed WiMAX Systems Tae-Hwan Kim and In-Cheol Park (KAIST, Korea)
- 1D-10 A Low-Cost Cryptographic Processor for Security Embedded System Ronghua Lu, Jun Han, Xiaoyang Zeng, Qing Li, Lang Mai, and Zhao Jia (Fudan Univ., China)
- 1D-11 Multithreaded Coprocessor Interface for Multi-Core Multimedia SoC

Shih Hao Ou, Tay-Jyi Lin, Xiang Sheng Deng, Zhi Hong Zhuo, and Chih Wei Liu (Nat'l Chiao Tung Univ., Taiwan)



1D-12 Parameterized Embedded In-Circuit Emulator and Its Retargetable Debugging Software for Microprocessor/Microcontroller/DSP Processor

Liang-Bi Chen, Yung-Chih Liu, Chien-Hung Chen, Chung-Fu Kao, and Ing-Jer Huang (Nat'l Sun Yat-Sen Univ., Taiwan)

Tuesday, January 22, 13:30-15:35 Room 310A 2A: Advanced Topic in Logic Synthesis

Chairs: Shih-Chieh Chang (Nat'l Tsing Hua Univ., Taiwan) In-Cheol Park (KAIST, Korea)

- 2A-1 Global Optimization of Common Subexpressions for Multiplierless Synthesis of Multiple Constant Multiplications Yuen-Hong Alvin Ho, Chi-Un Lei, Hing-Kit Kwan, and Ngai Wong (Univ. of Hong Kong, Hong Kong)
- 2A-2 Decomposition Based Approach for Synthesis of Multi-Level Threshold Logic Circuits Tejaswi Gowda and Sarma Vrudhula (Arizona State Univ., USA)
- 2A-3 Timing-Power Optimization for Mixed-Radix Ling Adders by Integer Linear Programming Yi Zhu, Jianhua Liu, Haikun Zhu, and Chung-Kuan Cheng (Univ. of California, San Diego, USA)
- 2A-4 Efficient Synthesis of Compressor Trees on FPGAs Hadi Parandeh-Afshar (Univ. of Tehran, Iran), Philip Brisk, and Paolo Ienne (EPFL, Switzerland)
- 2A-5(\$) Area Recovery under Depth Constraint by Cut Substitution for Technology Mapping for LUT-Based FPGAs Taiga Takata and Yusuke Matsunaga (Kyushu Univ., Japan)

2A-6(\$) An Optimal Algorithm for Sizing Sequential Circuits for Industrial Library Based Designs Sanghamitra Roy, Yu Hen Hu (Univ. of Wisconsin, Madison, USA), Charlie Chung-Ping Chen, Shih-Pin Hung, Tse-Yu Chiang, and Jiuan-Guei Tseng (Nat'l Taiwan Univ., Taiwan)

Tuesda	y, Ja	anuary	22, 1	13:30	-15:35			Room	310BC
	2B:	Interc	onne	ct M	odelina	and	Simulation	Techniques	

- Chairs: Yungseon Eo (Hanyang Univ., Korea) Yokomizo Goichi (STARC, Japan)
- 2B-1 Efficient Numerical Modeling of Random Rough Surface Effects for Interconnect Internal Impedance Extraction Quan Chen and Ngai Wong (Univ. of Hong Kong, Hong Kong)
- 2B-2 Efficient Techniques for 3-D Impedance Extraction Using Mixed Boundary Element Method Fang Gong, Wenjian Yu, Zeyi Wang, Zhiping Yu (Tsinghua Univ., China), and Changhao Yan (Fudan Univ., China)
- 2B-3 Generating Stable and Sparse Reluctance/Inductance Matrix under Insufficient Conditions Yuichi Tanji (Kagawa Univ., Japan), Takayuki Watanabe (Univ. of Shizuoka, Japan), and Hideki Asai (Shizuoka Univ., Japan)

- 2B-4 Hierarchical Krylov Subspace Reduced Order Modeling of Large RLC Circuits Duo Li and Sheldon X.-D. Tan (Univ. of California, Riverside, USA)
- 2B-5 Statistical Noise Margin Estimation for Sub-Threshold Combinational Circuits Yu Pu, José Pineda de Gyvez, Henk Corporaal (Technische

Yu Pu, José Pineda de Gyvez, Henk Corporaal (Technische Universiteit Eindhoven, The Netherlands), and Yajun Ha (Nat'l Univ. of Singapore, Singapore)

Tuesday,	January 22,	13:30-15	:35	Room	311A
		2C:	Floorplanning		

- Chairs: Shin'ichi Wakabayashi (Hiroshima City Univ., Japan) Ting-Chi Wang (Nat'I Tsing Hua Univ., Taiwan)
- 2C-1 Symmetry-Aware Placement with Transitive Closure Graphs for Analog Layout Design Lihong Zhang (Memorial Univ. of Newfoundland, Canada), C.-J. Richard Shi (Univ. of Washington, USA), and Yingtao Jiang (Univ. of Nevada, USA)
- 2C-2 Constraint-Free Analog Placement with Topological Symmetry Structure Qing Dong and Shigetoshi Nakatake (Univ. of Kitakyushu, Japan)
- 2C-3 TCG-Based Muli-Bend Bus Driven Floorplanning Tilen Ma and Evangeline F. Y. Young (The Chinese Univ. of Hong Kong, Hong Kong)
- 2C-4 Large-Scale Fixed-Outline Floorplanning Design Using Convex Optimization Techniques Chaomin Luo, Miguel F. Anjos (Univ. of Waterloo, Canada), and Anthony Vannelli (Univ. of Guelph, Canada)
- 2C-5(\$) Bus-Aware Microarchitectural Floorplanning Dae Hyun Kim and Sung Kyu Lim (Georgia Inst. of Tech., USA)
- 2C-6(\$) LP Based White Space Redistribution for Thermal Via Planning and Performance Optimization in 3D ICs Xin Li, Yuchun Ma, Xianlong Hong, Sheqin Dong (Tsinghua Univ., China), and Jason Cong (Univ. of California, Los Angeles, USA)

Tuesday, January 22, 13:30-15:35 2D: Special Session: Tackling Manufacturability/Variability for 45nm and Below

Organizer: David Z. Pan (Univ. of Texas, Austin, USA) **Chair:** Dale Edwards (Semiconductor Research, USA)

26

- 2D-1 Lithography Challenges and Solutions for 32nm Node and Beyond Yao-Ching Ku (TSMC, Taiwan)
- 2D-2 Predictive Models and CAD Methodology for Pattern Dependent Variability Nishath Verghese (Cadence Design Systems, USA)

- 2D-3 Technology Modeling and Characterization Beyond the 45nm Node Sani Nassif (IBM, USA)
- 2D-4 Synergistic Physical Synthesis for Manufacturability/Variability in 45nm Designs and Beyond David Z. Pan (Univ. of Texas, Austin, USA)

Tuesday, January 22, 15:50-17:55 Room 310A 3A: Routing

Chairs: Atsushi Takahashi (Tokyo Inst. of Tech., Japan) Jung Dong Cho (Sungkyunkwan Univ., Korea)

- 3A-1 MaizeRouter: Engineering an Effective Global Router Michael D. Moffitt (IBM, USA)
- 3A-2 A New Global Router for Modern Designs Jhih-Rong Gao, Pei-Ci Wu (Synopsys, Taiwan), and Ting-Chi Wang (Nat'l Tsing Hua Univ., Taiwan)
- 3A-3 Routability Driven Modification Method of Monotonic Via Assignment for 2-Layer Ball Grid Array Packages Yoichi Tomioka and Atsushi Takahashi (Tokyo Inst. of Tech., Japan)
- 3A-4 Ordered Escape Routing Based on Boolean Satisfiability Lijuan Luo and Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, USA)
- 3A-5 MeshWorks: An Efficient Framework for Planning, Synthesis and Optimization of Clock Mesh Networks Anand Rajaram and David Z. Pan (Univ. of Texas, Austin, USA)

Tuesday, January 22, 15:50-17:55	Room	310BC
3B: Interconnect, NoCs, and MPSoCs		

Chairs: Sungjoo Yoo (Samsung Electronics, Korea) Sungchan Kim (Seoul Nat'l Univ., Korea)

3B-1 Interconnect Modeling for Improved System-Level Design Optimization Luca Carloni (Columbia Univ., USA), Andrew B. Kahng, Swamy

Muddu (Univ. of California, San Diego, USA), Alessandro Pinto (Univ. of California, Berkeley, USA), Kambiz Samadi, and Puneet Sharma (Univ. of California, San Diego, USA)

- **3B-2** NoCOUT: NoC Topology Generation with Mixed Packet-Switched and Point-to-Point Networks Jeremy Chan and Sri Parameswaran (Univ. of New South Wales, Australia)
- **3B-3** Automatic Generation of Hardware Dependent Software for MPSoCs from Abstract System Specifications Gunar Schirner, Andreas Gerstlauer, and Rainer Dömer (Univ. of California, Irvine, USA)
- 3B-4 Application-Specific Network-on-Chip Architecture Synthesis Based on Set Partitions and Steiner Trees Shan Yan and Bill Lin (Univ. of California, San Diego, USA)

Tuesday, Januar	y 22, 15:50-17:55	Ro	om 311A+311BC
3D: Special Se	ession (Panel): The	Tears and Joy	of Sowing and
	Reaping Com	olex SoC's	

Organizer and Moderator: Ing-Jer Huang (Nat'l Sun Yat-Sen Univ., Taiwan)

Panelists: Youn-Long Lin (Nat'l Tsing Hua Univ./Global UniChip, Taiwan) Hoonmo Yang (Core Logic, Korea) Toshihiro Hattori (Renesas Technology, Japan) Ahmed Jarraya (CEA-LETI, MINATEC, France) Xu Chen (Peking Univ., China) Wednesday, January 23, 09:00-10:00

Keynote Address II

Chair: Chong-Min Kyung (KAIST, Korea)

The Evolution of SoC Platform According to the New Mobile Paradigm Ki-Soo Hwang (Core Logic, Korea)

Wednesday, January 23, 10:15-12:20 Room 310A 4A: Variability Issues in Timing

- Chair: Masanori Hashimoto (Osaka Univ., Japan) Janet Wang (Univ. of Arizona, USA)
- 4A-1 Statistical Gate Delay Model for Multiple Input Switching Takayuki Fukuoka, Akira Tsuchiya, and Hidetoshi Onodera (Kyoto Univ., Japan)
- 4A-2 Non-Gaussian Statistical Timing Models of Die-to-Die and Within-Die Parameter Variations for Full Chip Analysis Katsumi Homma, Izumi Nitta, and Toshiyuki Shibuya (Fujitsu Labs., Japan)
- 4A-3 Non-Gaussian Statistical Timing Analysis using Second-Order Polynomial Fitting Lerong Cheng (Univ. of California, Los Angeles, USA), Jinjun Xiong (IBM, USA), and Lei He (Univ. of California, Los Angeles, USA)
- 4A-4 A Capacitive Boosted Buffer Technique for High-Speed Process-Variation-Tolerant Interconnect in UDVS Application Saihua Lin, Yu Wang, Rong Luo, and Huazhong Yang (Tsinghua Univ., China)
- 4A-5 Static Timing: Back to Our Roots Ruiming Chen, Lizheng Zhang, Vladimir Zolotov, Chandu Visweswariah, and Jinjun Xiong (IBM, USA)

Wednesday,	Janua	ry 23,	10:15-1	2:20		Room	310BC
	4B:	Memo	v and	Processor	Optimization		

- Chairs: Jeonghun Cho (Kyungpook Nat'l Univ., Korea) Hiroyuki Tomiyama (Nagoya Univ., Japan)
- 4B-1 Synthesis and Design of Parameter Extractors for Low-Power Pre-Computation-Based Content-Addressable Memory Using Gate-Block Selection Algorithm Jui-Yuan Hsieh and Shanq-Jang Ruan (Nat'l Taiwan Univ. of Science and Technology, Taiwan)
- 4B-2 Block Cache for Embedded Systems Dominic Hillenbrand and Jörg Henkel (Univ. of Karlsruhe (TH), Germany)
- **4B-3** A Compiler-in-the-Loop Framework to Explore Horizontally Partitioned Cache Architectures Aviral Shrivastava (Arizona State Univ., USA), Ilya Issenin, and Nikil Dutt (Univ. of California, Irvine, USA)

- Fast, Quasi-Optimal, and Pipelined Instruction-Set Extensions 4B-4 Aiav K. Verma, Philip Brisk, and Paolo Jenne (EPFL, Switzerland)
- Load Scheduling: Reducing Pressure on Distributed Register 4B-5 Files for Free Mei Wen, Nan Wu, Maolin Guan, and Chunvuan Zhang (Nat'l Univ. of Defense Tech., China)

Wednesday, January 23, 10:15-12:20 Room 311A 4C: New Techniques for Physical Design Optimization

Chairs: Evangeline F. Y. Young (The Chinese Univ. of Hong Kong, Hong Kong)

Sherief Reda (Brown Univ., USA)

4C-1 DPlace2.0: A Stable and Efficient Analytical Placement Based on Diffusion

Tao Luo and David Z. Pan (Univ. of Texas, Austin, USA)

- Total Power Optimization Combining Placement, Sizing and 4C-2 Multi-Vt Through Slack Distribution Management Tao Luo (Univ. of Texas, Austin, USA), David Newmark (Advanced Micro Devices, USA), and David Z. Pan (Univ. of Texas, Austin, USA)
- 4C-3 An Innovative Steiner Tree Based Approach for Polygon Partition

Yonggiang Lu, Qing Su, and Jamil Kawa (Synopsys, USA)

- 4C-4 An MILP-Based Wire Spreading Algorithm for PSM-Aware Layout Modification Ming-Chao Tsai, Yung-Chia Lin, and Ting-Chi Wang (Nat'l Tsing Hua Univ., Taiwan)
- 4C-5(S) Low Power Clock Buffer Planning Methodology in F-D Placement for Large Scale Circuit Design Yanfeng Wang, Qiang Zhou, Yici Cai (Tsinghua Univ., China), Jiang Hu (Texas A&M Univ., USA), Xianlong Hong, and Jinian Bian (Tsinghua Univ., China)
- 4C-6(S) Power Grid Analysis Benchmarks Sani R. Nassif (IBM, USA)

Wednesday, January 23, 10:15-12:20 Room 311BC 4D: Designers' Forum: New Emerging Application Areas for Future SoC

Chair: Sungjoo Yoo (Samsung Electronics, Korea)

- In-Band Mobile Digital TV Transmission Technology for 4D-1 Advanced Television Systems Committee JuneHee Lee (Samsung Electronics, Korea)
- 4D-2 In-Vehicle Media Processors for Driver Assistant Systems Shorin Kyo (NEC, Japan)
- 4D-3 Multi-Core DSP for Base Stations: Large and Small Doug Pulley (picoChip, UK)
- 4D-4 1-cc Computer Using UWB-IR for Wireless Sensor Network Tatsuo Nakagawa (Hitachi, Japan)

30

Wednesday, January 23, 13:30-15:35 Room 310A 5A: Techniques for Formal and Simulation-Based Verification

- Chair: Sherief Reda (Brown Univ., USA) Jin-Young Choi (Korea Univ., Korea)
- 5A-1 Verifying Full-Custom Multipliers by Boolean Equivalence Checking and an Arithmetic Bit Level Proof Udo Krautz, Markus Wedler, Wolfgang Kunz (Univ. Kaiserslautern, Germany), Kai Weber, Christian Jacobi, and Matthias Pflanz (IBM, Germany),
- 5A-2 A Symbolic Approach for Mixed-Signal Model Checking Alexander Jesser and Lars Hedrich (Johann Wolfgang Goethe Universität Frankfurt a.m., Germany)
- 5A-3 Faster Projection Based Methods for Circuit Level Verification Chao Yan and Mark Greenstreet (Univ. of British Columbia, Canada)
- 5A-4 A Debug Probe for Concurrently Debugging Multiple Embedded Cores and Inter-Core Transactions in NoC-Based Systems Shan Tang and Qiang Xu (The Chinese Univ. of Hong Kong, Hong Kong)
- 5A-5(\$) Fast Two-Pass HDL Simulation with On-Demand Dump Kyuho Shim (Pusan Nat'l Univ., Korea), Youngrae Cho, Namdo Kim (Samsung Electronics, Korea), Hyuncheol Baik, Kyungkuk Kim, Dusung Kim (Pusan Nat'l Univ., Korea), Jaebum Kim, Byeongun Min, Kyumyung Choi (Samsung Electronics, Korea), Maciej Ciesielski (Logic-Mill Technology, USA), and Seiyang Yang (Pusan Nat'l Univ., Korea)

Wednesday, January 23, 13:30-15:35					Roo	om 310BC
5B: Power	and	Performance	Optimization	for	Embedded	Systems

- Chair: Naehyuck Chang (Seoul Nat'l Univ., Korea) Tohru Ishihara (Kyushu Univ., Japan)
- 5B-1 Hybrid Solid-State Disks: Combining Heterogeneous NAND Flash in Large SSDs Li-Pin Chang (Nat'l Chiao Tung Univ., Taiwan)

5B-2 Enabling Run-Time Memory Data Transfer Optimizations at the System Level with Automated Extraction of Embedded Software Metadata Information Alexandros Bartzas (Democritus Univ., Greece), Miguel Peon-Quiros (Univ. Complutense de Madrid, Spain), Stylianos Mamagkakis, Francky Catthoor (IMEC vzw, Belgium), Dimitrios Soudris (Democritus Univ., Greece), and Jose M. Mendias (Univ. Complutense de Madrid, Spain)

5B-3 Automatic Re-Coding of Reference Code into Structured and Analyzable SoC Models Pramod Chandraiah and Rainer Dömer (Univ. of California, Irvine, USA)

- 5B-4 Action Coverage Formulation for Power Optimization in Body Sensor Networks Hassan Ghasemzadeh, Eric Guenterberg, Katherine Gilani, and Roozbeh Jafari (Univ. of Texas, Dallas, USA)
- 5B-5(\$) Dynamic Scheduling of Imprecise-Computation Tasks in Maximizing QoS under Energy Constraints for Embedded Systems Heng Yu, Bharadwaj Veeravalli, and Yajun Ha (Nat'l Univ. of Singapore, Singapore)

Wednesday, January 23, 13:30-15:35	Room	311A
5C: Thermal Analysis and DFM		

- Chairs: Takashi Sato (Tokyo Inst. of Tech., Japan) Hideki Asai (Shizuoka Univ., Japan)
- 5C-1 Architecture-Level Thermal Behavioral Characterization for Multi-Core Microprocessors Duo Li, Sheldon X.-D. Tan (Univ. of California, Riverside, USA), and Murli Tirumala (Intel, USA)
- 5C-2 Full-Chip Thermal Analysis for the Early Design Stage via Generalized Integral Transforms Pei-Yu Huang, Chih-Kang Lin, and Yu-Min Lee (Nat'l Chiao Tung Univ., Taiwan)
- 5C-3 A Stochastic Local Hot Spot Alerting Technique Hwisung Jung and Massoud Pedram (Univ. of Southern California, USA)
- 5C-4 Design Rule Optimization of Regular Layout for Leakage Reduction in Nanoscale Design Anupama R. Subramaniam, Ritu Singhal, Chi-Chao Wang, and Yu Cao (Arizona State Univ., USA)
- 5C-5 Investigation of Diffusion Rounding for Post-Lithography Analysis Puneet Gupta (Univ. of California, Los Angeles, USA), Andrew B. Kahng (Univ. of California, San Diego, USA), Youngmin Kim (Univ. of Michigan, Ann Arbor, USA), Saumil Shah (Blaze DFM,

USA), and Dennis Sylvelster (Univ. of Michigan, Ann Arbor, USA)

Wednesday, January 23, 13:30-15:35	Room 311BC				
5D: Designers' Forum (Panel): Are System	Level EDA				
Tools/Methodologies Coming?					

Moderator: Ren-Song Tsay (Nat'l Tsing Hua Univ., Taiwan)

Panelists: Raul Camposano (Xoomsys, USA) Toshihiro Hattori (Renesas Technology, Japan) Austin Kim (Samsung Electronics, Korea) Howard Mao (Springsoft, Taiwan) Sri Parameswaran (Univ. of New South Wales, Australia) Wednesday, January 23, 15:50-17:55

6A: Trends in Timing

- Chairs: Youngsoo Shin (KAIST, Korea) Jung Yun Choi (Samsung Electronics, Korea)
- 6A-1 Pessimism Reduction in Coupling-Aware Static Timing Analysis Using Timing and Logic Filtering Debasish Das (Northwestern Univ., USA), Kip Killpack, Chandramouli Kashyap, Abhijit Jas (Intel, USA), and Hai Zhou (Northwestern Univ., USA)
- 6A-2 A Fast Incremental Clock Skew Scheduling Algorithm for Slack Optimization Kui Wang, Hao Fang, Hu Xu, and Xu Cheng (Peking Univ., China)
- 6A-3 Clock Tree Synthesis with Data-Path Sensitivity Matching Matthew Guthaus (Univ. of California, Santa Cruz, USA), Dennis Sylvester (Univ. of Michigan, USA), and Richard Brown (Univ. of Utah, USA)
- 6A-4 Buffered Clock Tree Synthesis for 3D ICs under Thermal Variations Jacob Minz (Synopsys, USA), Xin Zhao, and Sung Kyu Lim (Georgia Inst. of Tech., USA)
- 6A-5(\$) A Delay Model for Interconnect Trees Based on ABCD Matrix Guofei Zhou, Li Su, Depeng Jin, and Lieguang Zeng (Tsinghua Univ., China)
- 6A-6(\$) Analytical Model for the Impact of Multiple Input Switching Noise on Timing Rajeshwary Tayade (Univ. of Texas, Austin, USA), Sani Nassif (IBM, USA), and Jacob Abraham (Univ. of Texas, Austin, USA)

Wednesday, January 23, 15:50-17:55 Room 310BC 6B: Statistical Modeling and Yield Prediction

- Chairs: Sheldon Tan (Univ. of California, Riverside, USA) Woojin Jin (Samsung Electronics, Korea)
- 6B-1 Determination of Optimal Polynomial Regression Function to Decompose On-Die Systematic and Random Variations Takashi Sato, Hiroyuki Ueyama, Noriaki Nakayama, and Kazuya Masu (Tokyo Inst. of Tech., Japan)
- 6B-2 Within-Die Process Variations: How Accurately Can They Be Statistically Modeled? Brendan Hargreaves, Henrik Hult, and Sherief Reda (Brown Univ., USA)
- 6B-3 Chebyshev Affine Arithmetic Based Parametric Yield Prediction under Limited Descriptions of Uncertainty Jin Sun, Yue Huang (Univ. of Arizona, USA), Jun Li (Anova Solutions, USA), and Janet M. Wang (Univ. of Arizona, USA)
- **6B-4** Distribution Arithmetic for Stochastical Analysis Markus Olbrich and Erich Barke (Leibniz Univ. of Hannover, Germany)

6B-5 Handling Partial Correlations in Yield Prediction Sridhar Varadan (Texas A&M Univ., USA), Janet Wang (Univ. of Arizona, USA), and Jiang Hu (Texas A&M Univ., USA)

Wednesday, January 23, 15:50-17:55 6D: Special Session (Panel): How to Design Cool Chips for Hot Products

Organizers: Massoud Pedram (Univ. of Southern California, USA) Farzan Fallah (Fujitsu Labs of America, USA)

Moderator: Massoud Pedram (Univ. of Southern California, USA)

Panelists: Giovanni De Micheli (EPFL, Switzerland) Jan M. Rabaey (Univ. of California, Berkeley, USA) Soo-Kwan Eo (Samsung Electronics, Korea)



Thursday, January 24, 09:00-10:00

Keynote Address III

Chair: Soonhoi Ha (Seoul Nat'l Univ., Korea)

The Future of Semiconductor Industry - A Foundry's Perspective F. C. Tseng (TSMC, Taiwan)

Thursday,	January	24, 10:15-12:20	Room 310A
	7A:	Reliable/Testable Design Techniques	

Chairs: Huawei Li (Chinese Academy of Sciences, China) Sungho Kang (Yonsei Univ., Korea)

- 7A-1 Soft Error Rate Reduction Using Redundancy Addition and Removal Kai-Chiang Wu and Diana Marculescu (Carnegie Mellon Univ., USA)
- 7A-2 Localized Random Access Scan: Towards Low Area and Routing Overhead Yu Hu, Xiang Fu, Xiaoxin Fan (Chinese Academy of Sciences, China), and Hideo Fujiwara (NAIST, Japan)
- 7A-3 A Design-for-Diagnosis Technique for Diagnosing Both Scan Chain Faults and Combinational Circuit Faults Fei Wang, Yu Hu, Hua-Wei Li, and Xiao-Wei Li (Chinese Academy of Sciences, China)
- 7A-4 GECOM: Test Data Compression Combined with All Unknown Response Masking Youhua Shi, Nozomu Togawa, Masao Yanagisawa, and Tatsuo Ohtsuki (Waseda Univ., Japan)

Thursday, January 24,	10:15-12:20		Room	310BC
7B:	Communication a	and Interfaces		

- Chairs: Maziar Goudarzi (Kyushu Univ., Japan) Hiroyuki Yagi (STARC, Japan)
- 7B-1 Mixed Integer Linear Programming-Based Optimal Topology Synthesis of Cascaded Crossbar Switches Minje Jun (Yonsei Univ., Korea), Sungjoo Yoo (Samsung Electronics, Korea), and Eui-Young Chung (Yonsei Univ., Korea)
- 7B-2 Automatic Interface Synthesis Based on the Classification of Interface Protocols of IPs ChangRyul Yun (ADD, Korea), DongSoo Kang (Chungnam Nat'l Univ., Korea), YoungHwan Bae, HanJin Cho (ETRI, Korea), and KyoungSon Jhang (Chungnam Nat'l Univ., Korea)
- 7B-3 The Shining Embedded System Design Methodology Based on Self Dynamic Reconfigurable Architectures
 C. A. Curino, L. Fossati, V. Rana, F. Redaelli, M. D. Santambrogio, and D. Sciuto (Politecnico di Milano, Italy)

7B-4(\$) Robust On-Chip Bus Architecture Synthesis for MPSoC under Random Tasks Arrival

Sujan Pandey (NXP Semiconductors Research, The Netherlands) and Rolf Drechsler (Univ. of Bremen, Germany)

7B-5(\$) A Multi-Processor NoC Platform Applied on the 802.11i TKIP Cryptosystem

Jung-Ho Lee, Sung-Rok Yoon, Kwang-Eui Pyun, and Sin-Chong Park (ICU, Korea)

Thursday,	January :	24,	10:15-	12:20			Room	311A
	70	D: F	Power:	Delivery	and	Reduction		

Chairs: Ki-Seok Chung (Hanyang Univ., Korea) Junhyung Um (Samsung Electronics, Korea)

- 7C-1 A Unified Methodology for Power Supply Noise Reduction in Modern Microarchitecture Design Michael Healy, Fayez Mohamood, Hsien-Hsin S. Lee, and Sung Kyu Lim (Georgia Inst. of Tech., USA)
- 7C-2 Heuristic Power/Ground Network and Floorplan Co-Design Method Xiaoyi Wang, Jin Shi, Yici Cai, and Xianlong Hong (Tsinghua Univ., China)
- 7C-3 Vertical Via Design Techniques for Multi-Layered P/G Networks Shuai Li, Jin Shi, Yici Cai, and Xianlong Hong (Tsinghua Univ., China)
- 7C-4 Statistical Mixed V_t Allocation of Body-Biased Circuits for Reduced Leakage Variation Jinseob Jeong, Seungwhun Paik, and Youngsoo Shin (KAIST, Korea)
- 7C-5 Exploring High-Speed Low-Power Hybrid Arithmetic Units at Scaled Supply and Adaptive Clock-Stretching Swaroop Ghosh and Kaushik Roy (Purdue Univ., USA)

Thursday, January 24, 10:15-12:20 Room 311BC 7D: Special Session (Panel): Concurrent SoC and SiP Designs

Moderator: Wei-Chung Lo (ITRI, Taiwan)

Panelists: C. P. Hung (ASE, Taiwan) Lung Chu (Cadence Design Systems, USA) Joungho Kim (KAIST, Korea) Epan Wu (VIA Technologies, Taiwan)

36

Thursday, January 24, 13:30-15:35

Room 310A

8A: Test Generation and Test Power

- Chairs: Dong S. Ha (Verginia Tech., USA) Yu Hu (Chinese Academy of Sciences, China)
- 8A-1 Circuit Lines for Guiding the Generation of Random Test Sequences for Synchronous Sequential Circuits Irith Pomeranz (Purdue Univ., USA) and Sudhakar M. Reddy (Univ. of Iowa, USA)
- 8A-2 A New Low Energy BIST Using A Statistical Code Sunghoon Chun, Taejin Kim, and Sungho Kang (Yonsei Univ., Korea)
- 8A-3(\$) On Reducing Both Shift and Capture Power for Scan-Based Testing

Jia Li (Chinese Academy of Sciences, China), Qiang Xu (The Chinese Univ. of Hong Kong, Hong Kong), Yu Hu, and Xiaowei Li (Chinese Academy of Sciences, China)

- 8A-4(\$) Robust Test Generation for Power Supply Noise Induced Path Delay Faults Xiang Fu, Huawei Li, Yu Hu, and Xiaowei Li (Chinese Academy of Sciences, China)
- 8A-5(\$) Test Vector Chains for Increased Targeted and Untargeted Fault Coverage Irith Pomeranz (Purdue Univ., USA) and Sudhakar M. Reddy (Univ. of Iowa, USA)
- 8A-6(\$) Parallel Fault Backtracing for Calculation of Fault Coverage Raimund Ubar, Sergei Devadze, Jaan Raik, and Artur Jutman (Tallinn Univ. of Tech., Estonia)

Thursday, January 24, 13:30-15:35 Room 310BC 8B: Design Space Exploration

- Chairs: Sri Parameswaran (Univ. of New South Wales, Australia) Rainer Dömer (Univ. of California, Irvine, USA)
- 8B-1 ReSP: A Non-Intrusive Transaction-Level Reflective MPSoC Simulation Platform for Design Space Exploration Giovanni Beltrame (European Space Agency, The Netherlands), Cristiana Bolchini, Luca Fossati, Antonio Miele, and Donatella Sciuto (Politecnico di Milano, Italy)
- 8B-2 Collaborative Hardware/Software Partition of Coarse-Grained Reconfigurable System Using Evolutionary Ant Colony Optimization Dawei Wang, Sikun Li, and Yong Dou (Univ. of Defense Tech., China)
- 8B-3 Design Space Exploration for a Coarse Grain Accelerator Farhad Mehdipour, Hamid Noori (Kyushu Univ., Japan), Morteza Saheb Zamani (Amirkabir Univ. of Tech., Iran), Koji Inoue, and Kazuaki Murakami (Kyushu Univ., Japan)

- 8B-4 Efficient Symbolic Multi-Objective Design Space Exploration Martin Lukasiewycz, Michael Glaβ, Christian Haubelt, and Jürgen Teich (Univ. of Erlangen-Nuremberg, Germany)
- 8B-5(\$) Scalable Unified Dual-Radix Architecture for Montgomery Multiplication in *GF(P)* and *GF(2n)* Kazuyuki Tanimura, Ryuta Nara, Shunitsu Kohara, Kazunori Shimzu, Youhua Shi, Nozomu Togawa, Masao Yanaiswa, and Tatsuo Ohtsuki (Waseda Univ., Japan)

Thursday, January 24, 13:30-15:35	Room	311A
8C: Reliability and Power Management		

- Chairs: Koji Inoue (Kyushu Univ., Japan), Masaaki Kondo (The Univ. of Tokyo, Japan)
- 8C-1 Optimal Allocation and Placement of Thermal Sensors for Reconfigurable Systems and Its Practical Extension ByungHyun Lee and Taewhan Kim (Seoul Nat'l Univ., Korea)
- 8C-2 Exploring Power Management in Multi-Core Systems Reinaldo Bergamaschi (IBM, USA), Guoling Han (Univ. of California, Los Angeles, USA), Alper Buyuktosunoglu (IBM, USA), Hiren Patel (Virginia Tech., USA), Indira Nair, Gero Dittmann, Geert Janssen, Zhigan Hu, Pradip Bose, and John Darringer (IBM, USA)
- 8C-3 Dependability, Power, and Performance Trade-Off on a Multicore Processor Toshinori Sato (Kyushu Univ., Japan) and Toshimasa Funaki (Kyushu Inst. of Tech., Japan)
- 8C-4 High Performance Current-Mode Differential Logic Ling Zhang (Univ. of California, San Diego, USA), Jianhua Liu (Altera, USA), Haikun Zhu (Qualcomm, USA), Chung-Kuan Cheng (Univ. of California, San Diego, USA), and Masanori Hashimoto (Osaka Univ., Japan)
- 8C-5 NBTI Induced Performance Degradation in Logic and Memory Circuits: How Effectively Can We Approach a Reliability Solution? Kunhyuk Kang, Saakshi Gangwal, Sang Phill Park, and Kaushik Roy (Purdue Univ., USA)

Thursday,	January	24,	13:30-1	15:35				Room	311BC
	8D:	Des	igners'	Forum:	Low	Power	Chips		

Chair: Kang Yi (Handong Global Univ., Korea)

- 8D-1 Reaching the Limits of Low Power Design J. S. Hobbs and T. W. Williams (Synopsys, USA)
- 8D-2 Software-Cooperative Power-Efficient Heterogeneous Multi-Core for Media Processing Hiroaki Shikano, Masaki Ito, Kunio Uchiyama, Toshihiko Odaka (Hitachi, Japan), Akihiro Hayashi, Takeshi Masuura, Masayoshi Mase, Jun Shirako, Yasutaka Wada, Keiji Kimura, and Hironori Kasahara (Waseda Univ., Japan)

38

- 8D-3 Experiences of Low Power Design Implementation and Verification Shi-Hao Chen and Jiing-Yuan Lin (Global Unichip, Taiwan)
- 8D-4 Low Power Architecture Design Techniques for Mobile Handset LSI Medity[™] M2 Shuichi Kunie, Takefumi Hiraga, Tatsuya Tokue, Sunao Torii, and Taku Ohsawa (NEC, Japan)

Thursday, Jan	uary 24,	15:50-17:55			Room	310A
	9A:	Analog/RF/Mixed	Signal	CAD		

Chairs: Seonghwan Cho (KAIST, Korea), Zhiping Yu (Tsinghua Univ., China)

- 9A-1 An Efficient, Fully Nonlinear, Variability-Aware Non-Monte-Carlo Yield Estimation Procedure with Applications to SRAM Cells and Ring Oscillators Chenjie Gu and Jaijeet Roychowdhury (Univ. of Minnesota, USA)
- 9A-2 Analog Circuit Simulation Using Range Arithmetics Darius Grabowski, Markus Olbrich, and Erich Barke (Leibniz Univ. of Hannover, Germany)
- 9A-3(\$) LTCC Spiral Inductor Modeling, Synthesis, and Optimization Tuck Boon Chan, Hsin-Chia Lu, Jun-Kuei Zeng, and Charlie Chung-Ping Chen (Nat'l Taiwan Univ., Taiwan)
- 9A-4(\$) Symmetry Constraint Based on Mismatch Analysis for Analog Layout in SOI Technology Jiayi Liu, Sheqin Dong, Xianlong Hong, Yibo Wang, Ou He (Tsinghua Univ., China), and Satoshi Goto (Waseda Univ., Japan)

Thursday, January 24, 15:50-17:55 Room 310BC 9B: Architecture Exploration

- Chairs: Takao Onoye (Osaka Univ., Japan) Yun-Nan Chang (Nat'l Sun Yat-sen Univ., Taiwan)
- 9B-1 SPKM : A Novel Graph Drawing Based Algorithm for Application Mapping onto Coarse-Grained Reconfigurable Architectures Jonghee W. Yoon (Seoul Nat'l Univ., Korea), Aviral Shrivastava (Arizona State Univ., USA), Sanghyun Park, Minwook Ahn (Seoul Nat'l Univ., Korea), Reiley Jeyapaul (Arizona State Univ., USA), and Yunheung Paek (Seoul Nat'l Univ., Korea)

9B-2 Block Remap with Turnoff: A Variation-Tolerant Cache Design Technique Mohammed Abid Hussain (Int'l Inst. of Information Tech., Hyderabad, India) and Madhu Mutyam (Indian Inst. of Tech. Madras, India)

- 9B-3 ORB: An On-Chip Optical Ring Bus Communication Architecture for Multi-Processor Systems-on-Chip Sudeep Pasricha and Nikil Dutt (Univ. of California, Irvine, USA)
- 9B-4 Webpage-Based Benchmarks for Mobile Device Design Marc Somers and JoAnn M. Paul (Virginia Tech., USA)

Thursday, January 24, 15:50-17:55	Room 311A+311BC
9D: Designers' Forum	(Panel): Best Ways to
Use Billions of D	evices on a Chip

Moderator: Grant Martin (Tensilica, USA)

Panelists: Deming Chen (Univ. of Illinois, Urbana-Champaign, USA) Nikil Dutt (Univ. of California, Irvine, USA) Joerg Henkel (Karlsruhe Univ., Germany) Kyungho Kim (Samsung Electronics, Korea) Kazutoshi Kobayashi (Kyoto Univ., Japan)

Tutorials

Monday, January 21, 09:	00-17:30		Room 3	10A
	Tutorial 1	(Full Day)		
System-Level Synthesis:	Functions,	Architectures,	and Communicat	ions

Speakers: Alberto Sangiovanni Vincentelli (Univ. of California, Berkeley, USA) Jason Cong (Organizer, Univ. of California, Los Angeles, USA) Radu Marculescu (Carnegie Mellon Univ. USA) Clas A. Jacobson (United Technologies Research Center, USA)

Abstract: Each of the grand themes in the future of design of integrated systems and circuits proposes to develop solutions addressing a particular problem, such as power, concurrency, variability or reliability, and brings together aspects from multiple communities such as modeling, architecture exploration, design synthesis, verification, and test. To do this successfully requires an underlying and common design technology framework for complex heterogeneous systems, which can be shared over technology domains and optimization targets. At GSRC, we have expended considerable effort in developing the basic foundations for such a framework. Yet, while we have made major inroads, plenty of challenges remain to be resolved if we want to successfully address the challenges raised by the technology advances. More specifically, the following design needs can be identified:

- Formal specifications that include declarative and operational components expressed in continuous and discrete time domains.
- Design as a formally verified refinement process on a set of consistent abstraction layers where appropriate interfaces are built to handle heterogeneous signal domains, thereby ensuring vertical consistency.
- Optimized and automatic design space exploration with heterogeneous implementation architectures.
- Mapping of functionality onto architectures exploiting multi-processor optimized compilers, high-level hardware synthesis, and automatic communication synthesis.
- Automatic extraction of architecture models with stochastic models to capture uncertainties typical of nano-fabrics and mapping of functionalities onto these architectures with optimization of expected performance and cost.
- An integration framework based on formalized models where the design process can be adaptively defined according to the application domain and offering the opportunity to different constituencies to leverage each other's work.

This tutorial covers recent advances in system-level design and synthesis achieved in the core foundations for heterogeneous system-level design of the Giga-scale System- level Research Center (GSRC). We start with the foundations of the methodology posed as the basis for the multi-year effort of this theme that has been adopted broadly in industry: platform-based design. Following the introduction of the overall methodology, we proceed to present the development of an integration framework, Metropolis II, that builds upon the work of

Metropolis. This framework aims at the system design problem where software and hardware are important implementation methods but are determined by overall system consideration and specification. We describe the execution semantics as well as the modeling approach we have followed. This framework and the methodology it supports are exemplified with a few test cases taken from our industrial partners in particular, automobiles and building management. The second part of the tutorial presents recent developments in automatic system level synthesis for complex functional blocks starting from behavior- level specification such as C, C++, SystemC, or Metropolis metamodels. We will present latest results on constraint-driven scheduling from totally untimed models or partially timed models, resource binding and microarchitecture generation for area, performance, and power optimization, and simultaneous behavior and communication synthesis. We shall also present the results on synthesis of application-specific instruction-set processor (ASIPs) as an alternative solution for efficient implementation of the complex function blocks. These techniques have been integrated into the xPilot synthesis system and we shall discuss its results on several real-life examples. The third part of the tutorial addresses the emerging area of NoC design and presents several research issues where the concept of "network" is at the forefront of multi-core processing. Specifically, we plan to discuss performance models and optimization techniques that can be used to design different NoC architectures for multimedia applications, while reasoning about performance, energy, and fault-tolerance tradeoffs. To better understand the advantages in terms of area, performance, and energy consumption offered by the NoC approach, we discuss a concrete NoC-based implementation of an MPEG-2 encoder and provide direct measurements using an FPGA prototype and actual video clips. Finally, we present the practice and results of these state-of-art system-level design and synthesis techniques in an industrial setting. In particular the system level design issues that arise in incorporating networked embedded systems in infrastructure areas (building functionality, HVAC/R, power generation and distribution) are covered through several examples.

Monday, January 21, 09:00-17:30	Room 310BC
Tutorial 2 (Full Day) Cross-Layer Approaches to Designing Reliable Syst Unreliable Chips	tems using

Speakers: Nikil Dutt (Organizer, Univ. of California, Irvine, USA) Fadi Kurdahi (Univ. of California, Irvine, USA) Ahmed Eltawil (Univ. of California, Irvine, USA) Sani Nassif (IBM, USA)

Abstract: Designers of next generation Systems-on-Chip (SoCs) face daunting challenges in generating high yielding architectures that integrate vast amounts of logic and memories in a minimum die size, while simultaneously minimizing power consumption. Advanced manufacturing technologies will make it economically impractical to insist on a 100% error-free SoC in terms of area and power. Fortunately, many important application domains (e.g., communication and multimedia) are inherently error-aware, allowing a range of designs with a specified Quality of Service (QoS) to be generated. This tutorial addresses this notion of error-awareness across multiple abstraction layers -application,

architectural platform, and technology- for next generation SoCs. The intent is to allow exploration and evaluation of a large, previously invisible design space exhibiting a wide range of power, performance, and cost attributes. To achieve this one must synergistically bring together expertise at each abstraction layer: in communication/multimedia applications, SoC architectural platforms, and advanced circuits/technology, in order to allow effective co-design across these abstraction layers. Such approaches must be validated and tested in real applications. An ideal context for the convergence of such applications are handheld multimedia communication devices in which a WCDMA modem and an H.264 encoder must co-exist, potentially with other applications such as imaging. These applications present an example of a system that has a wide scope, executes in highly dynamic environment and presents interesting opportunities for tradeoff analysis and optimization.

Outline:

I. Technology Modeling

The tutorial begins with the technological trends that highlight the increasing error-prone design process in advanced process technologies, and motivates the need for error-awareness.

II. Application Level Error-Aware Design

Following that, we highlight approaches for error-aware design processes using typical application drivers. These applications include wireless communication systems, multimedia systems, and imaging systems. The concept of yield is extended beyond manufacturing yield to its broader perspective encompassing power, performance and error tradeoffs, enabling new dimensions of system tradeoffs.

III. Platform and higher level design tradeoffs

This concept is then raised and then extended to the software/ architectural domain, considering processors and memories, as well as upper protocol layers. Case studies are presented throughout the tutorial.

Monday, January 21	, 09:00-12:30			Room 311A
	Tutorial	3 (Half Day)		
Latest Advances	and Future	Opportunities	on CAD	for FPGAs

Speakers: Deming Chen (Univ. of Illinois, Urbana-Champaign, USA) Martin D. F. Wong (Organizer, Univ. of Illinois, Urbana-Champaign, USA)

Abstract: As cost and complexity for ASIC designs grow in a steady and rapid pace along the technology scaling, FPGA designs offer an attractive alternative. According to research firm Gartner/Dataquest, the year 2007 will see nearly 89,000 FPGA design starts, and will swell to 112,000 in 2010 - some 25 times that of ASICs. As major FPGA vendors pushed out their high-end 65nm platform FPGA chips, new concerns and challenges emerge for the FPGA CAD community. Although CAD for high performance is still an active research area, power and variation-aware synthesis and physical design are increasingly more important and catching people's attention. How much margin is there for optimizing performance and power through new CAD algorithms and techniques that focus on new aspects such as glitch power, multi-clock, and process variation? How can ESL design methodology play a role for FPGA design space exploration? What can we learn from research thrusts such as FPGA floorplan and BDD synthesis? What will be the future challenges and opportunities for FPGA CAD research? In this half-day tutorial, we will introduce the latest advances on CAD for FPGAs and offer our insights on these intriguing and exciting questions.

Monday, January 21,	09:00-12:30	Room	311BC	
Improvements in	Tutorial 4 (Half Day) 65/45nm Physical Implementation	Flow	and	
Methodology				

Speaker: Andrew B. Kahng (Organizer, Univ. of California, San Diego, USA)

This tutorial will discuss new challenges that face developers and users of 65nm and 45nm physical implementation flows, as well as opportunities for improved design turnaround time and quality of result obtained with such flows. The tutorial is targeted to practitioners (CAD integrators, CAD R&D, physical design methodologists, back-end chip implementation groups) as well as students and researchers. Topics covered will include:

- 1. Introduction.
 - a. Technology and library development (design rules, SPICE models, guardbands and process maturation).
 - b. Trajectory of layout styles (e.g., restricted layout rules vs. doublepatterning) and optimization knobs (e.g., multi-Vt vs. adaptive biasing) at 45nm and below.
 - c. Guardbanding. Various sources of guardbanding and their costs with respect to turnaround time and design quality.
- 2. New variability-aware analyses.
 - a. How systematic and random litho, etch, CMP non-idealities will be incorporated into golden characterization and analysis flows
 - b. Stress-induced variability: modeling at circuit and library levels of abstraction (STI width, dual stress liner, etc.)
 - c. Thermal and supply-voltage fluctuation
- 3. New variability-aware optimizations.
 - a. How manufacturing variability can or should be captured in design flows
 - i. Virtual manufacturing flows
 - ii. Statistical optimization flows
 - iii. Correct by construction and construct by correction flows
 - b. Stress mitigations using placement and active-layer fill
 - c. Sensitivity optimizations and 'self-compensating' robust design techniques
- 4. New physical design challenges (and magnitude of significance)
 - a. Library richness and complexities (data management, synthesis/ optimization failures, etc.)
 - b. Double-patterning lithography
 - c. Interconnect reliability

- d. Emerging variation sources beyond-die (reticle- and wafer-scale) and within-die (dopant fluctuations, overlay, line-edge roughness, etc.)
- 5. Differentiating physical design techniques.
 - a. New methodologies for handle the challenges
 - b. "Glue" optimizations: clock and power distribution
 - c. Convergence: detailed placement, detailed routing and circuit optimization
 - d. Direct improvement of yield and reliability

Monday, January 21, 14:00-17:30	Room	311A
Tutorial 5 (Half Day)		
On-Chip Network: State-of-the-Art Industrial	Solution	
and Academic Research		

Organizer: Sungjoo Yoo (Samsung Electronics, Korea) Speakers: David Gwilt (ARM, UK) Axel Jantsch (Royal Inst. of Tech., Sweden)

Abstract: On-chip bus has a significant impact on the area, power, performance and design cycle of complex SoCs. The conventional on-chip bus was based on shared buses and their hierarchical compositions. However, the ever increasing requirements of high frequency, low power, and fast design cycle require innovation in on-chip bus designs for SoCs.

From industrial viewpoint, the innovation seems to apply crossbar (often called bus matrix)-based bus design. Most of academic research tackles more ambitious goals, designing 'network' on a chip.

This tutorial covers recent advances of both industrial solution and academic research towards on-chip network design. In the first part of this tutorial, the presenter, Mr. David Gwilt, who is the engineering director of ARM's System Design Division, provides a tour (sub-title: "AMBA3 technology in the design of on-chip communication and data management infrastructure") through the on-chip bus design issues commonly faced by today's industry leaders in pursuit of high performance, low power and fast time-to-market. State-of-the-art commercial solutions based on crossbar components are then presented, delivering benefits that not only address all the common concerns but many of the less common ones too.

The second part of this tutorial, presented by Prof. Axel Jantsch, will systematically discuss (1) the main elements in a Network on Chip (NoC), i.e. the network interface, the switch and the link, and (2) the main issues in communication networks: topology, routing, switching, flow control and offered communication services. The significance and effect of a two dimensional VLSI implementation will be emphasized throughout the tutorial. A strong emphasis is put on performance, performance models and implications of design decisions on network performance and quality of service will be discussed. A particular approach to analyze worst case performance will be introduced which is based on Network Calculus.

Proceedings

ASP-DAC 2008 proceedings are published in two versions: a paper version and a CD-ROM version. All papers are included in both versions. Conference registration includes both versions of the proceedings. Additional proceedings are available for purchase at the conference. Prices are as follows:

- Paper Version: KRW 45,000 each
- CD-ROM Version: KRW 20,000 each

Banquet

- * Date & Time January 23, 18:30 ~ 20:30
- * Location Room 103, COEX
- * Performance NANTA
- * Additional Ticket KRW 45,000

※ NANTA

Nanta is a nonverbal performance integrating Korean traditional "Samulnori" rhythm with comic and drama. Audiences of all ages and nationalities can enjoy. Nanta made its international debut in 1999 at the Edinburgh Fringe Festival, where it received an award for best performance. Since then, it has been staged in the U.K., Germany, Austria, Italy, Japan, Taiwan, Singapore, The Netherlands, and Australia. With plenty of support from successful oversea performances, in February 2004, Nanta finally opened a long term performance in Broadway New York, being the first in Asia. Nanta is voted to be one of the 10 most famous tourist attractions in Seoul by Korean Tourist Service (300,000 tourists every year).



Venue Information

COEX



ASP-DAC 2008 will be held in the COEX Convention Center in Seoul, Korea. COEX is Asia's premier international convention and exhibition center opened in Seoul, Korea, in the year 2000. At the forefront of globalization, COEX will continue to provide a high-tech venue for international exhibitions, meetings, and cultural events in the 21st century.

Deluxe hotels are within a 2-5 minute walking distance, while a number of other hotels can be reached within 10 minutes by bus or

subway from the venue. The venue also has easy subway access, and taxis and buses are readily available. Furthermore, the Korea City Air Terminal, conveniently located within the complex, offers a non-stop limousine bus service to and from Incheon International Airport.

Seoul

Seoul has been the capital city of Korea for more than 600 years since Joseon Dynasty and the city bears important meaning as the heart of Korea's politics, economics, society and culture. There are a number of invaluable cultural assets in Seoul, a region encompassing cultural features of the northern and southern areas of the Peninsula. Seoul has gained international recognition by successfully holding the '86 Asian Games, the '88 Olympic Games, and the 2002 Korea-Japan World Cup. Among its numerous skyscrapers and glass towers, Seoul presents a number of beautiful palaces and ancient gates in various parts of its downtown core. Tradition and modernity, and nature and humans coexist in this city. Website: http://english.seoul.go.kr/

ASP-DAC 2008 Exhibition

Exhibition Date: January 22~23, 2008 Time: 09:00~18:00



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E-mail	hoonkim@cadence.com	Web Site	www.cadence.com	
Contents of Exhibit	OrCAD PCB design	tools		
Introduction	OrCAD PCB design tools Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence®software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. Cadence reported 2006 revenues of approximately \$1.5 billion, and has approximately 5,300 employees. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products,			

[Booth No. 2]			
Name of Company	Synopsys Korea Inc.		
President	Yong-seok Shin		
Address	12 th Fl., Star Tower, 737, Yeoksam-dong, Kangnam-gu, Seoul, 135-984, Korea.		
Tel	+82-2-3404-2700	Fax	+82-2-558-2148
E-mail	jclee@synopsys.com	Web Site	www.synopsys.com
Contents of Exhibit	Galaxy Platform		
Introduction	Galaxy Platform Synopsys provides electronic design automation (EDA) software and services used to design complex integrated circuit (ICs) and Systems-on-Chip (SoC) for the global semiconductor and electronics industries. Synopsys gives its customers a competitive edge in bringing the best products to market quickly with minimal risk from high-level synthesis to placed gated, Synopsys provides solutions to the most difficult challenges that confront engineers who are pushing electronic design to the limit. Synopsys technology is in the DNA of every important chip in the world. The company was founded in 1996 and now has over 5,000 employees worldwide. 1. Implementation products : DC Ultra, Prime Time, DFT Compiler, TetraMAX, Physical Compiler, Astro, IC Compiler, Hercules, Star RCXT 2. Verification products : OPC, TCAD, Solid-E, YMS/PME, Prime Yield		

[Booth No. 3]				
Name of Company	Flash Memory Resea	Flash Memory Research Group, Seoul National University		
President	Jang-Moo Lee			
Address	599 Gwanangno, Gwanak-gu, Seoul, 151-742, Korea			
Tel	+82-2-880-7047 Fax +82-2-886-7589			
E-mail	symin@archi.snu.ac.kr	Web Site	http://archi.snu.ac.kr	
Contents of Exhibit	Flash Memory-based Embedded Multimedia Software			
Introduction	Flash memory is increasing being used in mobile embedded systems. The Flash Memory-based Embedded Multimedia Software project is supported by the IT R&D program of MIC/IITA in Korea. The project is intended to develop a total software solution for Flash memory including FTL (Flash Transation Layer), file system, and embedded DBMS system			

[Booth No. 4]			
Name of Company	Synplicity Korea		
President	Suk-Ha Lee		
Address	#801-2, 8 Floor Trade Tower, 159-1 Samsung-dong, Kangnam-gu, Seoul, 135-729, Korea		
Tel	+82-2-561-7671	Fax	+82-2-566-7671
E-mail	shlee@synplicity.com	Web Site	www.synplicity.com
Contents of Exhibit	HAPS, Certify, Synplify Premier, Synplify DSP, Identify		
Introduction	Synplicity® Inc. is the leading supplier of innovative software and system solutions for the design and verification of semiconductors.		

[Booth No. 5]			
Name of Company	System Centroid Inc.		
President	Inhag PARK		
Address	#7119 HTVC KAIST, 53-3 Eoeun-dong Yusong-gu, Daejeon, 305-806, Republic of Korea		
Tel	+82-42-862-7747 Fax +82-42-862-7947		
E-mail	ihpark@systemcentroid.com	Web Site	www.systemcentroid.com
Contents of Exhibit	Flowrian, Scenian, K	inowledgeSaf	er, SSi-1
Introduction	Found in 2000 as System Centroid Inc. VHDL, Verilog, Sys debug tools, design web-based SIP (S verification system. System Centroid Inc. technology and web o the collaborative co-we web based sharing centralized design a enable for design e together by accessii through the internet.	an ETRI sp is in business temC langua knowledge n emiconducto is surely the communication orking of design unalysis serv xperts locate ng the centr	in-off venture company, s of developing innovative age based capture and nanagement system and r Intellectual Property) first pioneer fusing EDA technology, which enables sign team members, the n knowledge and the ice. These technologies d in the world to work alized design resources

[Booth No. 6]			
Name of Company	HUINS CO., LTD.		
President	Tae-hun Song		
Address	11F, Kofomo BLD, 16-3, Sunae-Dong, Bundang-Gu, Seongnam-Si, Gyeonggi-Do, 463-825, Korea		
Tel	+82-31-719-8200 (Rep) Fax +82-31-719-8201		
E-mail	bnkim@huins.com	Web Site	www.huins.com
Contents of Exhibit	 * SoC prototyping Platform : RPS-3000, RPS-7000, VIP- 1000/5000, SoCMaster3 * Embedded System : PXA320PRO, Acuman270/270G, PXA255, X-Station * Wireless Sensor Network Kit : USN-AP, USS2400, UBee430/AP * ARM Solution : RealView DS, ICE, H/W Platform 		
Introduction	Huins is headquartered in Korea. Huins is founded in Seoul in 1995. Huins has grown to become one of the leading supplier of SoC Development Kit for prototyping and emulation, Embedded System, SBC, Wireless Sensor Network Kit, Arm Solution Distributor.		

[Booth No. 7]			
Name of Company	Libertron		
President	Man-bok Kim		
Address	3 rd Fl. Nam-jeong Bldg., 362-1, Habjeong-dong, Mapo-gu, Seoul, 121-884, Korea		
Tel	+82-2-3486-5278 Fax +82-2-3486-5271		
E-mail	cho@libertron.com	Web Site	www.libertron.com
Contents of Exhibit	 * FPGA Platform - RoV-Lab3000 - EDA-Mod LX330 * Embedded Platform - SYS-Lab5000 * DSP Platform - DSP-Plus5000 		
Introduction	We have developed FPGA based training kit and instrument for professional ASIC/FPGA designer since 1998. * Proprietary technology development and patents. * R&D Projects sponsored by Government * Co-promotion and marketing in Korea with Xilinx * Technical support for Professors and Engineer related to ASIC/ FPGA		

[Booth No. 8]				
Name of Company	Dynalith Systems Co	Dynalith Systems Co., Ltd., MDS Technology Co., Ltd.		
President	Jong Suk Kim	Jong Suk Kim		
Address	2 nd Fl. Taejin Bldg., 14-2, Yangjae-dong, Seocho-gu, Seoul, 137-888, Korea			
Tel	+82-2-556-0020 Fax +82-2-556-2252			
E-mail	contact@dynalith.com	Web Site	www.dynalith.com	
Contents of Exhibit	HW/SW Co-verification, acceleration and Rapid Prototyping			
Introduction	Dynalith Systems Co., Ltd. founded year 2000, Korea has been producing many innovative SoC design verification solutions that include functional and behavioral-level HW/SW co-verification, cost effective hardware acceleration, and virtual prototyping. Dynalith also provides FPGA-based Prototyping systems, USB2.0 and PCIe based host interface, and software development environment for embedded systems.			

[Booth No. 9]			
Name of Company	Polliwog Corporation		
President	Sun Hue Huh		
Address	463-825, 2F GRATEA, 6-2, SuNae-Dong, BunDangGu, SungNam, GyeongGi-Do, Korea		
Tel	+82-31-712-4128~9 Fax +82-31-712-4139		
E-mail	kssong@polliwogeda.com	Web Site	www.polliwogeda.com
Contents of Exhibit	PollEx Suite (PCB,	CP, SI, DFM	, DFE)
Introduction	Polievogation Established in 2000 Polliwog Corporation has provided the global electronics industry with unique sets of EDA software allowing the users to efficiently verify and evaluate their product designs. We understand the problems and provide the solutions to our customers encountered with ever increasing performance and complexity issues in their design environment. Polliwog's products have been developed based on the inputs from our customers and the needs of leading electronics industry.		

[Booth No. 10]				
Name of Company	SELOCO Inc.	SELOCO Inc.		
President	Young Uk Yu	Young Uk Yu		
Address	3FI. Namyang Bldg., 60-5 Bangi-dong, Songpa-gu, Seoul, 138-828, Korea			
Tel	+82-2-3433-0000 Fax +82-2-3433-0099			
E-mail	sales@seloco.com	Web Site	www.seloco.com	
Contents of Exhibit	ARM ESL, Forte de	sign, HandSh	ake Solution, MyCAD	
Introduction	We are offering the best solution to our customers by providing with the newest and suitable EDA Tool and semiconductors to support companies, educational and research institutes that are developing electronic tele- communication semiconductors and SoC/NoC. We also introduce the world trend to the domestic customers by offering educational information. SELOCO Inc. will continue to increase customer values and contribute to the growth of IT Korea by supplying the newest Tool.			

[Booth No. 11]				
Name of Company	Chungbuk Technopark, Zephyr Logic Inc.			
President	Chuck Jung			
Address	501, Information & Communication Bldg, Far East University Gamgok-myeon, Eumseong-gun, Chungcheongbuk-do, 369-851, Korea			
Tel	043-879-3611	Fax	043-879-3110	
E-mail	hoil.moon@zephyrlogic.com	Web Site	N/A	
Contents of Exhibit	Electro-Static-Discharge(ESD), I/O and Foundry Service			
Introduction	Founded in 2005, Zephyr Logic is the solution provider of high electro-static-discharge(ESD) immunity I/O intellectual property(IP) and foundry service. We focus on high ESD immunity and custom I/O design and consulting for high speed, high voltage and mixed signal applications. We also provide the valued foundry sourcing service to fabless customers.			

[Booth No. 12]				
Name of Company	Magma Korea			
President	Roy E Jewell			
Address	1301 Korea World Trade Center, 159-1, Samseong-dong, Gangnam-gu, Seoul, 135-729, Korea			
Tel	+82-2-6000-3501	Fax	+82-2-6000-3500	
E-mail	jykim@magma-da.com	Web Site	www.magma-da.com	
Contents of Exhibit	Achieving a 2-Day RTL-to-GDSII Turnaround On Any Size Design with Talus			
Introduction	You'll see how Magma's Talus platform provides fundamental advances that accelerate the design cycle, including automated partitioning, time budgeting, relative floorplan constraints, block shaping, pin placement, clock and power synthesis, and final chip assembly. You'll learn how most of these steps can be distributed across a compute network using multiprocessing as well as multithreading technologies . We'll also show you how you can make a major change to the RTL of a multimillion-cell design and still complete the GDSII implementation in less than 2 days. The results of an 8M+ cell hierarchical design implemented using Talus and several underlying technologies related to automatic floorplanning and block implementation will also be presented.			

[Booth No. 13]				
Name of Company	Silvaco			
President	Man-Gyu Hwang			
Address	5F, STAR-CITY Bldg., 469-1, Chonho-Dong, Kangdong-Gu, Seoul, 134-020, Korea			
Tel	+82-2-447-5421	Fax	+82-2-447-5420	
E-mail	hwang@silvaco.com	Web Site	http://www.silvaco.co.kr	
Contents of Exhibit	Process Simulation Software – ATHEN Device Simulation Software – ATLAS Analog Circuit Simulation Software - SmartSpice Full Panel Simulation Software - TwisterFP Layout Design Software - Celebrity / Expert Verification Software - Guardian DRC/LvS			
Introduction	Silvaco International is a leading provider of electronic design automation (EDA) software for analog and mixed- signal integrated circuit design. Founded in 1984, the company delivers proven products for TCAD process and device simulation, Spice parameter extraction, circuit simulation, and custom IC design/verification. The company integrates these best-in-class products with experienced support and engineering services to provide complete analog semi- conductor process, device and design automation solutions in CMOS, Bipolar, SiGe and compound technologies. Worldwide customers include leading fabless semiconductor companies, integrated semiconductor manufacturers, foundries, universities and designers of analog integrated circuits who require the utmost accuracy.			

[Booth No. 14]				
Name of Company	Mentor Graphics			
President	Young-In Yang			
Address	RM2104, Trade Tower, World Trade Center, Samseong-dong, Gangnam-gu, Seoul 135-729, Korea			
Tel	+82-2-3016-4427	Fax	+82-2-551-2336	
E-mail	Angela_cho@mentor.com	Web Site	www. Mentor.com	
Contents of Exhibit	Catapult C synthesis for High level synthesis / Calibre nmDRC			
Introduction	Catapult is for ASIC and FPGA hardware designers of portable wireless, video, and image processing equipment who need to deliver optimal implementations with aggressive time-to-market requirements. Catapult is a high-level synthesis tool that uses industry-standard ANSI C++ to generate correct-by-construction, high-quality RTL 10-100x faster than other methods. DRC has changed from the traditional pass/no pass compliance check to a comprehensive methodology that supports multiple analyses, increased performance and scaling, enhanced productivity, and improved cycle times			



