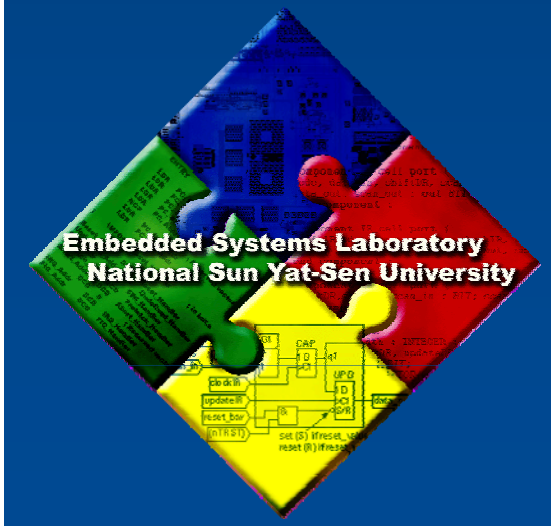
Parameterized Embedded In-Circuit Emulator and Its Retargetable Debugging Software for Microprocessor / Microcontroller / DSP Processor



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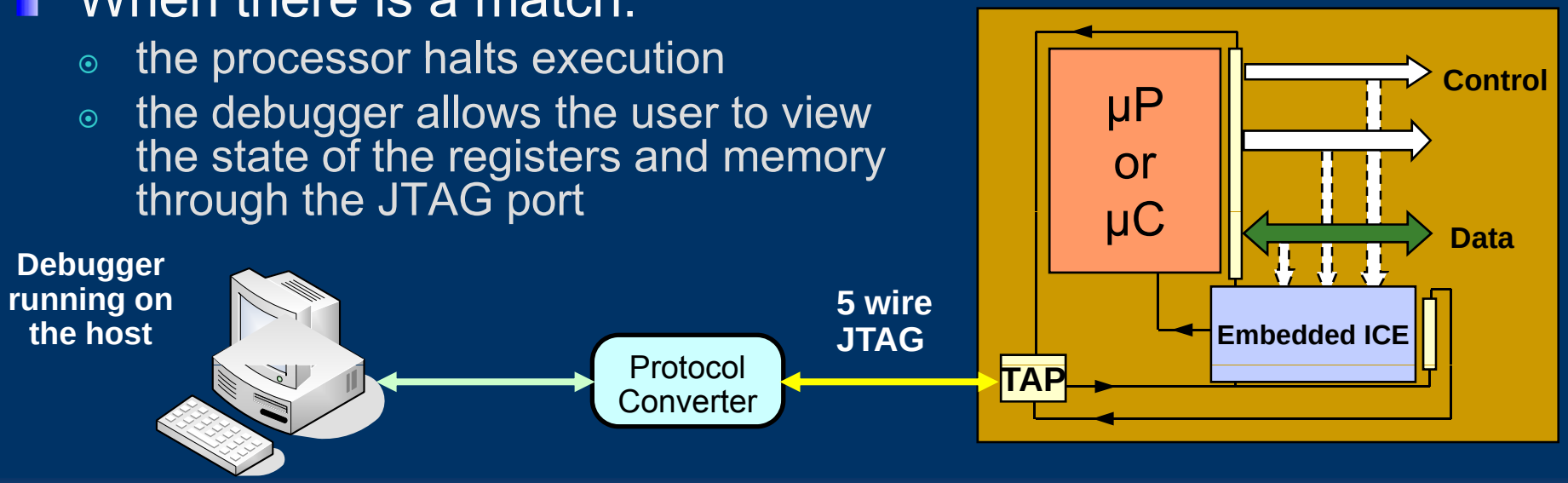
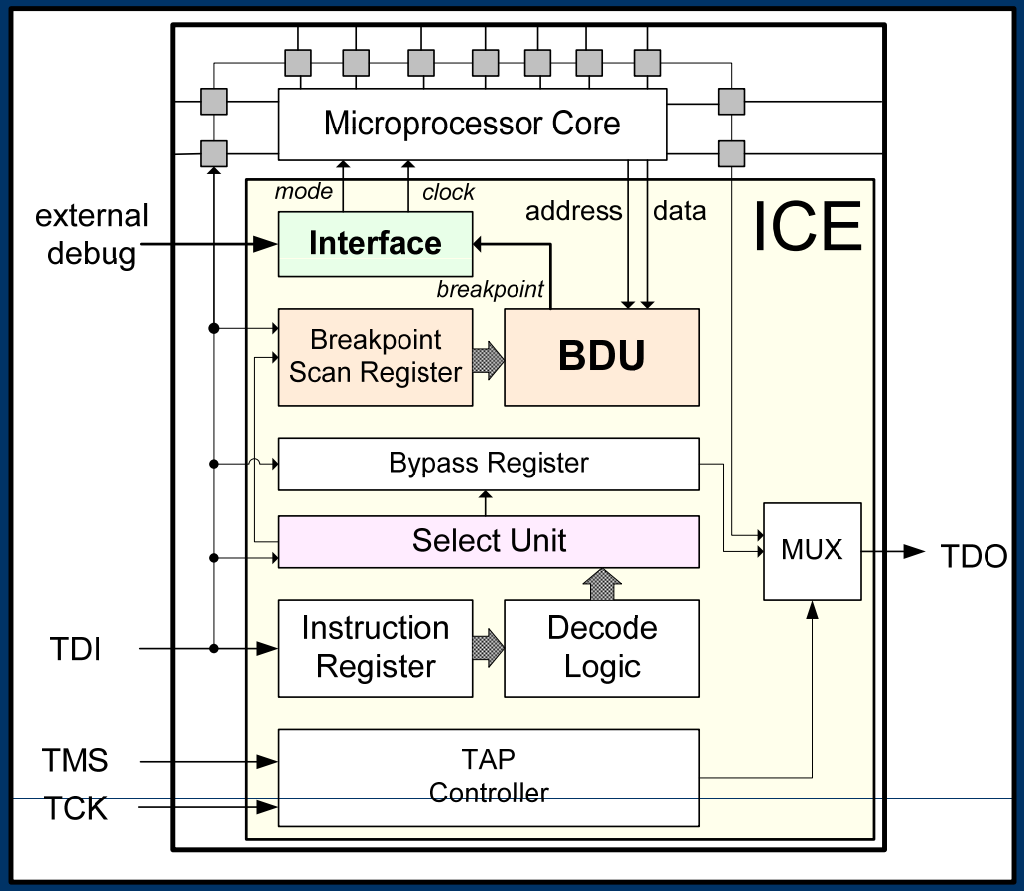
Introduction to Embedded ICE

- Preserve the original behavior of a microprocessor
- Embedded ICE contains hardware breakpoint
- Allows instruction breakpoints and data watchpoints to be set
- Programmable through JTAG
- Comparators monitor:
  - Address bus
  - Data bus
  - Control signals
- When there is a match:
  - the processor halts execution
  - the debugger allows the user to view the state of the registers and memory through the JTAG port



Block Diagram for the Embedded ICE

- Our EICE is based on IEEE 1149.1 with some extensions



JTAG Extensions to Support the EICE Functionality

- Component Modification

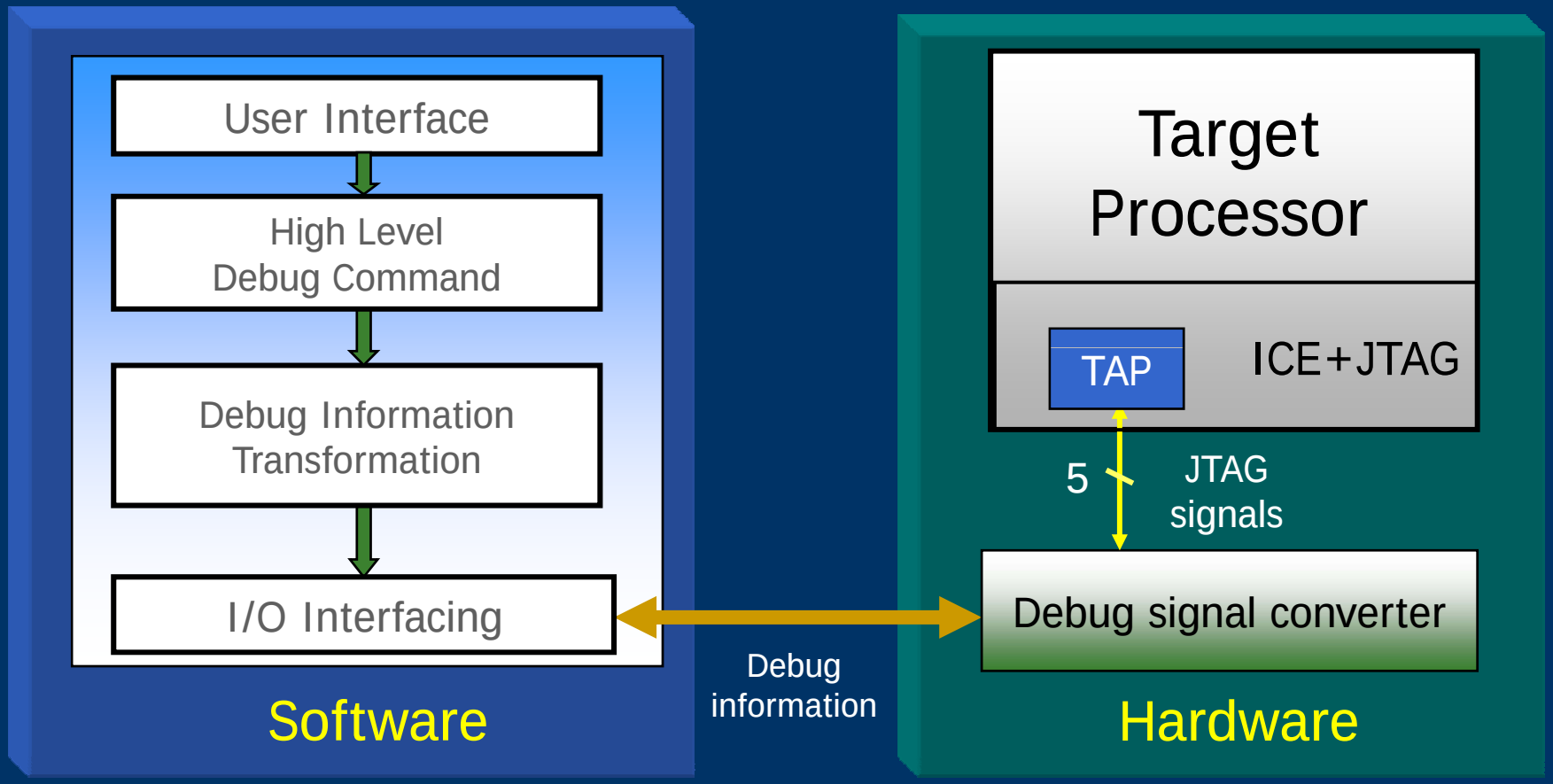
Classification	Components
Original 1149.1 JTAG components	TAP controller, Boundary Scan Registers, Bypass Register
Modified 1149.1 JTAG components	Instruction Register, Instruction Decode Logic, Data Register Selector
New Components	Core Data Register, Breakpoint Scan Register, Scan-Chain Select Register, Breakpoint Detection Unit

Feature

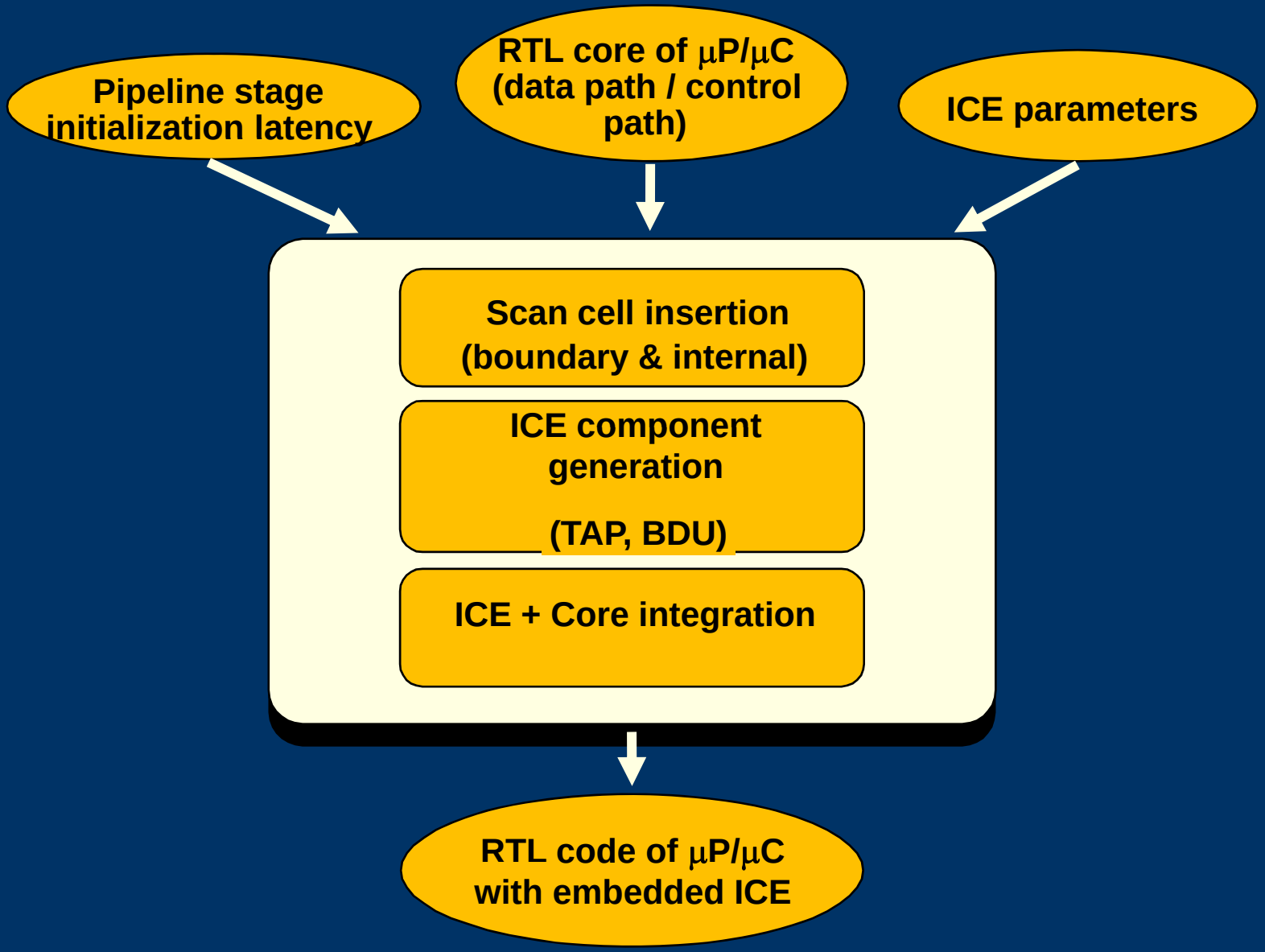
- Reusable ability to Reduce HW/SW Development Cost
  - In general, EICEs are designed for specific targets.
  - Our design can be applied different processors
- Easy to Integrate Embedded ICE IP into Processor

Proposed approach

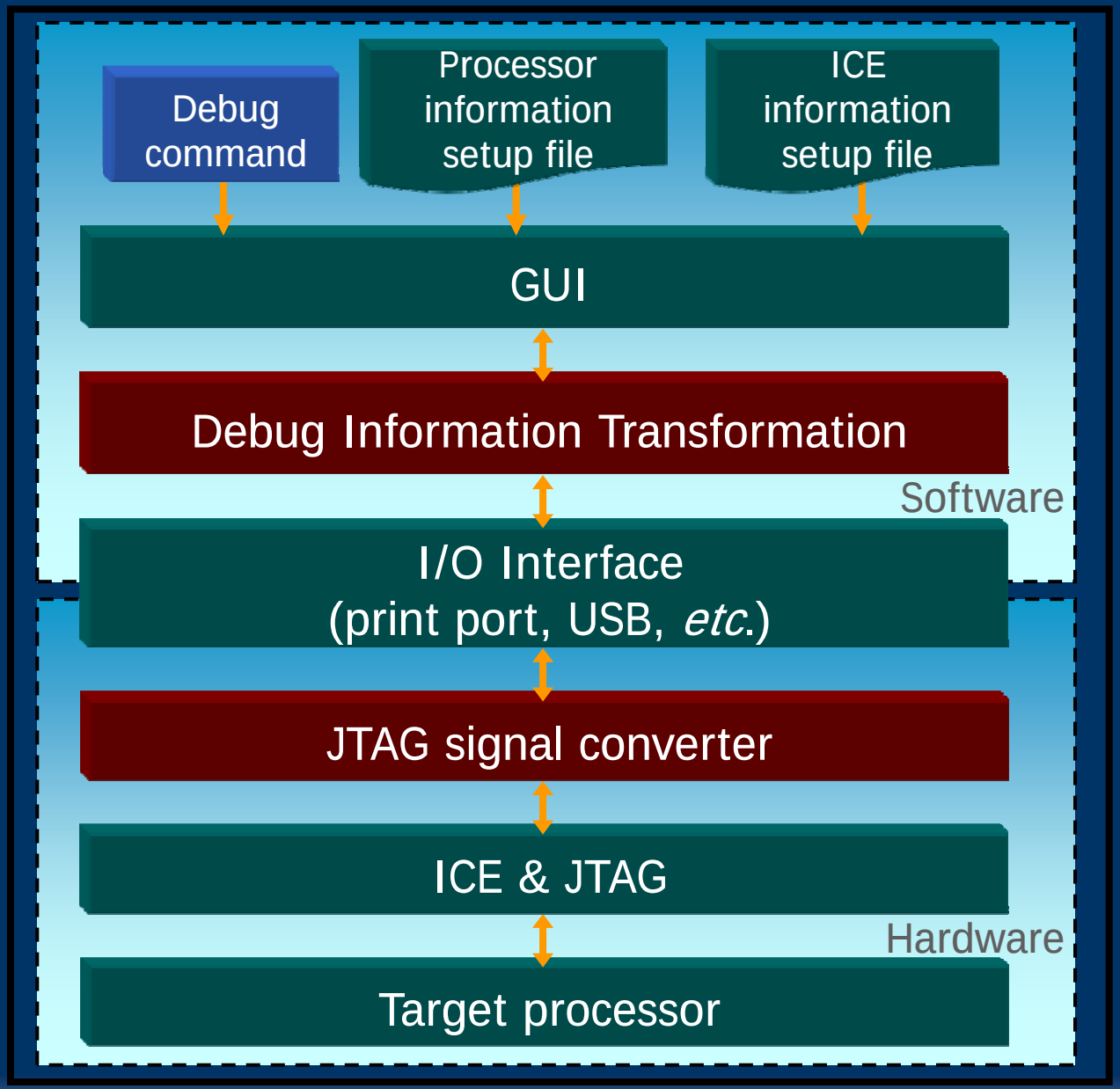
- HW/SW co-generate the debugging information



μP/μC + ICE Integration Flow



Retargetable EICE debugging software



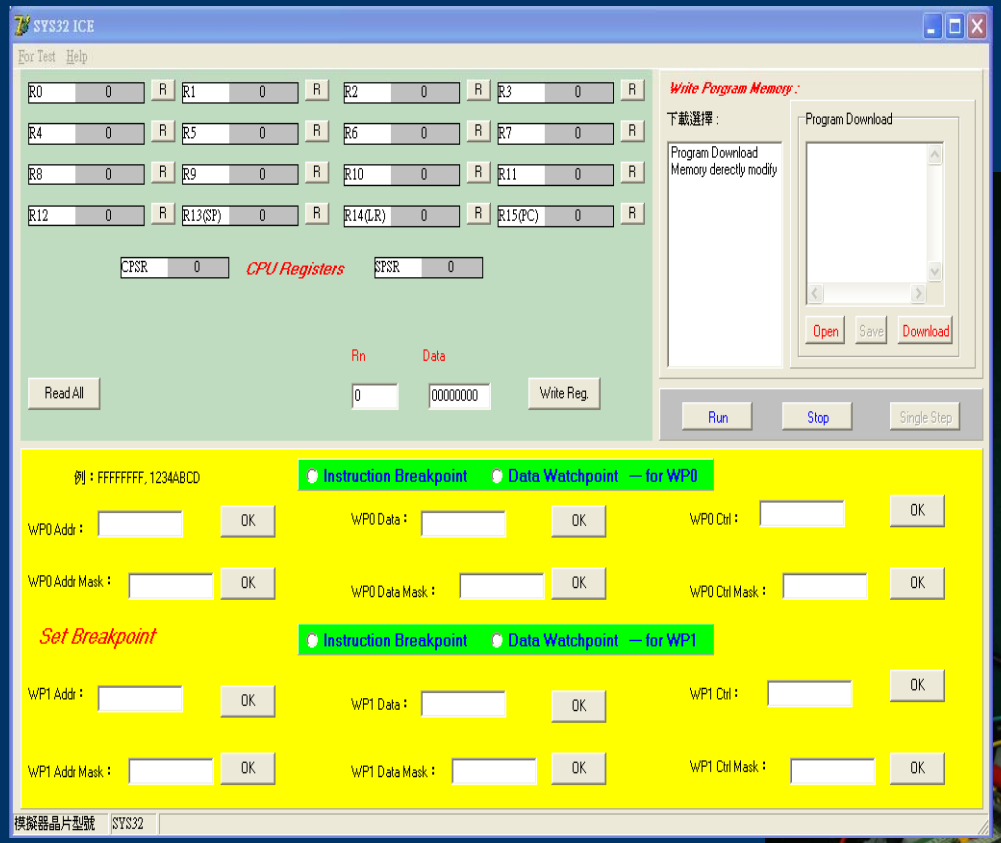
Integration Consideration

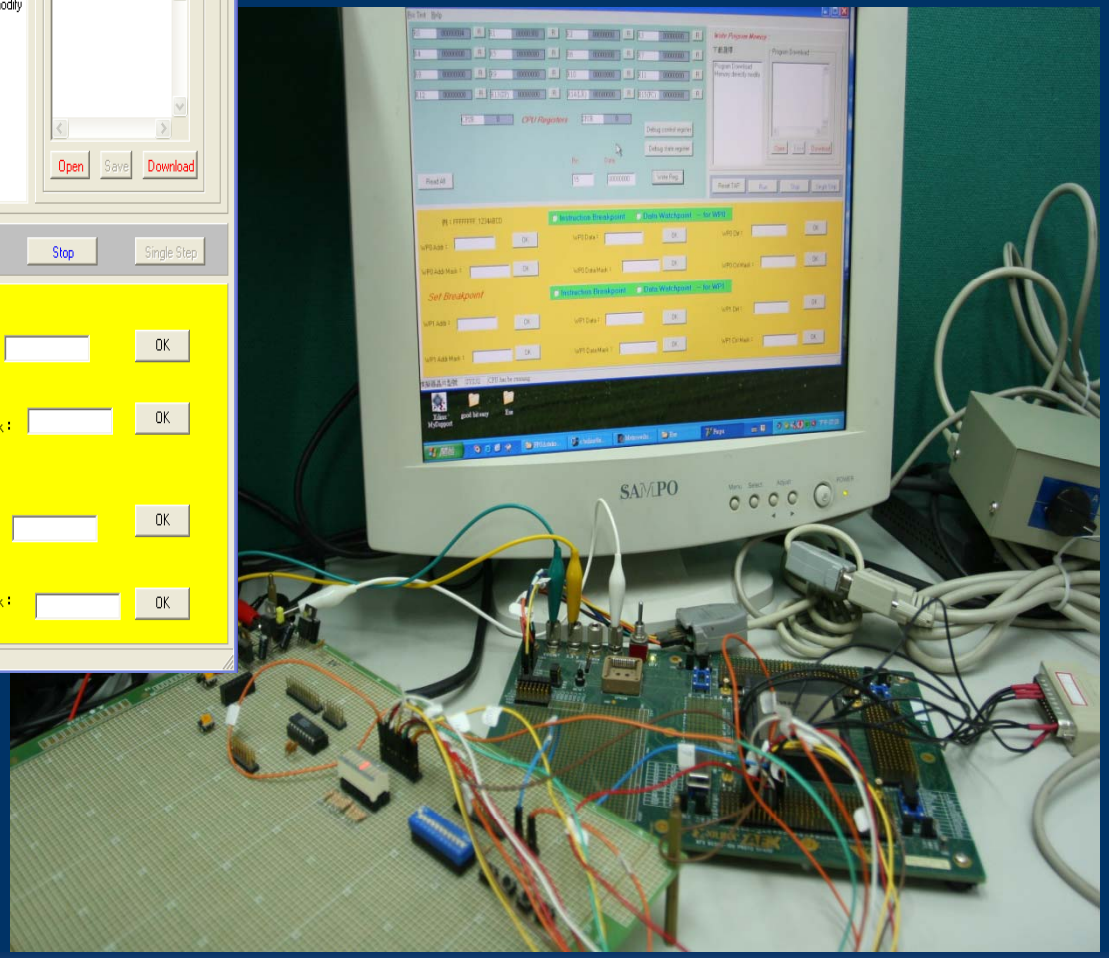
- Interface between microprocessor and ICE
- Insertion of internal scan cells
- Define test data registers
- Breakpoint scan register
- Breakpoint detection unit
- Test data register selection method
- JTAG instructions extension
- Instruction decoder modification

Applications of the Retargetable ICE

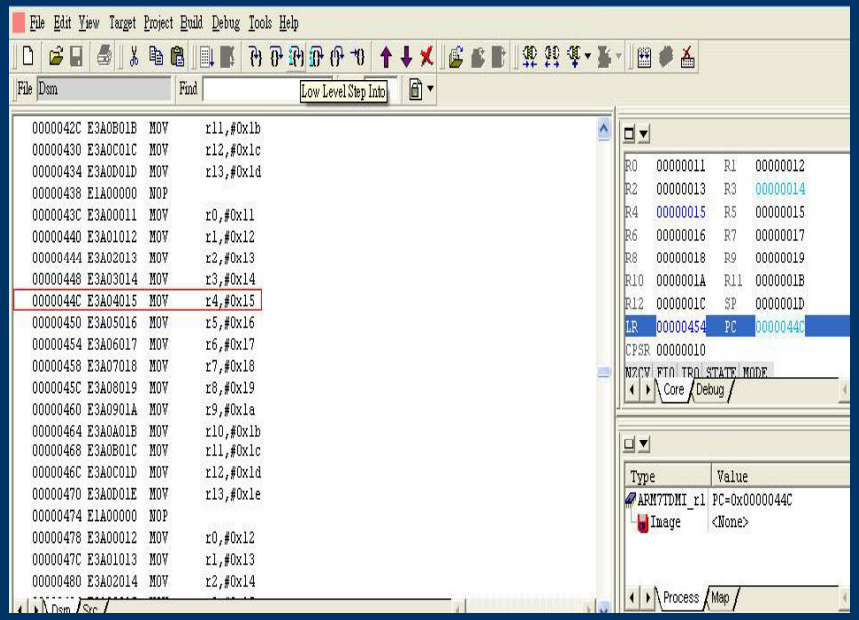
- with 8-bit μC:
  - HT48100 (FPGA, chip) …Holtek
- with 32-bit μP:
  - Academic ARM7-like CPU core (SYS32TM Series) (FPGA, chip) …NSYSU
  - SPARC-like core (RTL) …ACard
  - K310 CPU (in progress) …Himax
- With DSPs:
  - PAC DSP (FPGA, chip) …ITRI-STC,
  - “Q” DSP (in progress) …Himax

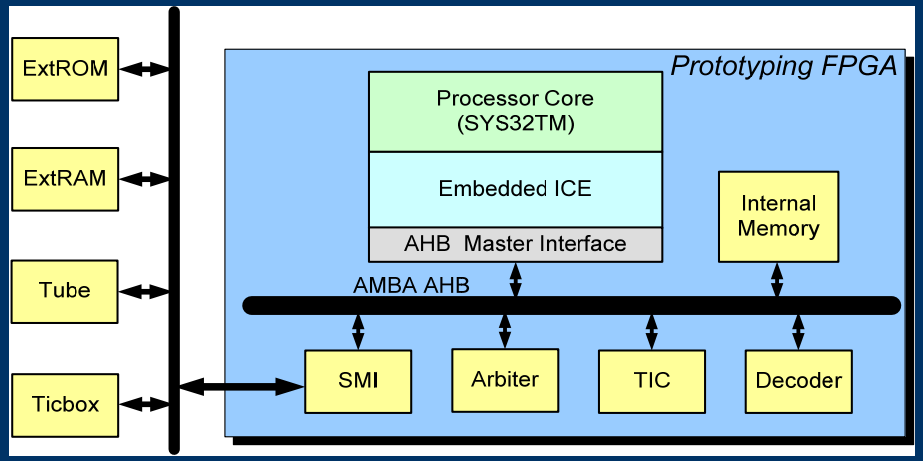
Prototyping for Our Designed Environment

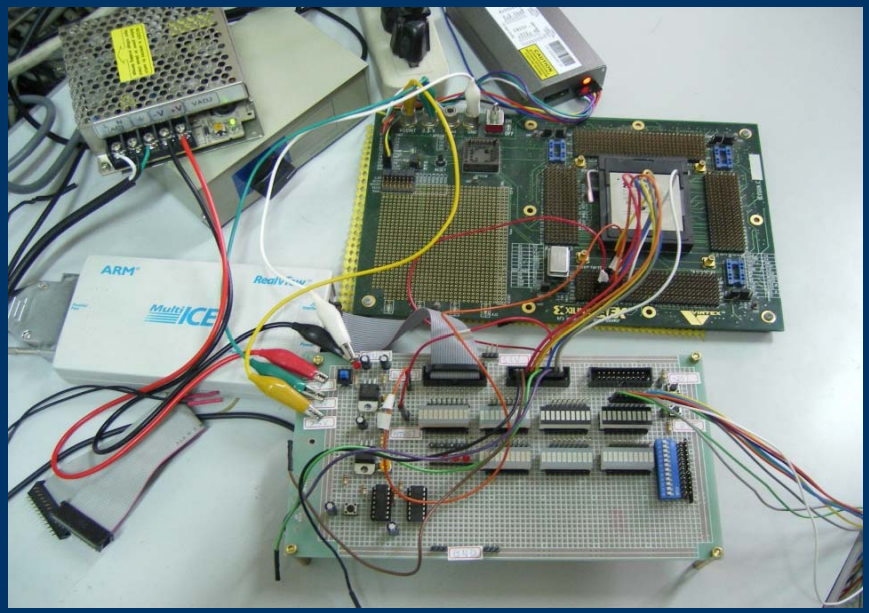




Prototyping for ARM Development Environment







Conclusion

- We propose a parameterized embedded in-circuit emulator and its retargetable debugging software in order to reduce the debugging design procedure time for different target systems.
- The goal is to integrate the EICE component into the microcontroller/microprocessor/DSP processor, and to execute debugging functions via proposed retargetable GUI debugger tool.
- As a result of it, the duration of debugging procedure and time-to-market is reduced.