Statistical Noise Margin Estimation for Sub-Threshold Combinational Circuits

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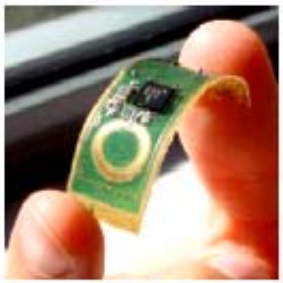
Why Sub-threshold Operations?

- Utilize leakage current drivability
- Quadratic dynamic power saving
- Super-linearly reduced leakage power due to DIBL and GIDL effect
- Optimal energy/operation point exists in the sub-threshold region

Possible Applications

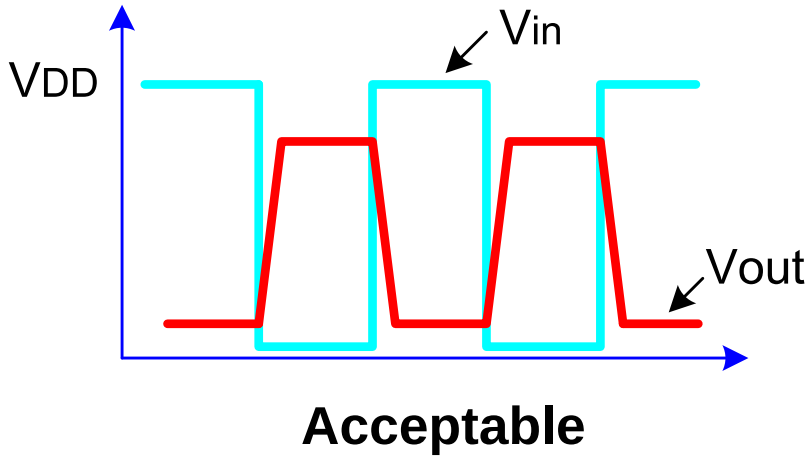


Sensor Network

Biomedical, in-vivo applications, etc.

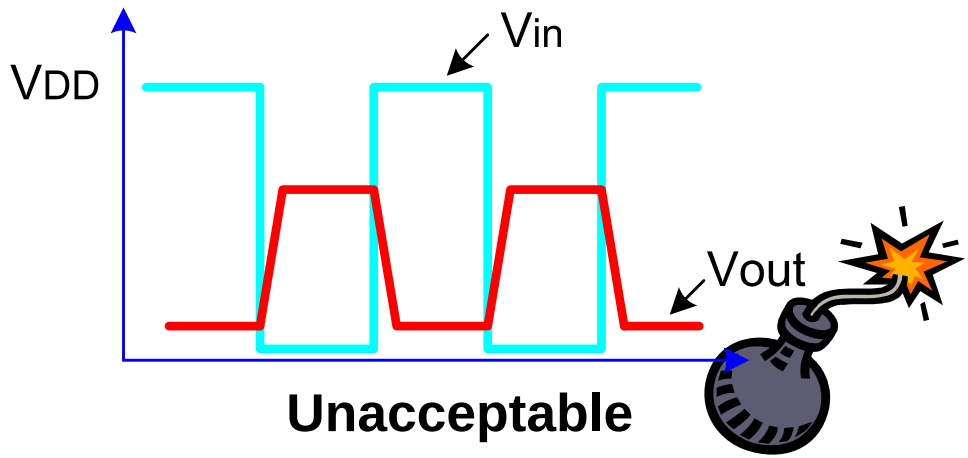
Functional Yield: The Main Limitation

- **The effective-to-idle current ratio (I_{eff}/I_{idle}) of a logic gate working in weak-inversion is 100~1000 times worse compared to in strong-inversion**



Acceptable

- **Manufacturing variability further reduces the available *noise margin*, which may eventually lead to decoding failure (e.g., V_{DD}, V_T variations)**



Unacceptable

Methods for Noise Margin Enhancement

Approach I. ([2]-[5]):

- **ensuring enough noise margins for individual cells**
- **neglects correlations between gates and results in a pessimistic estimation of the outputs noise margin. For instance, a gate that outputs higher V_{OL} (lower V_{OH}) can tolerate higher V_{OL} (lower V_{OH}) from its preceding gate**
- **Ignoring inter-cell correlations results in an overestimation of the minimum power supply V_{DD} and device sizes, thus an increase of power consumption**

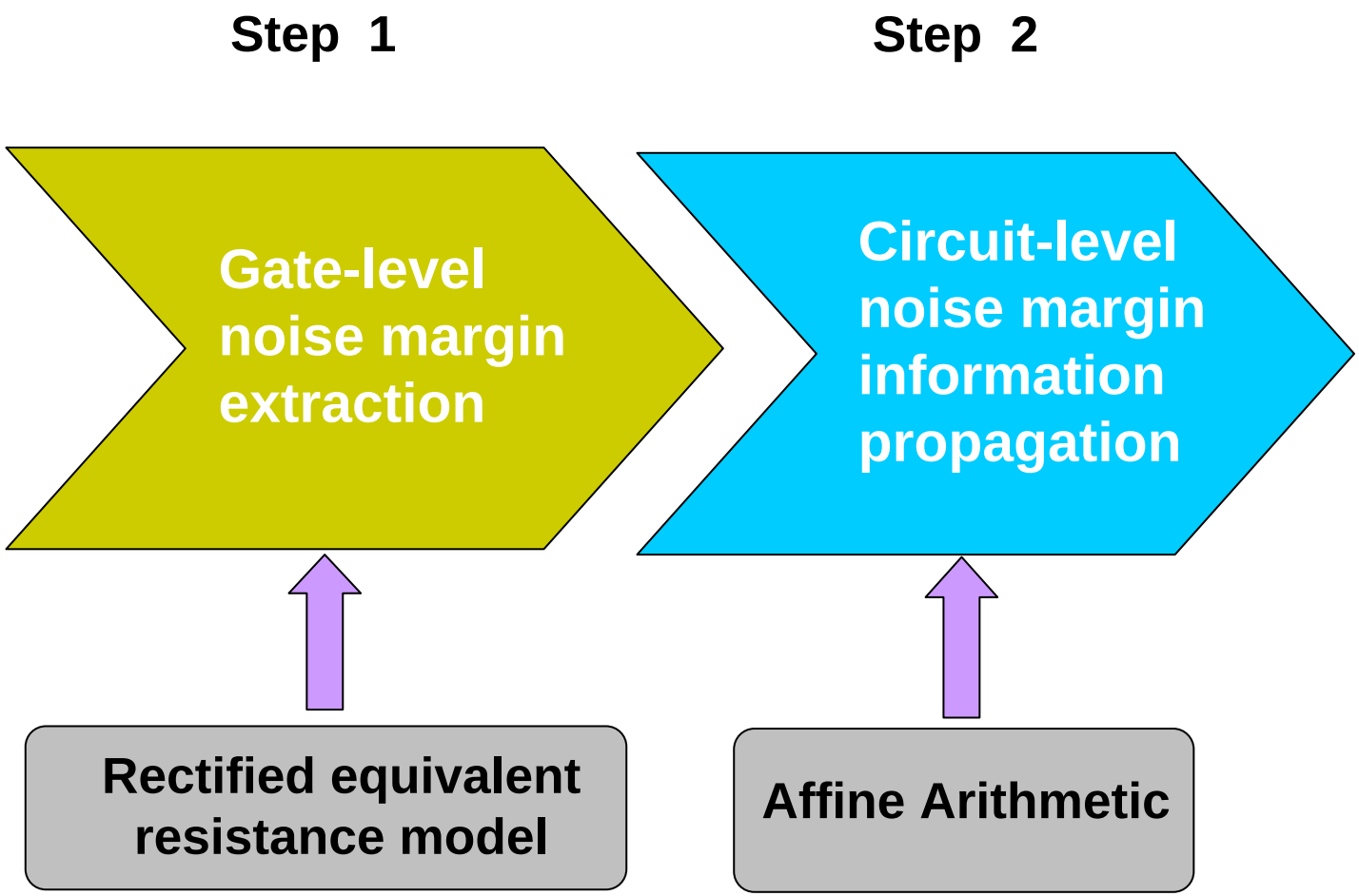
Methods for Noise Margin Enhancement

Approach II.

- **Using Monte-Carlo Analog DC simulations to extract the noise margin**
- **Based on the extracted noise margin information, the designer can improve the robustness of the circuitry by means such as gate resizing, buffer insertion, logic restructuring and etc.**
- **Requires multiple iterations between noise margin extraction and circuit tuning**
- **Prevent additional area and power overhead**
- **But, Very slow...Almost impossible for block with more than thousands of cells!**

Strongly Calling for EDA support to promptly estimate noise margins!

Proposed Noise Margin Extraction Method



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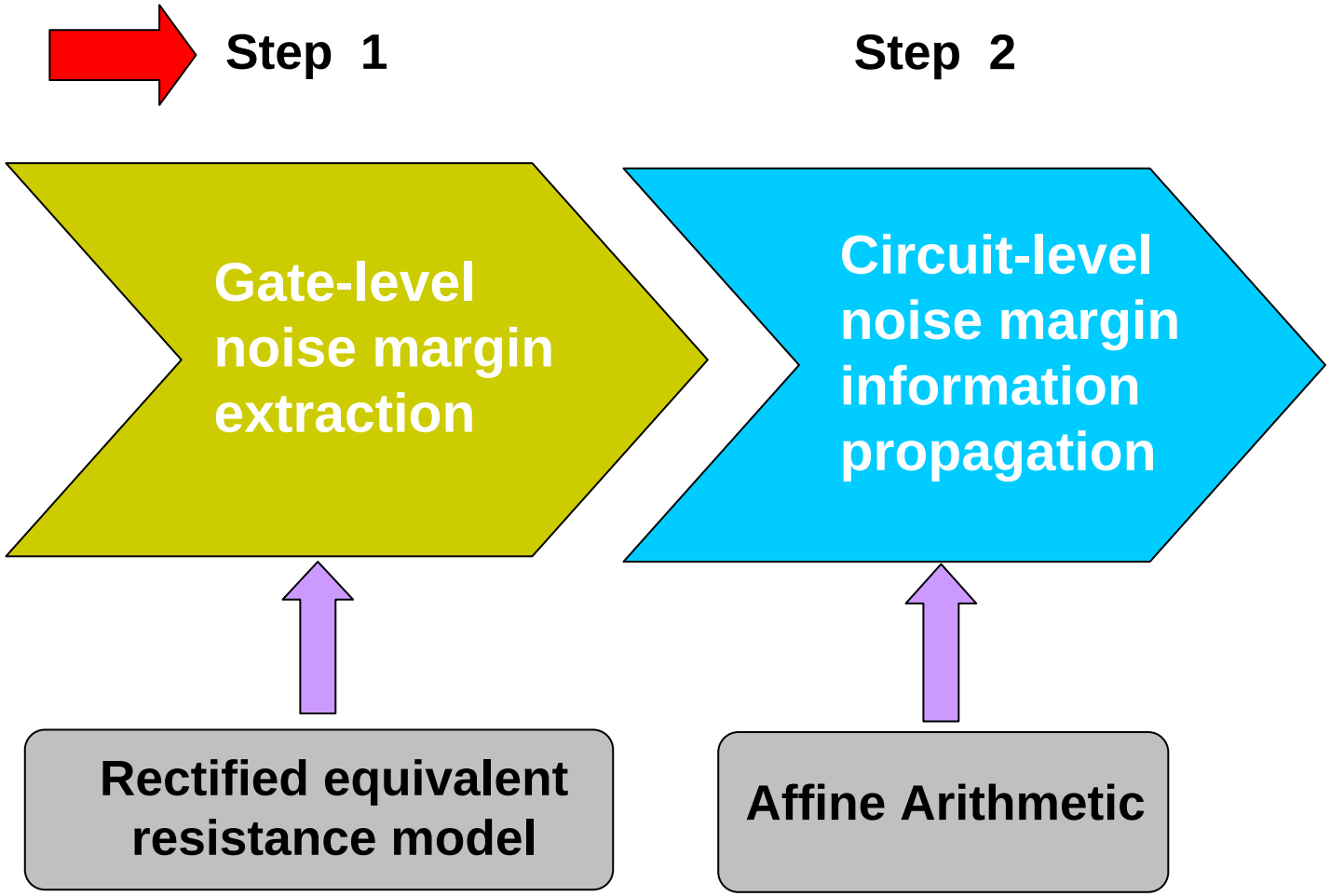
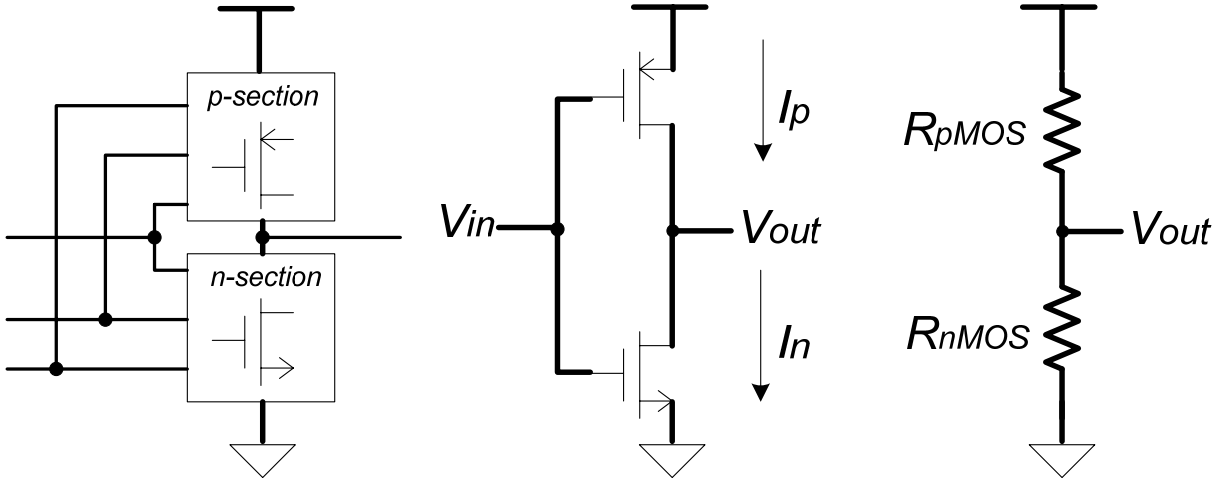


Gate-Level Noise Margin Extraction (1)



$$R_{nMOS} = (I_{0n})^{-1} U e^{-(Vin - VTn)/nU}$$

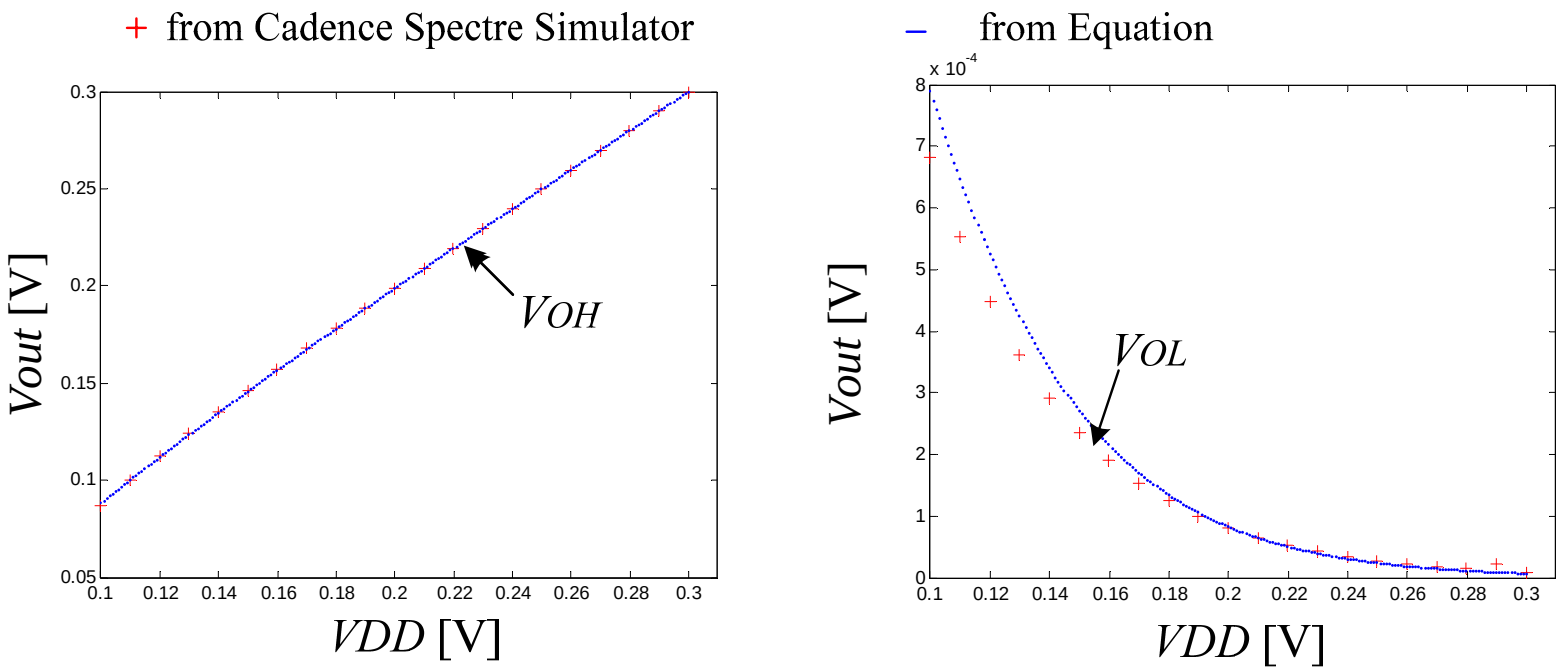
$$R_{pMOS} = (I_{0p})^{-1} U e^{(Vin - V_{DD} - VTp)/nU}$$

$$V_{out} = \left\{ 1 + \left[e^{(Vin - X - V_{DD}/2)/nU} \right]^2 \right\}^{-1} V_{DD} \quad \textbf{where} \quad X = (V_{Tn} + V_{Tp})/2$$

Gate-Level Noise Margin Extraction (2)

Curve fitting by Inserting parameter *λ*, so

$$V_{out} = \left\{1 + \left[e^{\lambda + (Vin - X - V_{DD}/2)/nU} \right]^2 \right\}^{-1} V_{DD}$$



(a)VOH (b) VOL

Noise margin generated from Spectre Simulator vs from Equation

Gate-Level Noise Margin Extraction (3)

For an *N*-input gate, its output voltage can be expressed as a function

$$V_{out} = f(V_{in}, X, V_{DD})$$

For example,

the output voltages of an N-input *NAND* and an N-input *NOR* gate can be expressed as

$$V_{out} = \left\{1 + \left[\sum_{i=1}^{N}\left[e^{\lambda i-(Vin\_i-Xi-V_{DD}/2)/nU}\right]\right]^{-2}\right\}^{-1} V_{DD}$$

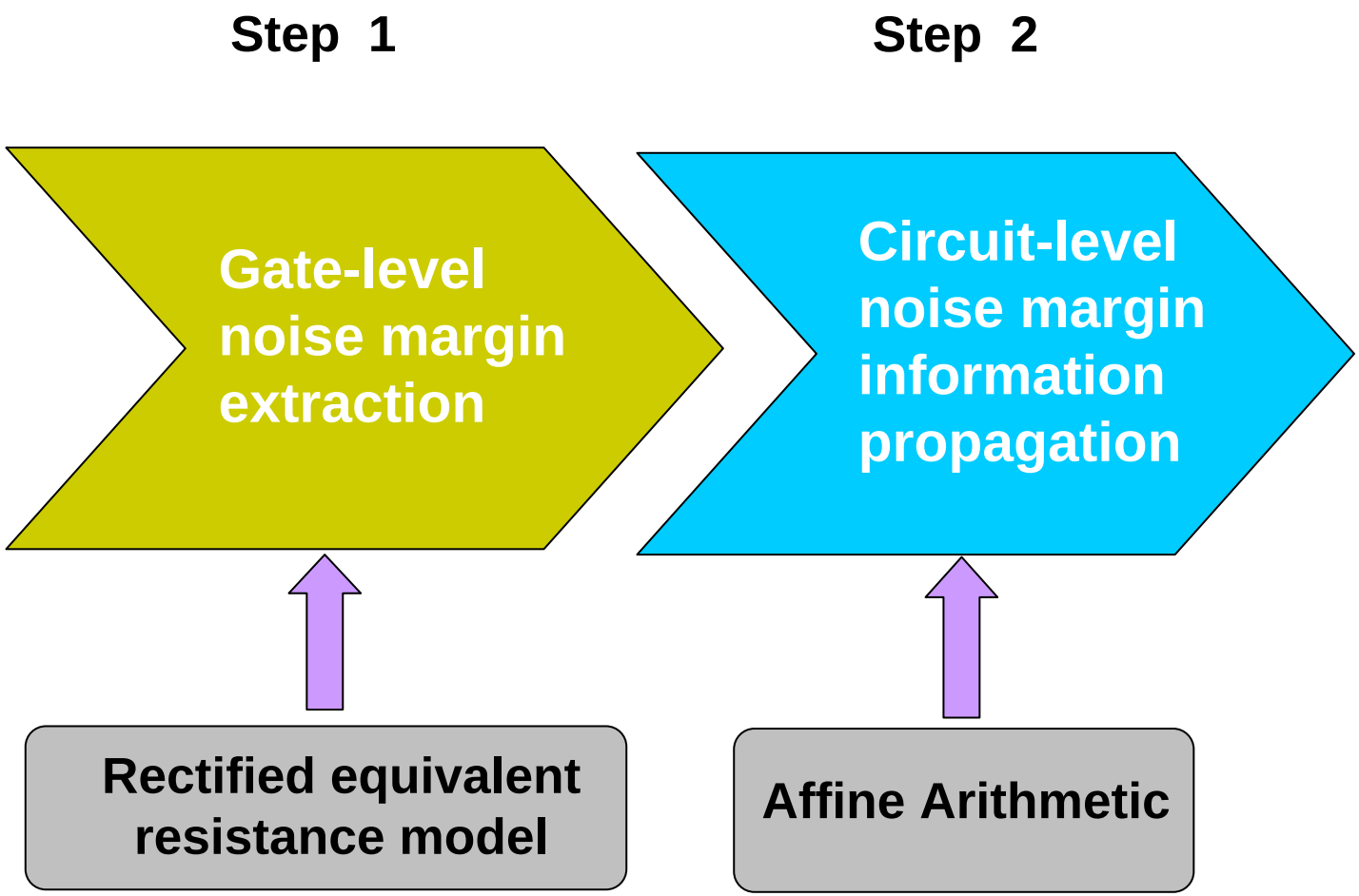
$$V_{out} = \left\{1 + \left[\sum_{i=1}^{N}\left[e^{\lambda i+(Vin\_i-Xi-V_{DD}/2)/nU}\right]\right]^{2}\right\}^{-1} V_{DD}$$

V_{in_i} is the voltage of the i^{th} input ($V_{in\_i} \in \boldsymbol{V_{in}}$)

X_i is the set of inputs ($Xi \in \boldsymbol{X}$ and $X_i \sim N(\mu_{x\_i}, \sigma_{x\_i}^2)$,

λ_i is the i^{th} fitted parameter.

Proposed Noise Margin Extraction Method



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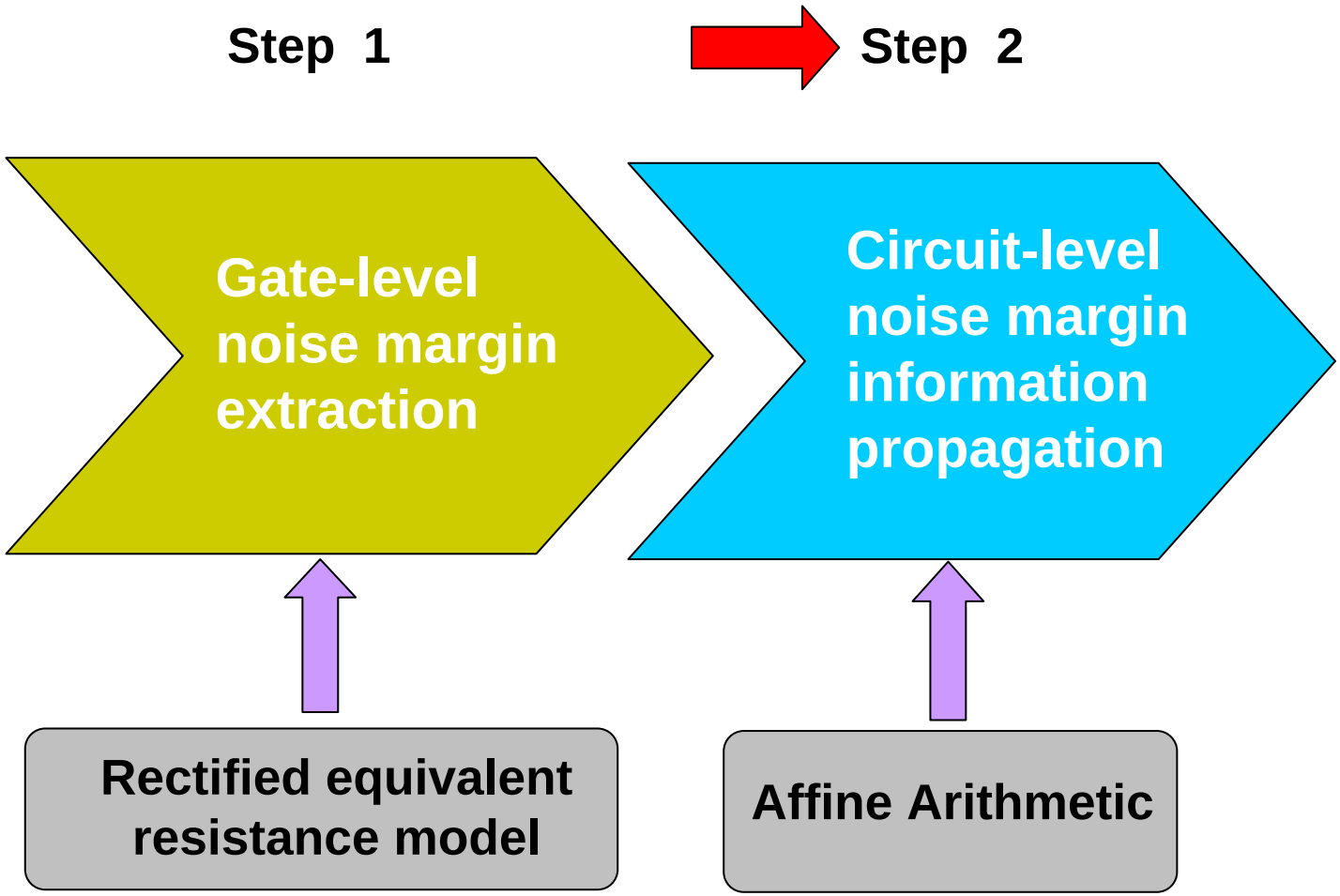


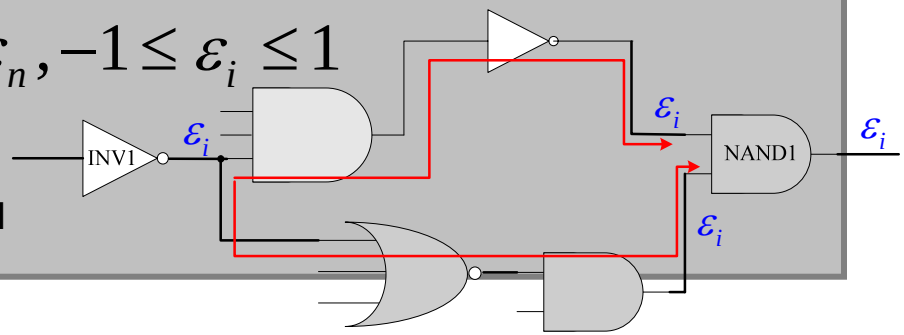
Circuit-level noise margin information propagation (1)

Introduction to AA symbolic propagation

An uncertain variable $\overline{X}$ is expressed as

$$\hat{x} = x_0 + x_1\varepsilon_1 + x_2\varepsilon_2 + \cdots + x_n\varepsilon_n, -1 \le \varepsilon_i \le 1$$

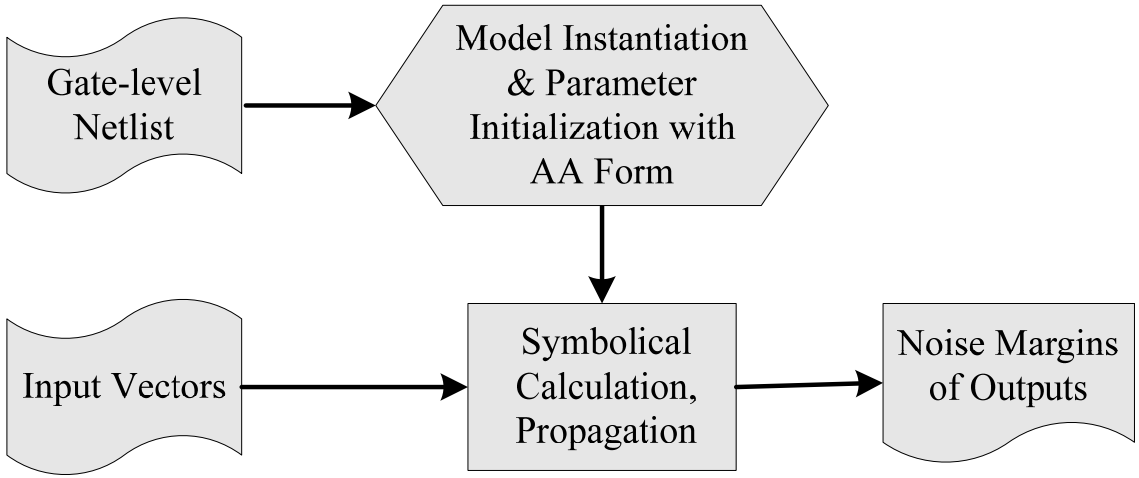
central value coefficient noise symbol



➔***AA*** **is capable of carrying correlation information. Along a propagation data-path, one *noise symbol* ε_i may contribute to the uncertainties of two or more variables.**

➔**AA enables tighter range propagation through cancelling some uncertainties along data-path.**

Circuit-level noise margin information propagation (2)



$$V_{output} = V_{output0} + \sum_{\forall(i,k)} \eta_{i,k}\varepsilon_{i,k}$$

$$V_{out} \sim N(V_{out0}, \sum_{\forall(i,k)} \eta_{i,k}^{\,2})$$

$\varepsilon_{i,k}$ is an independent ***noise symbol*** and $\varepsilon_{i,k} \sim N(0,1)$.
$\eta_{i,k}$ is the corresponding accumulated coefficient.

Experimental Results (1)

Simulation Setup:

- using the ISCAS combinational benchmark circuits
- performed for a CMOS 65nm Standard V_T (SVT) technology from NXP
- circuits are synthesized to netlists with minimum size logic gates
- gates that have more than 4 stacked transistors or 4 paralleled transistors are prevented to avoid severe robustness degradation
- *VOL'* (*VOH'*) here is defined as the maximum (minimum) value among all the outputs 3 σ VOL (VOH), normalized w.r.t. V_{DD}.

Experimental Results (2)

Results from C880:

Bench mark	Sim	150mV		180mV		210mV		Running Time/ Input Vector
		V_{OL}'	V_{OH}'	V_{OL}'	V_{OH}'	V_{OL}'	V_{OH}'	
C880	MC by Cadence	2.4%	84.6%	1.2%	92.2%	0.3%	96.2%	> 10 hours
	New	2.9%	85.4%	1.1%	93.7%	0.4%	97.4%	0.08sec

Estimated 3 σ Statistical Noise Margin from Cadence Spectre Monte-Carlo DC Simulation and the New Approach

Experimental Results (3)

Results from other ISCAS combinational benchmarks

Bench-mark		150mV		180mV		210mV		RunningTime (sec)
		V_{OL}'	V_{OH}'	V_{OL}'	V_{OH}'	V_{OL}'	V_{OH}'	
C1355	3 σ	2.5%	85.0%	1.8%	93.7%	0.3%	97.4%	0.172
	6 σ	4.1%	73.2%	2.6%	88.8%	0.68%	95.4%	
C1908	3 σ	2.4%	78.3%	1.7%	92.6%	0.4%	97.2%	0.204
	6 σ	4.3%	61.1%	2.3%	86.8%	0.7%	95.0%	
C2670	3 σ	3.0%	83.3%	1.2%	91.3%	0.4%	97.4%	0.484
	6 σ	8.0%	70.1%	2.0%	86.7%	0.73%	95.0%	
C3540	3 σ	3.4%	85.1%	1.1%	91.8%	0.4%	97.4%	0.688
	6 σ	6.2%	73.3%	1.95%	88.4%	0.68%	95.4%	
C5315	3 σ	3.5%	77.2%	1.1%	92.6%	0.4%	97.2%	1.203
	6 σ	6.4%	59.4%	1.95%	88.9%	0.73%	95.1%	
C6288	3 σ	7.1%	78.9%	2.4%	92.7%	0.8%	97.2%	1.422
	6 σ	13.0%	62.2%	4.38%	86.9%	1.63%	95.0%	
C7552	3 σ	2.7%	78.4%	1.1%	92.7%	0.4%	97.4%	1.781
	6 σ	4.8%	61.2%	2.1%	86.8%	0.74%	95.1%	

Conclusion

- We have introduced a novel noise margin extraction methodology for sub-threshold combinational circuits
- We model the noise margin of individual cells at the gate-level based on an equivalent resistance model
- We also introduced the *Affine Arithmetic* model to efficiently calculate, propagate and estimate the output statistical noise margin, minimum functional VDD, as well as the functional yield of a circuit
- Experimental results show that our approach has 98.5% accuracy using MC simulations as a reference, but can remarkably reduce the running time by several orders of magnitude.