Design Rule Optimization of Regular layout for Leakage Reduction in Nanoscale Design

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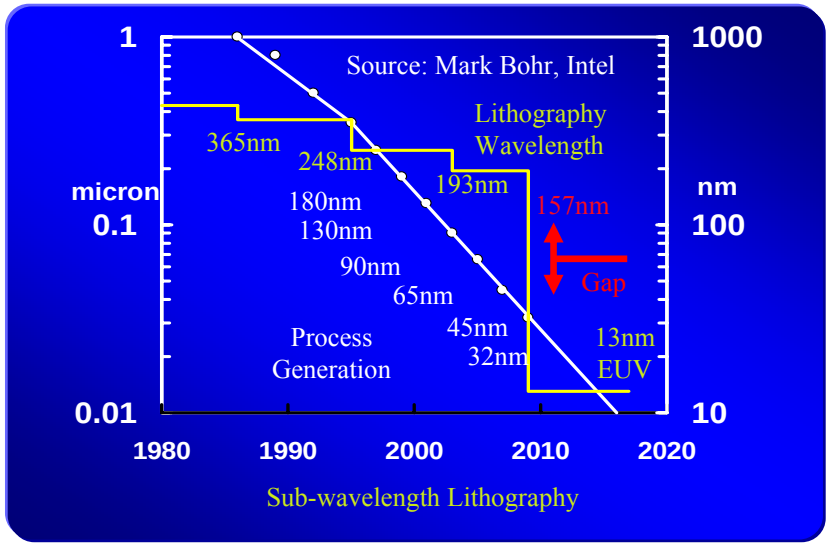
Lithography Trend and Yield Constraints

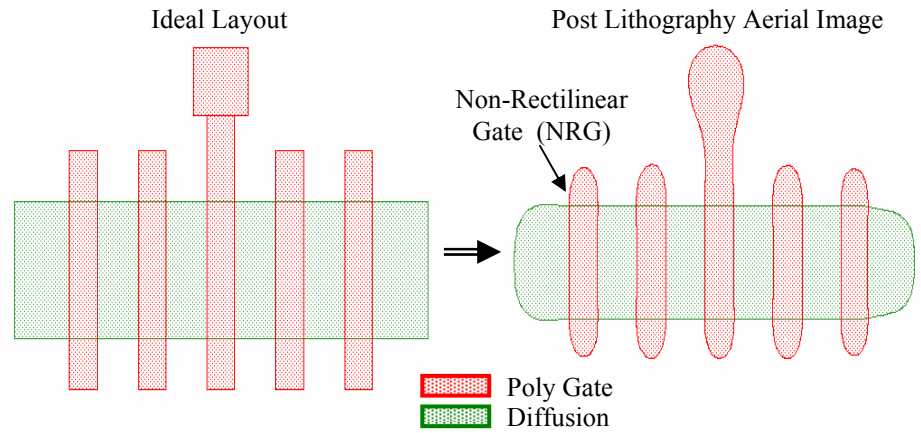
- Yield issues due to device scaling:
  - Yield will be limited by physical dimension instead of traditional particle defects.
  - Device will be distorted due to Lithography limitations, Mask misalignment, Etching, Oxide growth, System defects and Random effects.

- Lithography limits:
  - When Critical Dimension (CD) is getting smaller than optical wave length.
  - Functional yield (defects) :
    - Shorts for dense feature
    - Opens for isolated features.
  - Parametric yield (process variation):
    - Edge placement error for CD.
    - Power and Performance impact.

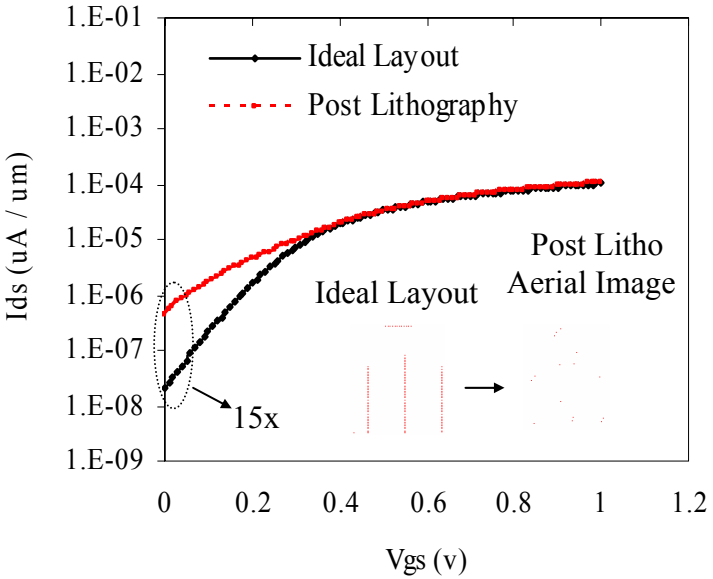


Post Lithography Gate Shape

- Post Litho Non Rectilinear Gate (NRG) Impact:
  - Shortening of poly line end can cause device failure.
  - Sub-threshold leakage may increase by more than ~15x compared to ideal layout.
  - Overall yield impact.



DAC 2007

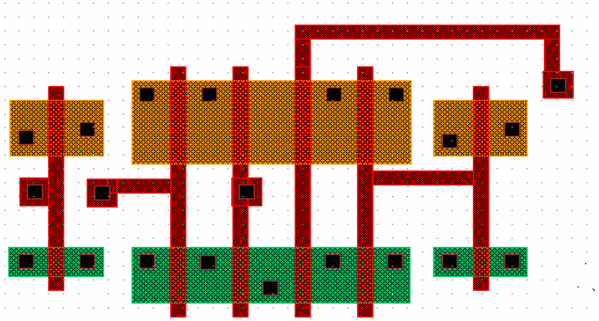


Leakage current fluctuation with ideal layout versus post litho NRG Model.

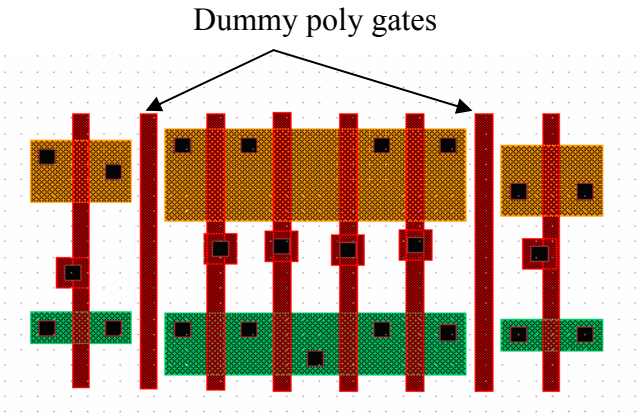
Regular Layout

- Follows the concept of single pitch and single orientation.
- Restrictive Design Rule (RDR) was proposed to effectively enhance yield and minimize the process variation.
- Minimize variation in gate length due to distortion caused by lithography.

- Why do we need Regular Layout Optimization and RDR Prediction:
  - As the interaction between Layout and Leakage becomes more pronounced, there is a growing demand to predict and optimize the Regular Layout under RDR for low power designs.



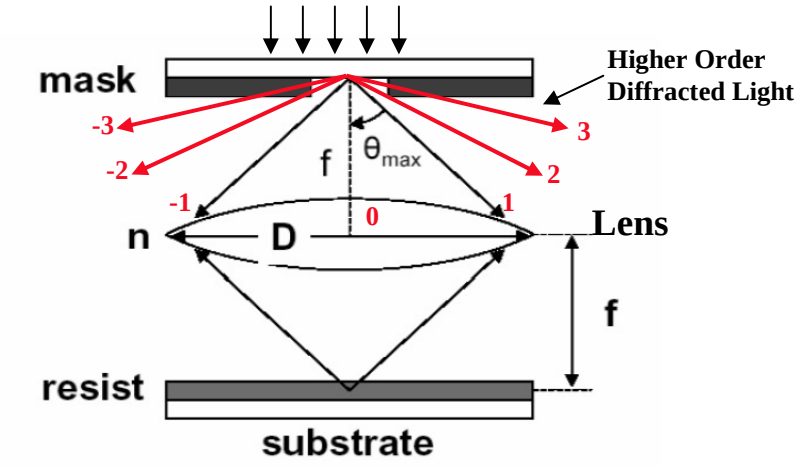
Random layout showing gate, diffusion and contacts location.



Regular layout showing gate, diffusion and contacts. location.

Lithography Basics:

- Projection Lithography Basics:



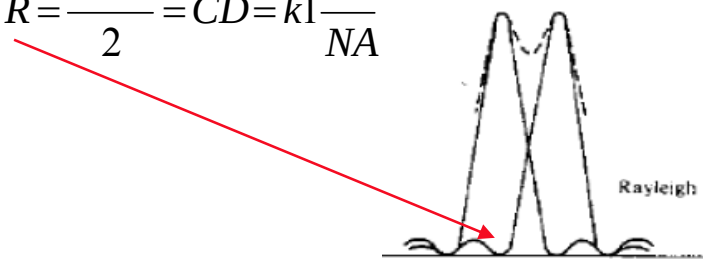
$$NA = n \cdot \sin(\theta_{max})$$

$$\frac{NA}{n} = \frac{\frac{D}{2}}{\sqrt{\left(\frac{D}{2}\right)^2 + f^2}}$$

n – Refractive Index
f – Focal Distance
D – Lens Diameter
NA – Numerical Aperture
θ_{max} **– Max Focus angle**
λ **– Optical Wave Length**

- Resolution: Diffraction Limited.
  - In a smaller feature size,
    - → Larger Diffraction.
    - → Fewer diffraction order can be captured
    - → Loss of image details.

$$R = \frac{Pitch}{2} = CD = k1\frac{\lambda}{NA}$$



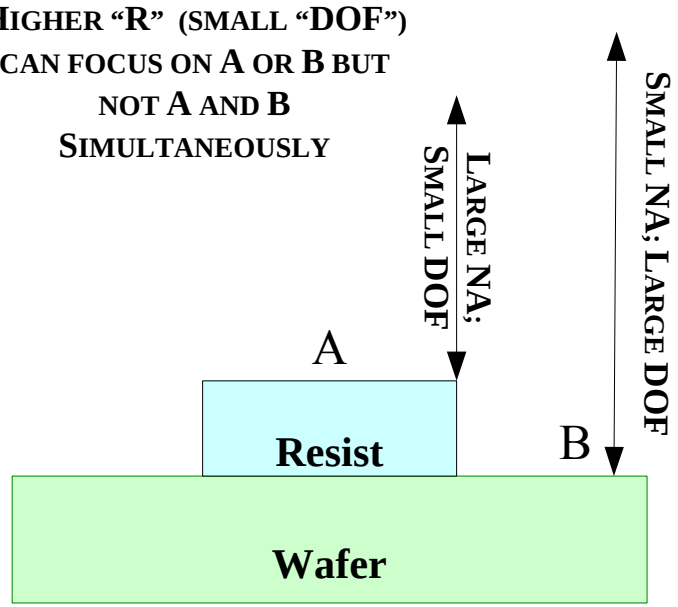
- k1 : Process dependent adjustment factor
  - Practical lower limit k1 ~= 0.25
  - K1 can be determined by resist capability, tool control, reticle pattern adjustment and other process control.

Defocus

- Defocus Tolerance: Depth Of Focus (DOF):
  - Range of Focus for which the resist profile remains within specs.

$$DOF \approx \pm k2 \frac{\lambda}{NA^2} \approx \pm k2 \frac{CD^2}{k1^2 \lambda}$$

  - DOF can't be too low because the low image definition and contrast can alter CD and limit exposure latitude.
  - Variation in surface height of processed wafer must be less than the optical DOF.
  - There is a negative effect between DOF and Resolution. That means the better the resolution, the worse the DOF.



Resolution Enhancement Techniques (RET)

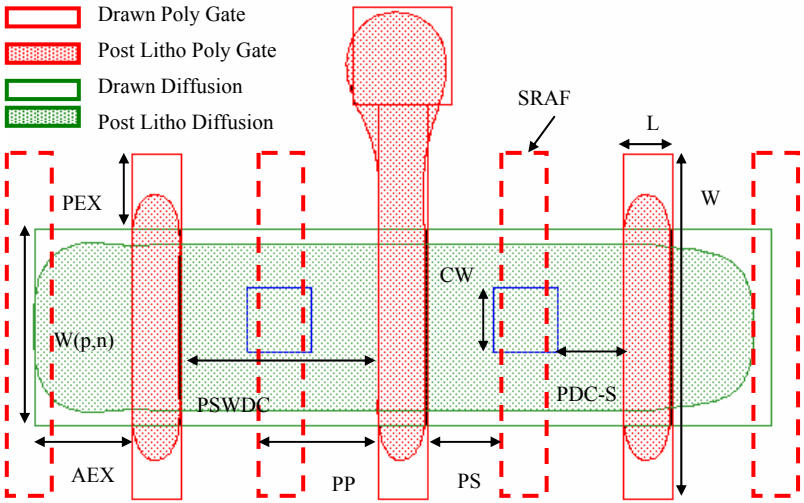
- Litho process window is defined by adjusting R and DOF along with other process specific parameters.
- RET: Resolution Enhancement Techniques.
  - Amplitude, Direction, Phase and Wavelength of optical system can be controlled to improve Resolution.
  - RET Benefits:
    - Better Resolution.
  - RET Limits:
    - High Mask Cost.
    - Huge Turnaround Time for yield verification due to large data volume.
    - Requires the Layout to follow the concept of Single pitch and single orientation.
    - Impact on Layout Rule / Design Restriction.

RET approaches:

- Optical Proximity Correction (OPC).
- Phase Shift Mask (PSM) – attenuated PSM / alternating PSM.
- Off Axis Illumination (OAI).
  - Allows some of the higher order diffracted light to be captured and hence can improve resolution (by decreasing k_1).
  - Amplifies certain pitch at the cost of others.
- Sub Resolution Assist Feature (SRAF).
  - Dummy poly feature are placed in between two poly gates where the poly pitch is greater than the optimal pitch for OAI .

Regular Layout Optimization under RDR

- Critical Design Rules impact to CD:
  - 1st order effect to PS and PDC-S.
  - 2nd order effect to PEX, W, CW, AEX etc..



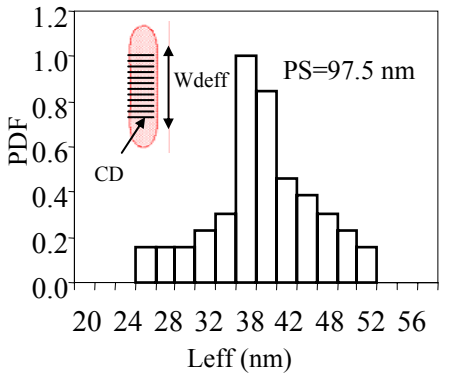
Post litho aerial image super imposed on top of ideal layout illustrating critical design rule index used for optimization.

Critical design rule index

Design Rule (nm)	Rule Index
Poly Pitch	PP
Poly Gate Length	L=(LW)
Poly Gate Width	W
Poly Space	PS=(LS)
Contact Width	CW
Poly End Cap	PEX
Poly to Diffusion Contact Space	PDC-S
Active Extension	AEX
Active Width Nmos	$W_d=W_n$
Active Width Pmos	$W_d=W_p$

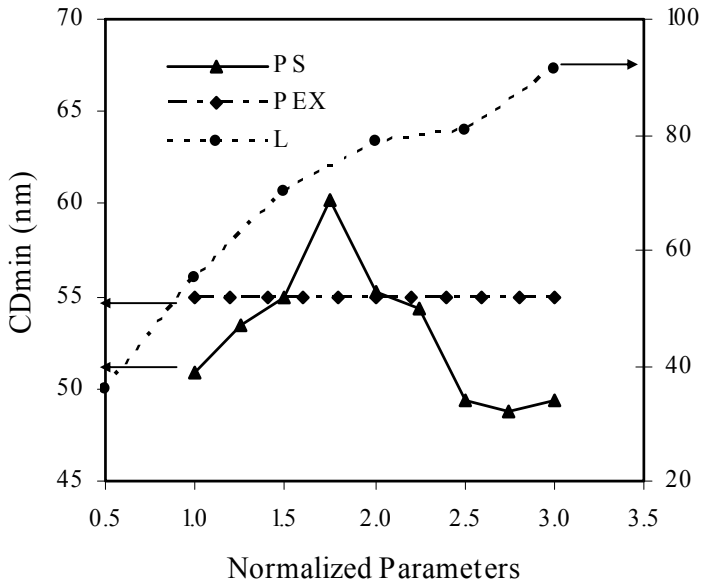
Validation suite for Regular Layout Optimization

- Calibre - Post Lithography Aerial Image Simulation for NRG:
  - λ=157nm; NA=0.95; n=1.437;
  - OAI along with SRAF are added into consideration.
  - Post lithography aerial image simulation model combined with NRG leakage model is suitable for leakage analysis for Regular layout optimization using RDR.
- Benchmark Circuits:
  - NAND gate, XOR gate and 1bit full adder.
- Regulate Layout:
  - We follow the concept of single pitch and single orientation to alleviate the leakage induced by NRG effect.



Normalized PDF of post litho, post etch effective channel length (Etch effect ~=30nm). *Leff = CD – etch effect*

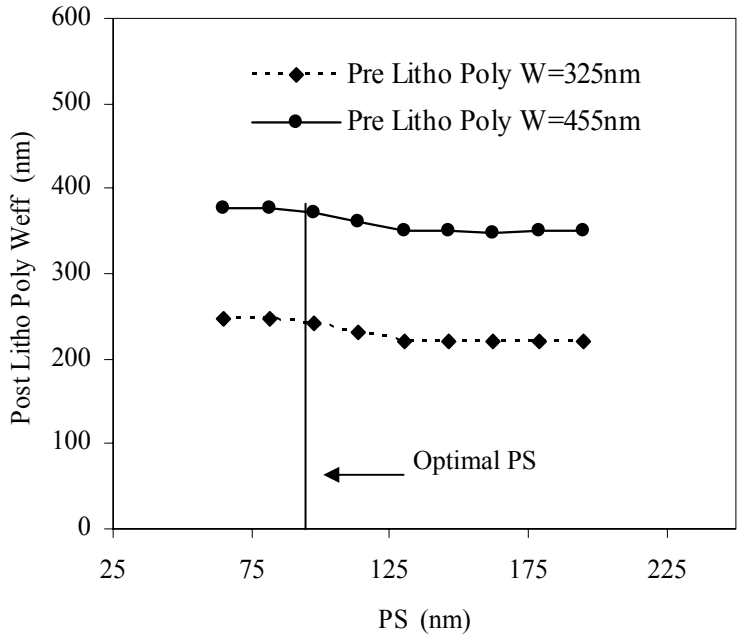
Priority of Optimization for Layout Parameters



CDmin sensitivity to poly space (PS), poly end extension (PEX) and gate length (L).

- Poly space (PS) has 1st order impact on CD and in turn leakage energy.
  - Optimized for leakage
- Poly end extension (PEX) has 2nd order impact on CD.
  - Critical for circuit operation.
  - Optimized for manufacturability.
  - *PEX ~= 1.5L (considering process variation)*
- L process window is in the range of 60nm to 75nm depending on design requirement.
- Cdmin is affected profoundly by PS.

Post Litho Effective Poly Width

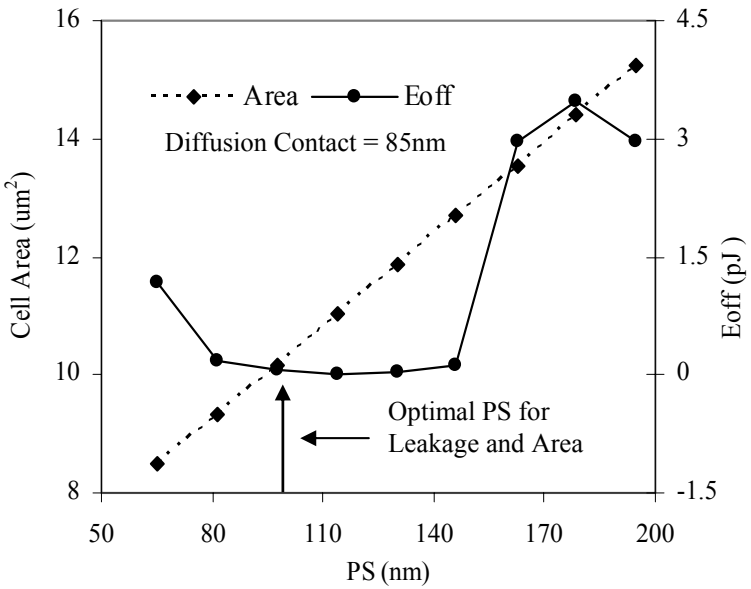


Post litho effective poly width (Weff) with respect to PS optimization.

- W_{eff} has marginal impact with respect to PS.
- Poly width (W) can be optimized for better manufacturability.
  - *W= Wd + 2PEX.*

    where Wd - diffusion width.

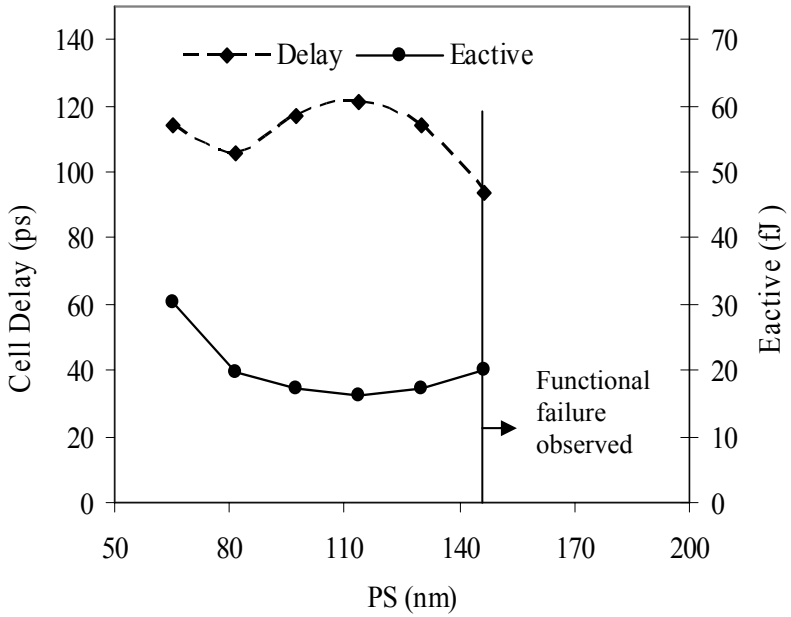
Finding optimal Poly Space for Regular Layout



Finding optimal poly space (PS) considering leakage energy (Eoff) and area trade off.

- Leakage energy (Eoff) is sensitive to CD min obtained from aerial image simulation, and PS has a strong connection with CD.
- Thus, once we have the optimal PS, Eoff impact and area penalty can also be optimized.
- Compared to un-optimized regular layout for benchmark circuits, 73% reduction Eoff with 10% area penalty can be achieved in our optimal simulation.

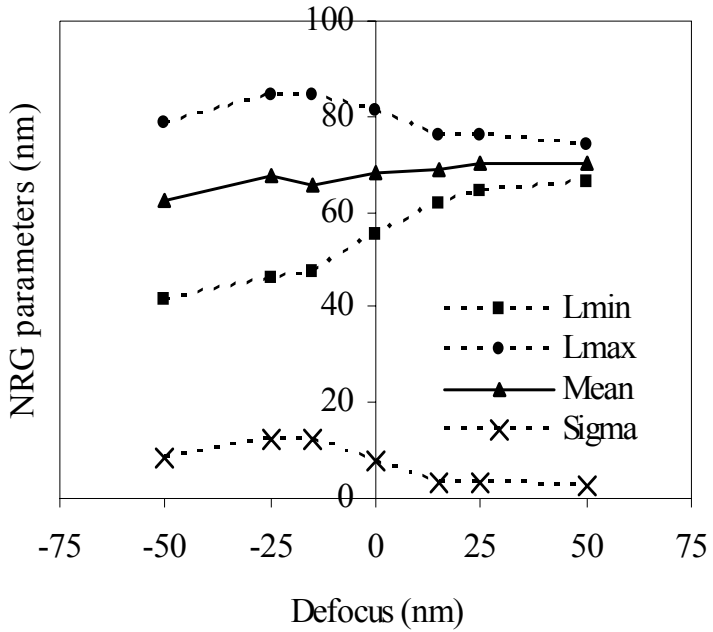
Active Energy and Delay Impact due to RDR



Impact of active energy (Eactive) and speed (Tpd) due to PS optimization.

- There is a marginal impact on the cell delay and active power.
- Circuit speed (Tpd) has ~12.5% slow down compared to un-optimized regular design.
- On the other hand, active energy (Eactive) can be improved by ~12% .

Effect of Defocus

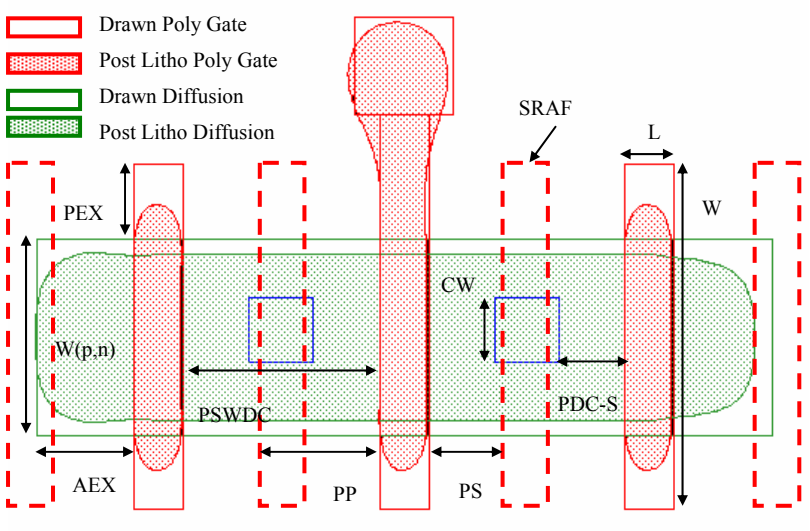


The impact of defocus on post litho NRG parameters for optimized layout.

- Variation in Lmin due to defocus : +6.8nm to -7.7nm
- Positive defocus range : reduce leakage and slow down the circuit speed due to Lmin increase
- Negative defocus range : increase the leakage as well as speed and could cause fatal failure due heavy leakage caused by reduction in Lmin

Optimized RDR parameters for Regular Layout

Optimized RDR Parameter	Optimized Value (nm)
PP	162.5
PS	97.5
PDC-S	87.5
CW	85
PEX	97.5
W	455
L	65
AEX	172.5



- *PP = L + PS = LW + LS*
- *PDC-S = [(2 PS) + L – CW]/ 2*
- *PSWDC = CW + (2PDC-S)*
- *AEX = CW + PDC-S + X*
  - X – Active overlap of contact. X can be eliminated considering 1st order approximation.

Comparative Analysis of Benchmark Layouts

Layout Design Style	T_{pd} (ps)	E_{active} (fJ)	Area (um2)	E_{off} (fJ)
NAND				
Typical Regular	33.58	1.316	1.187	0.0228
Optimized Regular	37.66	1.536	1.231	0.0146
Optimized vs Typical Regular (%)	12.15	16.72	3.71	-36.12
XOR				
Typical Regular	90.82	7.53	4.260	52.63
Optimized Regular	97.56	7.21	4.612	13.97
Optimized vs Typical Regular (%)	7.42	-4.20	8.26	-73.46
One bit full Adder				
Typical Regular	104.00	19.56	9.341	184.5
Optimized Regular	117.00	17.25	10.173	50.15
Optimized vs Typical Regular (%)	12.50	-11.81	8.91	-72.82

Conclusion

- With optimized regular layout, E_{off} (off-state power consumption) due to NRG is reduced by ~73% for PS=97.5nm with area penalty of ~9% on the benchmark standard cells.
- Marginal impact on Eactive and Tpd of ~5% to 12.5% for 1bit full adder in 65nm process technology.
- Proposed RDR prediction method and regular layout optimization technique can be efficiently applied during design phase of product cycle to help reduce energy consumption and improve product yield.

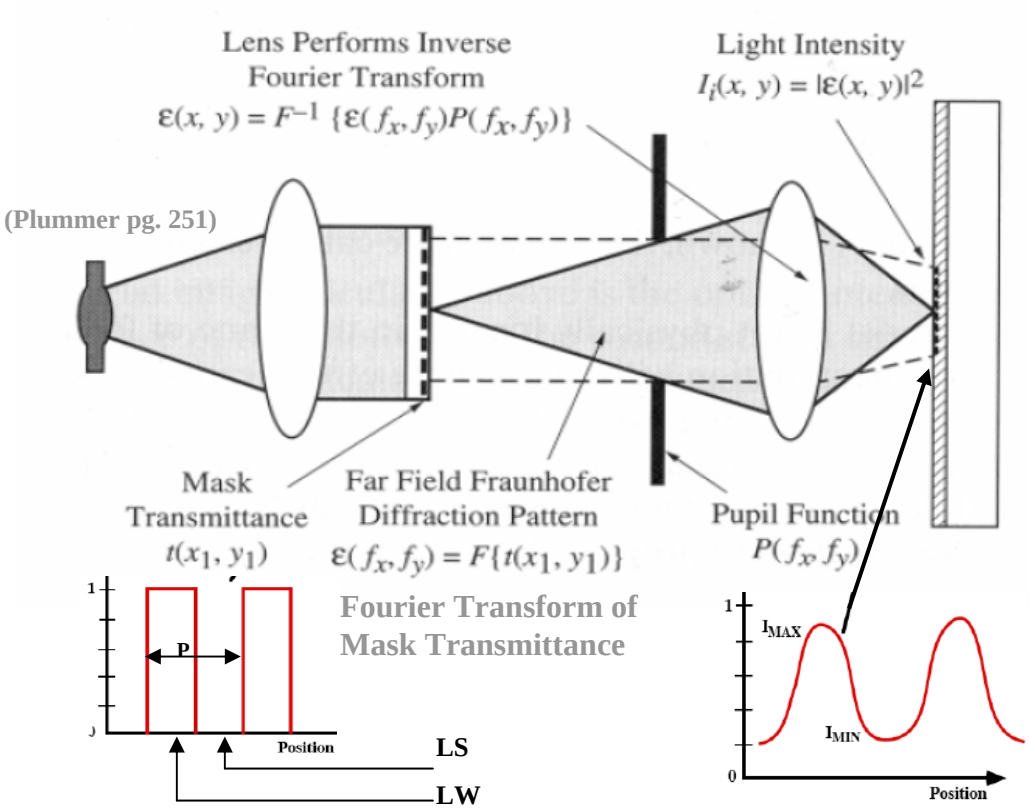
Thank You !

Questions?
Comments
Concerns

Backups

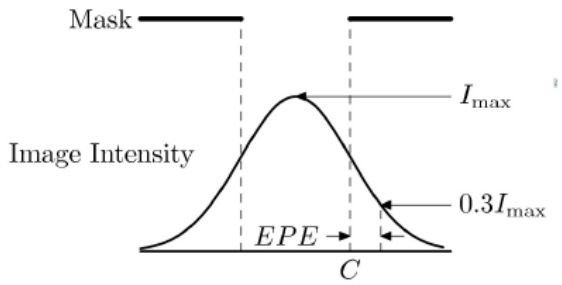
CD Variation Estimation

- 2-D Aerial Image Simulation Method Using Projection Litho Model.



- Modulation Transfer Function (MTF)

$$MTF = \frac{M_{image}}{M_{mask}} \qquad MTF = \left(\frac{I_{max} - I_{min}}{I_{max} + I_{min}}\right)$$



(DAC2005: RET aware Fast Litho simulation)

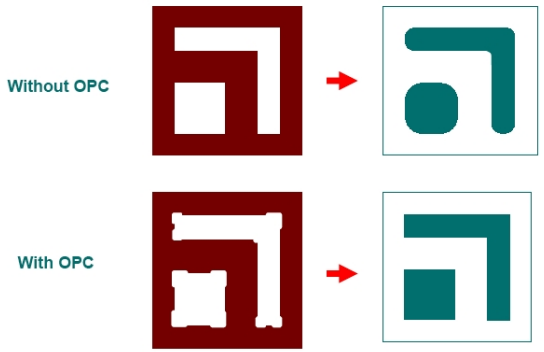
Problem Description

- Yield: Percentage of Manufactured chip that meet product specification
  (ie. power, performance and area specs)
- Litho illumination Impact:
  - Edge Placement Error for Critical Dimension (CD):
    EPE (ΔCD) = drawn layout mask CD – printed CD in wafer
    → Results in parametric yield (process variation).
    - -ve EPE (poly gate) → Leakage impact.
    - +ve EPE (poly gate) → Performance impact.

Source: IBM and Intel

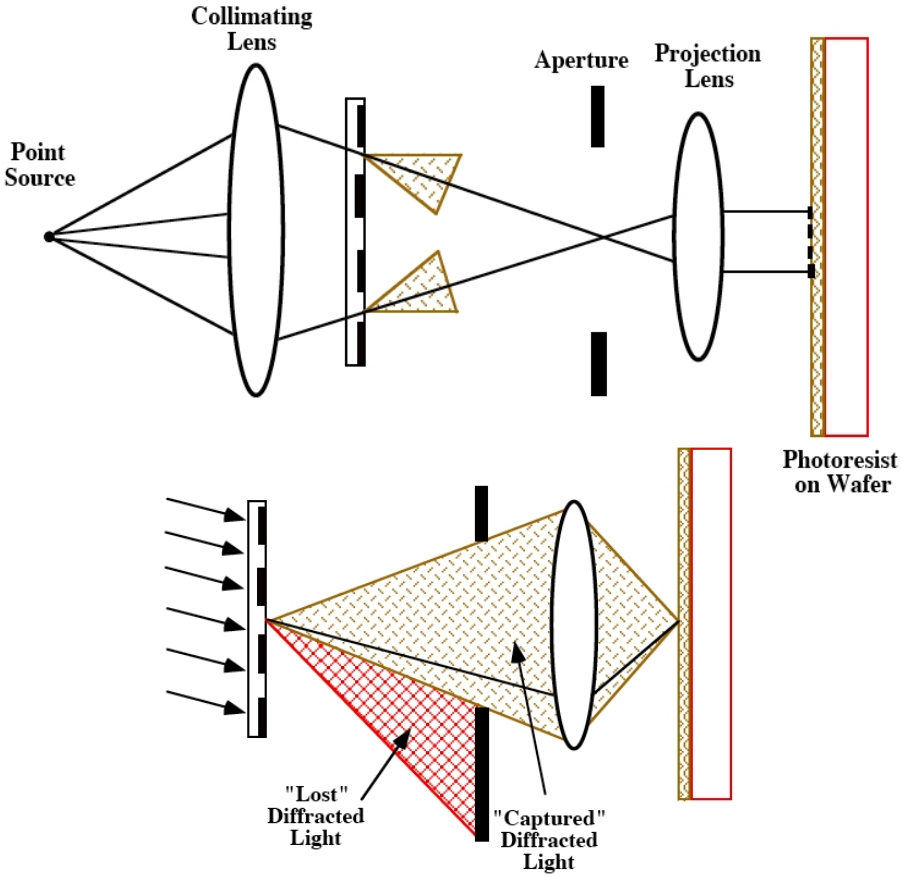
Photolithography- OPC

- Optical Proximity Correction (OPC) can be used to compensate somewhat for diffraction effects.
- Sharp features are lost because higher spatial frequencies are lost due to diffraction. These effects can be calculated and can be compensated for. This improves the resolution by decreasing k_1.



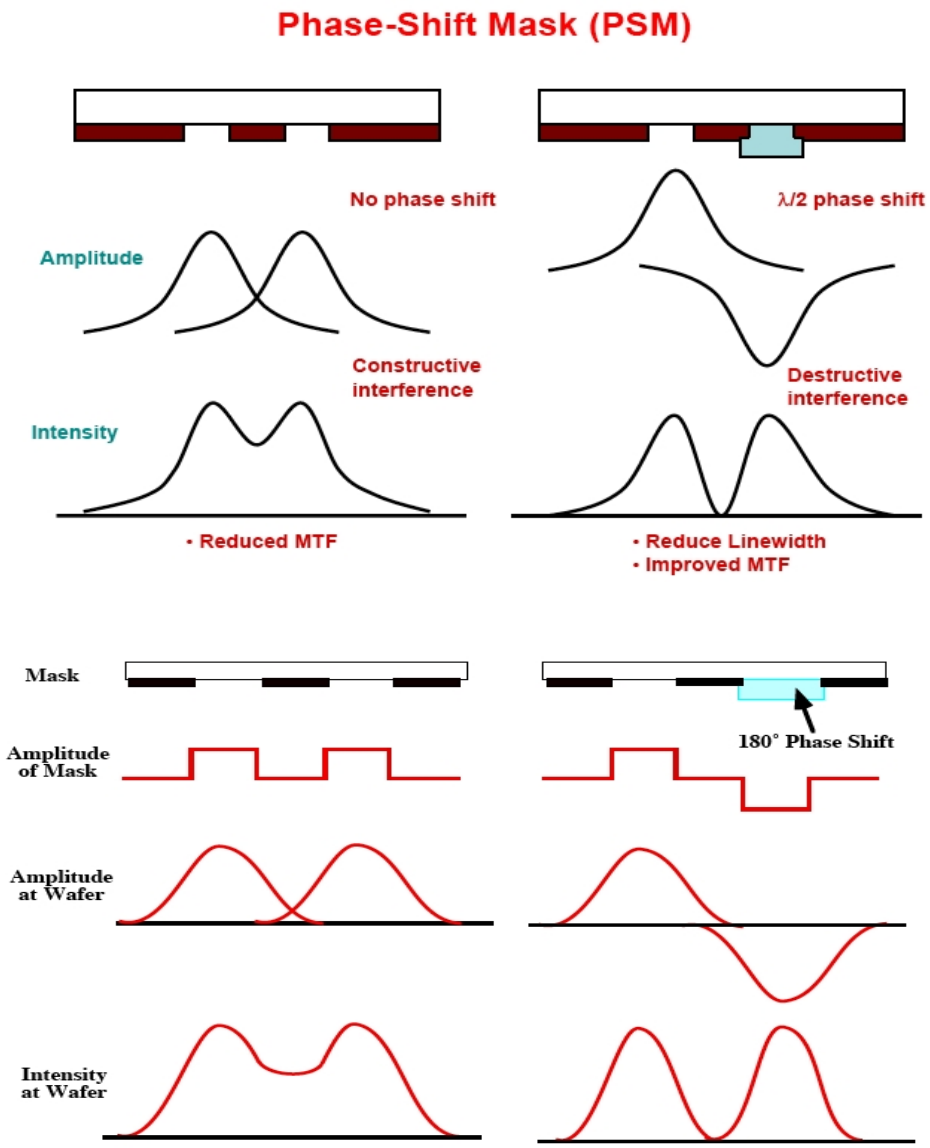
Photolithography-OAI

- OAI systems focus the light at the entrance pupil of the objective lens. This “captures” diffracted light equally well from all positions on the mask.
- This method improves the resolution by bringing k_1 down.
- “Off-axis illumination” also allows some of the higher order diffracted light to be captured and hence can improve resolution (by decreasing k1).



Photolithography- Phase Shift Masks

- Extends resolution capability of current optical lithography
- Takes advantage of the wave nature of light
- PSM changes the phase of light by 180° in adjacent patterns leading to destructive interference rather than constructive interference
- Improves MTF of aerial image on wafer. Making k_1 smaller.
- allow sharper resist images and/or smaller feature sizes for a given exposure system.



Aerial Image Simulation Model

- Post Lithography Aerial Image Simulation:
  - Calibre workbench used for post litho aerial image simulation.
    - Model based OPC.
    - TCCALC engine with scalar diffraction model.
  - Technology node – 65nm;
  - Illumination wavelength λ=157nm;
  - Numerical aperture NA=0.95 (maximum theoretical limit);
  - Refractive index n=1.437;
  - Due to regular layout style, OAI combined with SRAF is added benefit.
  - Resist thickness ~=125nm assumed (ITRS requirement < 225nm.
  - CD calculated at 30% of maximum image intensity

NRG Leakage Simulation Model

- Leakage Simulation using NRG model:
  - PTM 65nm technology model with Leff in place of gate length in spice simulation.
    - Verilog-A model for transistors used in integrating NRG Leff model with spice simulator.
  - NRG leakage mode requires the PDF of Leff obtained from post litho simulation to have Gaussian distribution.

$L_e^{\min} = L_{\min} + \ln(\sigma W / Wc)$ Wc = ~5nm from post litho aerial image simulation

$L_e^{\min}$ Fuction of Lmin and sigma of all lengths that form the gate section. Leakage has exponential dependence on this parameter

$L_e^{\max} = \mu - \ln(\sigma)$

$L_e^{\max}$ Fuction of mean gate length and sigma

$$L_{eff} = L_e^{\min} + \frac{\Delta L \sqrt{\alpha} Vgs}{\sqrt{\alpha (Vgs)^2 + 1}}$$

$\Delta L = L_e^{\max} - L_e^{\min}$ Fitting parameter

- Post lithography aerial image simulation model combined with NRG leakage model is suitable for Regular layout optimization using RDR for leakage.

Preliminary Results (contd…)

Critical design rule index and parameter range used for layout optimization.

Design Rule (nm)	Rule Index	Minimum value	Maximum value
Poly Pitch	PP	130	200
Poly Gate Length	L=(LW)	60	85
Poly Gate Width	W	325	650
Poly Space	PS=(LS)	65	195
Contact Width	CW	65	85
Poly End Cap	PEX	33	180
Poly to Diffusion Contact Space	PDC-S	60	130
Active Extension	AEX	65	260
Active Width Nmos	W_d=W_n	130	195
Active Width Pmos	W_d=W_p	195	260

Final optimized parameters for regular layout vs typical regular layout.

Optimized Layout Parameter	**Typical value (nm)**	**Optimized Value (nm)**
PP	146	162.5
PS	81	97.5
PDC-S	71	87.5
CW	80	85
PEX	65	97.5
W	455	455
L	65	65
AEX	151	172.5