Investigation of Diffusion Rounding for Post-Lithography Analysis

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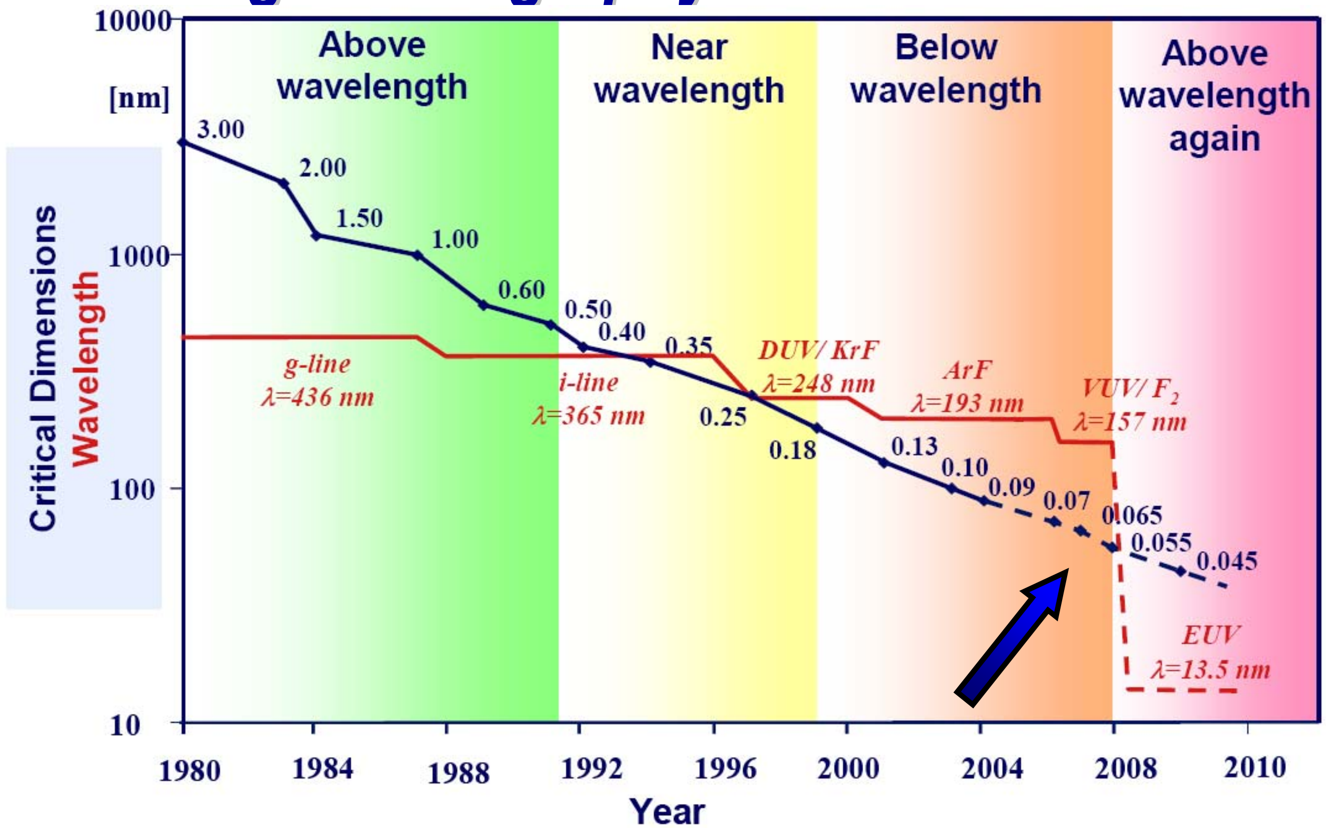
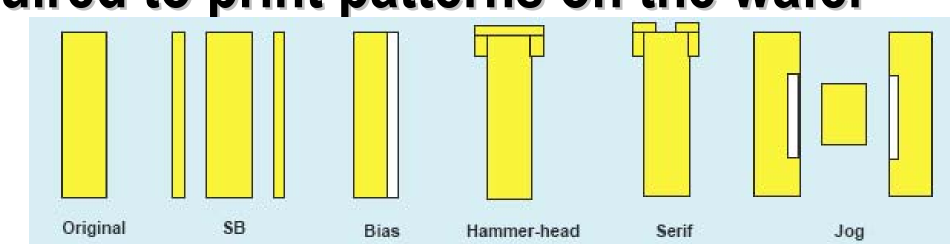
Subwavelength Lithography

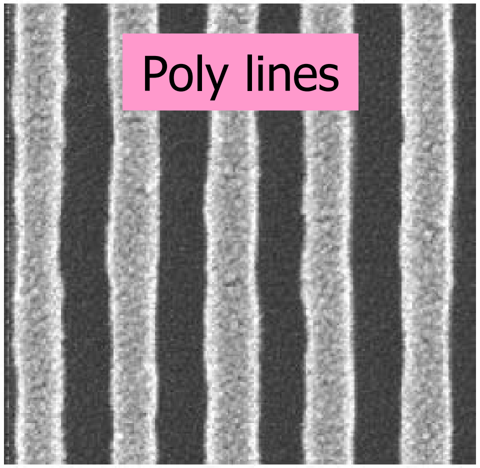


(Source: Infineon)

- Scaling of minimum feature size outpaced the wavelegnth (<0.35um) → subwavelength lithography regime
- Significant variations are expected
- Enhancement techniques are required to print patterns on the wafer (RETs): e.g., OAI, OPC, PSM, SRAFs

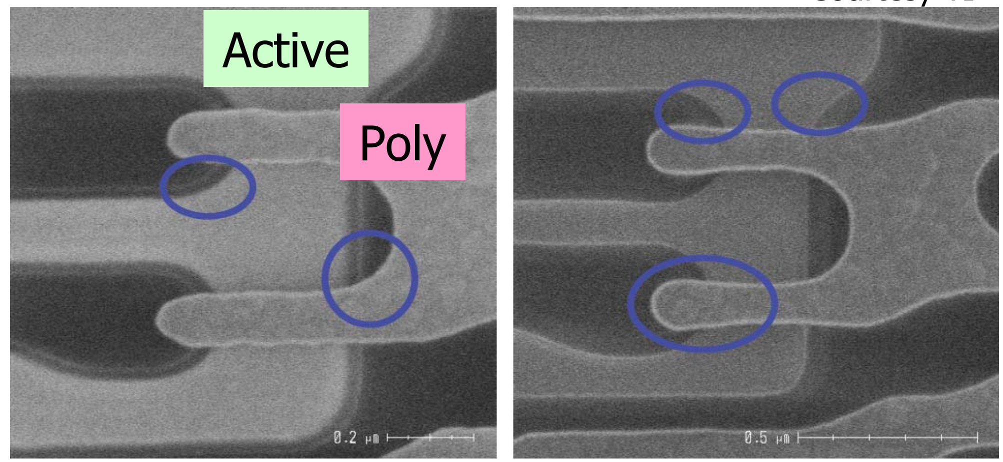


Non-rectilinear Gate and Diffusion

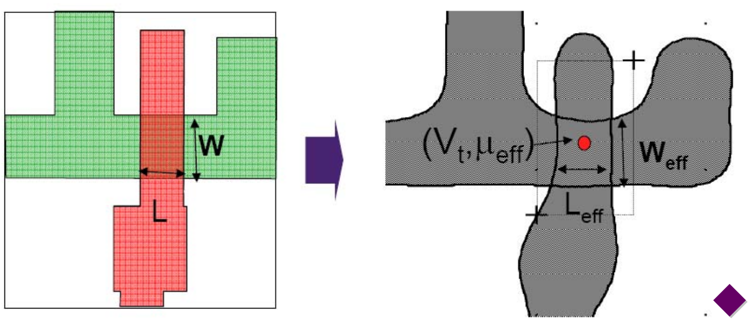


Line Edge Roughness (LER)

Courtesy TI

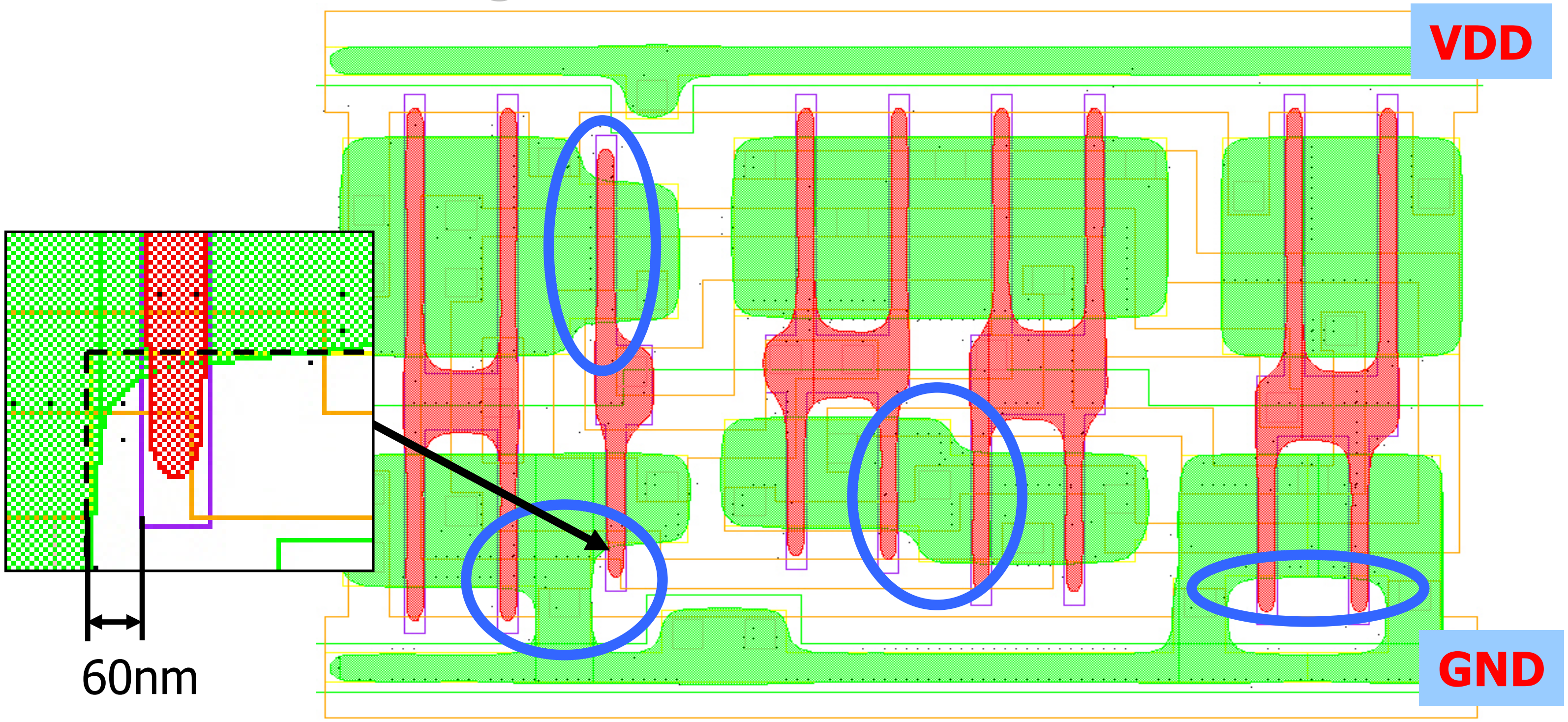


- **Gate/diffusion profile loses definition and getting rougher**
  - **Bigger impact on performance (delay and leakage)**
- **Non-rectilinear poly gate and diffusion (SEM images)**
  - **LER**
    - **ITRS suggest 3~5nm LER control in < 50nm node**
    - **Expected to dominate total parameter fluctuations at 32nm**
  - **Poly and *diffusion rounding***
  - **Necking, flaring, line-end shortening, etc…**
- **Accurate modeling is required to quantify the impact (PLS)**
  - **Printed images are not restricted to simple rectilinear geometries**
  - **Current tool can not handle non-rectilinear gate or diffusion shape (e.g., HSPICE)**



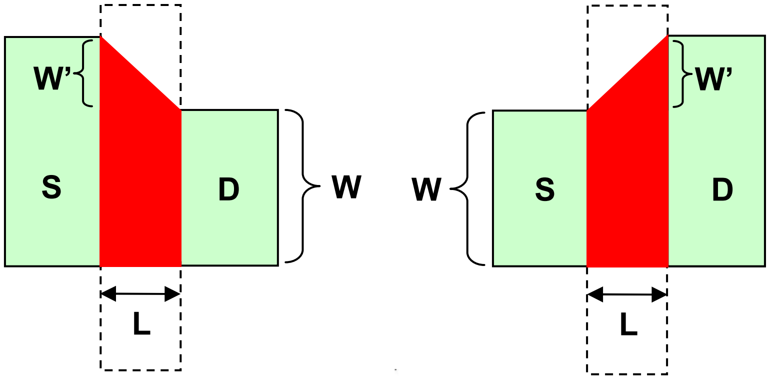
Courtesy Synopsys

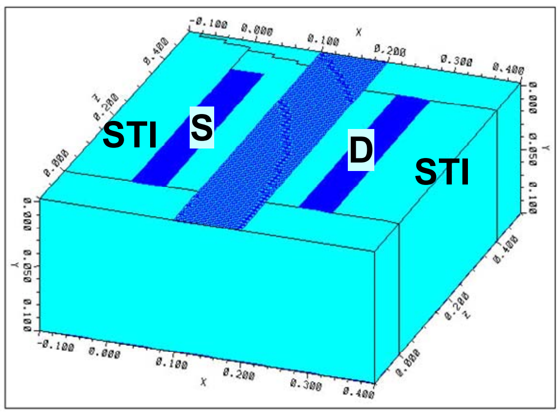
Diffusion Rounding

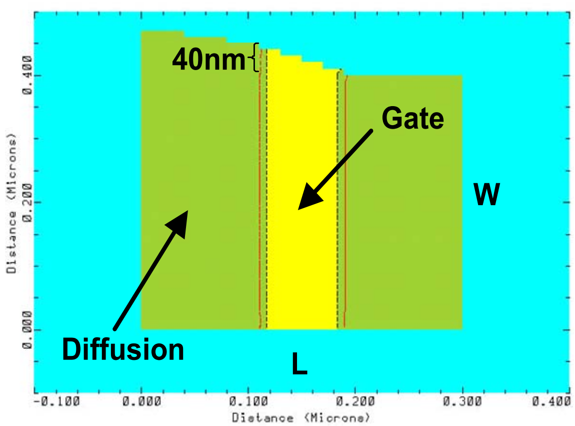


- Aggressive scaling to improve performance (e.g., 90nm → 65nm → 45nm, and so on)
  - Neither poly nor diffusion is rectilinear
- Diffusion rounding
  - Non-rectangular shapes: e.g., L and T-shaped layout to connect to power rails
  - Size mainly depends on the minimum distance from gate poly to the bent diffusion
    - E.g., 60nm in 90nm node
  - Not negligible impact: several 10s of nm of rounding under the gate in 90nm node
  - Location: source (common) or drain side of devices

TCAD Simulation Setup

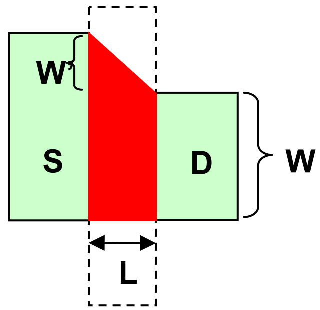




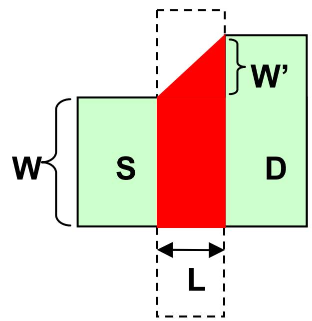


Parameters	Value
$L_{physical}$	70nm
Width	400nm
Vdd	1.2V
T_{ox}	2nm
Channel doping	3.0e+18 cm^{-3}
NSUB	3.0e+15 cm^{-3}
Junction depth	14nm
Line-End Extension	100nm
S/D Electrode length	50nm
S/D Electrode width	400nm
S/D Region to Gate poly	50nm
STI width	100nm
STI depth	100nm

TCAD Simulation Results



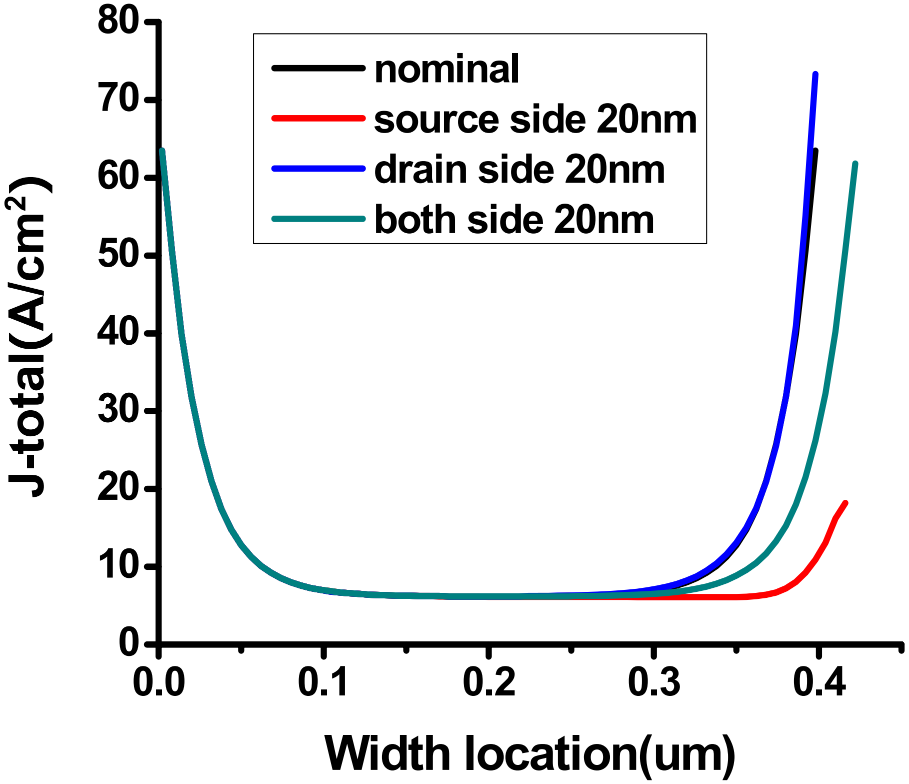
Source side		nominal	5nm	10nm	20nm	30nm	40nm	20nm both	40nm both
NMOS	I_{on} (μA)	232	235	236	237	238	241	245	255
	I_{off} (pA)	249	241	232	217	206	198	259	269
	$I_{on\ norm}$	1.00	1.01	1.01	1.02	1.03	1.04	1.06	1.10
	$I_{off\ norm}$	1.00	0.96	0.93	0.87	0.83	0.79	1.04	1.08

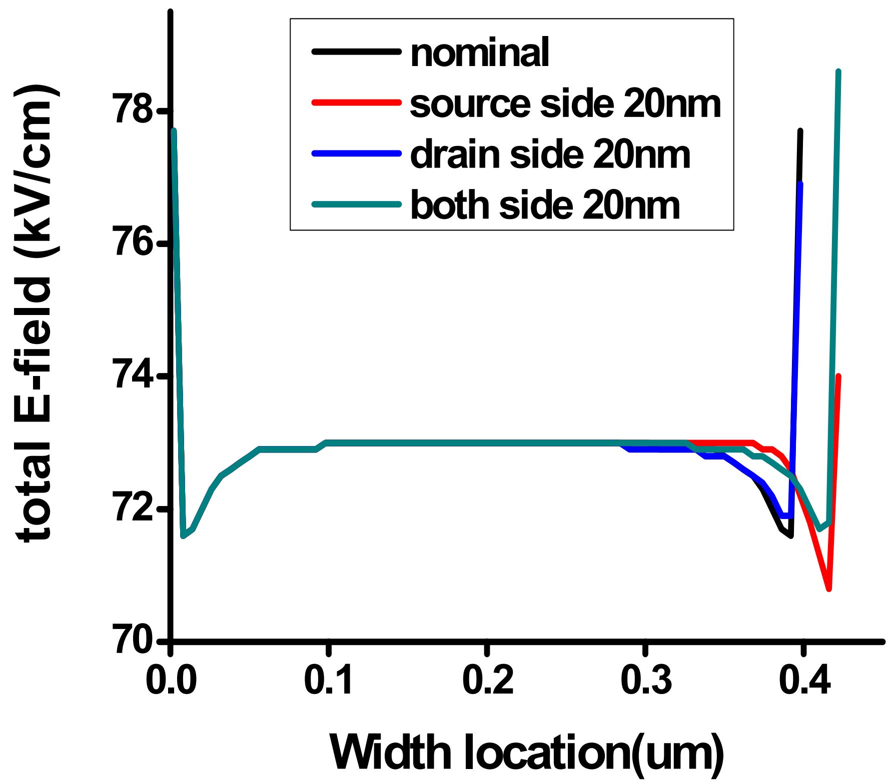


Drain side		nominal	5nm	10nm	20nm	30nm	40nm
NMOS	I_{on} (μA)	232	234	235	237	239	240
	I_{off} (pA)	249	289	279	254	255	245
	$I_{on\ norm}$	1.00	1.01	1.01	1.02	1.03	1.04
	$I_{off\ norm}$	1.00	1.16	1.12	1.02	1.02	0.98

- Small change on I_{on} in both cases
- I_{off} decreases by source-side diffusion rounding (~20% in NMOS, ~17% in PMOS),
- But, drain-side slope makes I_{off} increase then saturates as slope size increases (e.g., 20nm cases)

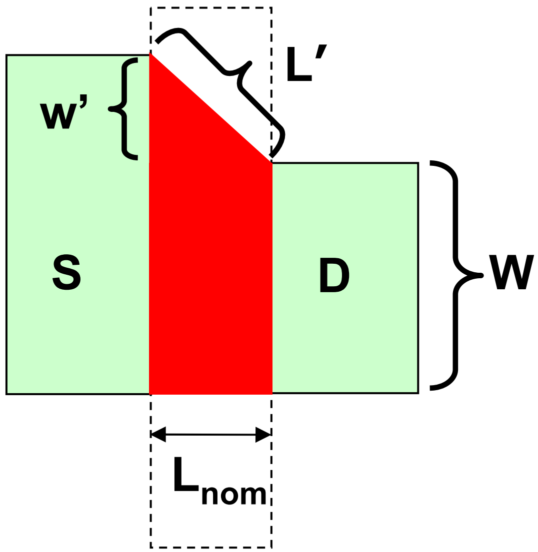
Total Current Density and E-field





- **leakage reduction by source-side diffusion rounding only**
  - Source-side diffusion rounding increases the W_{eff} at source side → reduce NWE → increases V_{th} → reduce leakage exponentially
  - Source-side diffusion rounding decreases E-field at the source junction: L_{eff} (at the source side junction) > L_{nom}

Simple Models for Diffusion Rounding Effects



- For I_{on}, effective gate area change

$$I_{on} = I_{on\_nom} * \left[1 + \frac{(w'/2)}{W} \right]$$

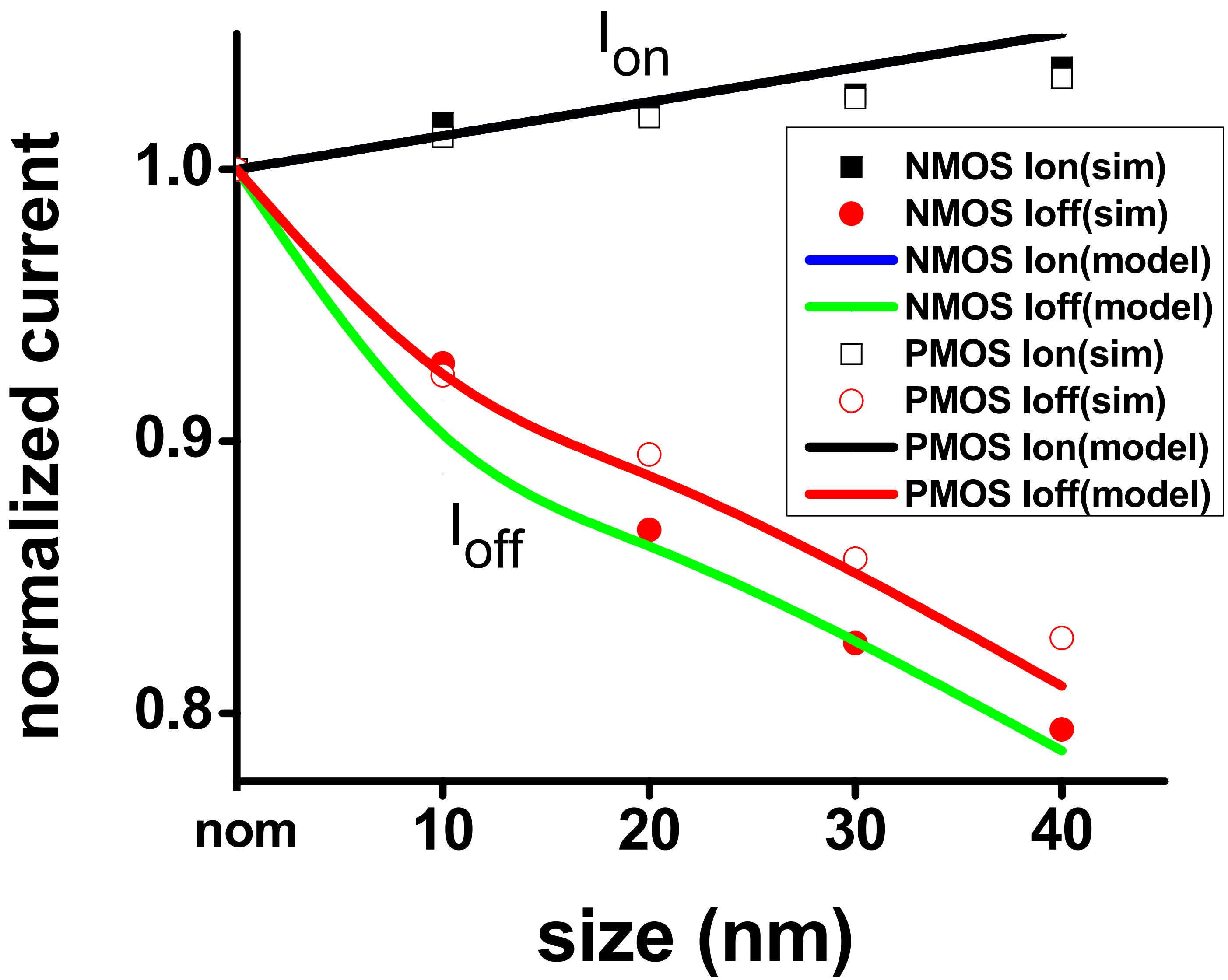
- For I_{off}, exponential function of L_{eff} at the edge
  - Only source-side rounding (common)
  - Ignore drain-side diffusion rounding

$$I_{off} = I_{off\_nom} * K_1 * \exp\left(\frac{L_{nom}}{L'}\right)$$

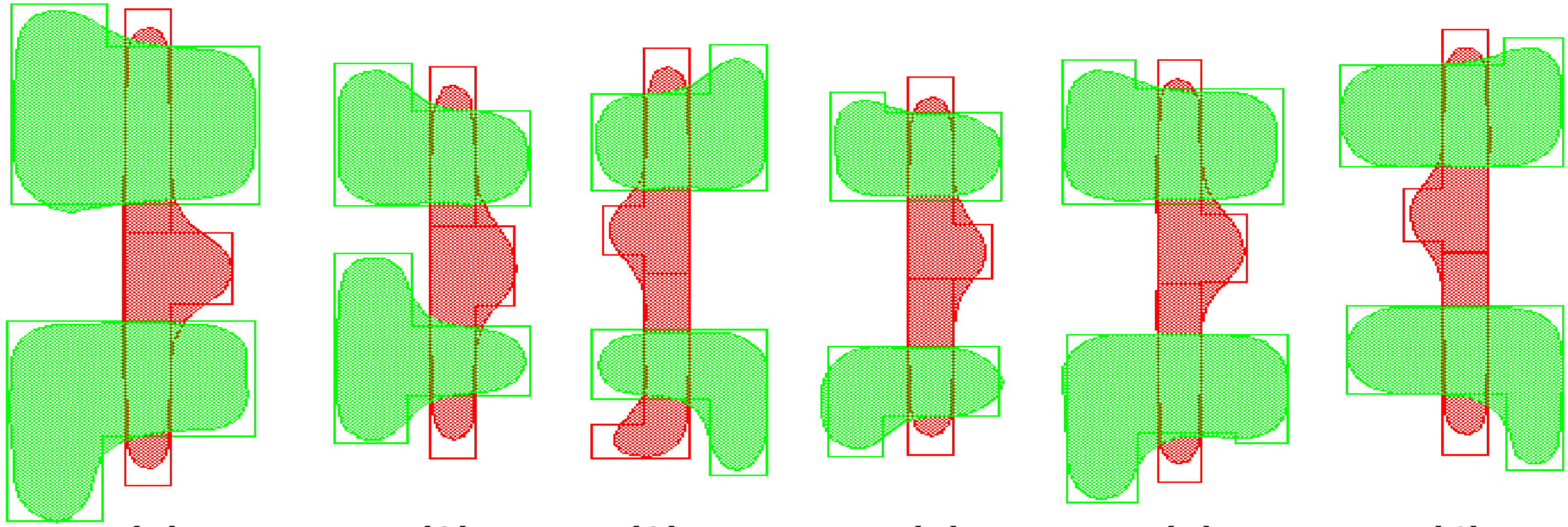
where, K_1 is fitting parameters (NMOS: 0.33, PMOS: 0.34)

L' is effective channel length at the edge ($= \sqrt{w'^2 + L_{nom}^2}$)

Model Accuracy



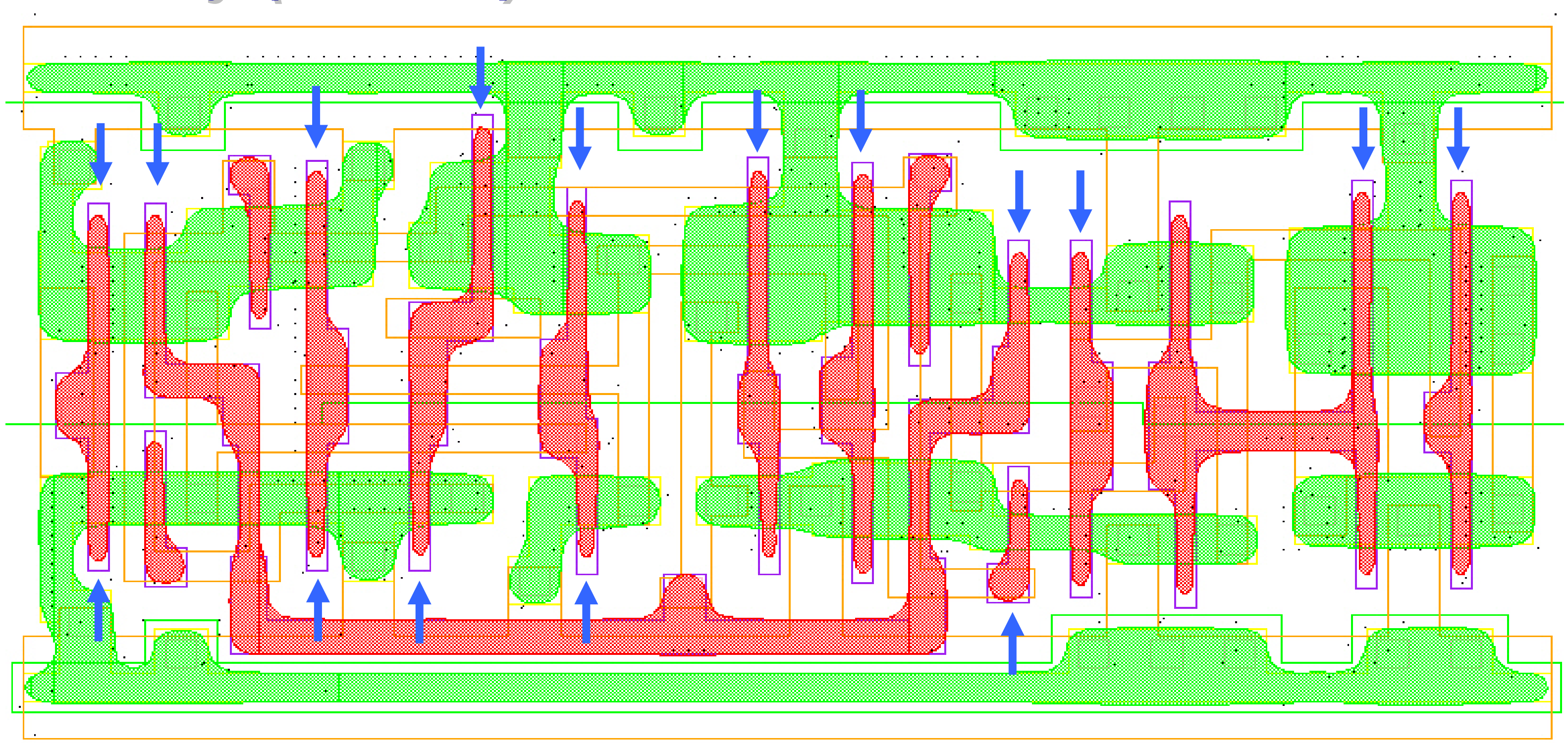
Verifications



(1) (2) (3) (4) (5) (6)

device #	W_{drawn} (nm)	nominal		litho-contour (TCAD)		contour2nom (%)		model			model2contour (%)	
		I_{on} (μA)	I_{off} (pA)	I_{on} (μA)	I_{off} (pA)	I_{on}	I_{off}	W' (nm)	I_{on} (μA)	I_{off} (pA)	I_{on}	I_{off}
1	274	136.15	6.53	137.48	4.88	0.98	-25.24	15	139.88	4.95	***1.74***	***1.41***
2	164	85.33	5.87	90.63	3.59	**6.21**	**-38.85**	20,15	91.40	3.71	***0.85***	***3.50***
3	164	85.33	5.87	87.81	5.20	2.91	-11.36	19	88.62	5.12	***0.93***	***-1.51***
4	164	85.33	5.87	88.96	5.43	4.25	-7.41	11	87.23	5.22	***-1.94***	***-4.02***
5	234	117.66	6.29	120.09	5.43	2.07	-13.71	15	120.17	5.55	***0.07***	***2.18***
6	209	106.11	6.14	108.64	5.70	2.38	-7.19	19	109.33	5.36	***0.63***	***-5.92***

Case Study (DFFX1)

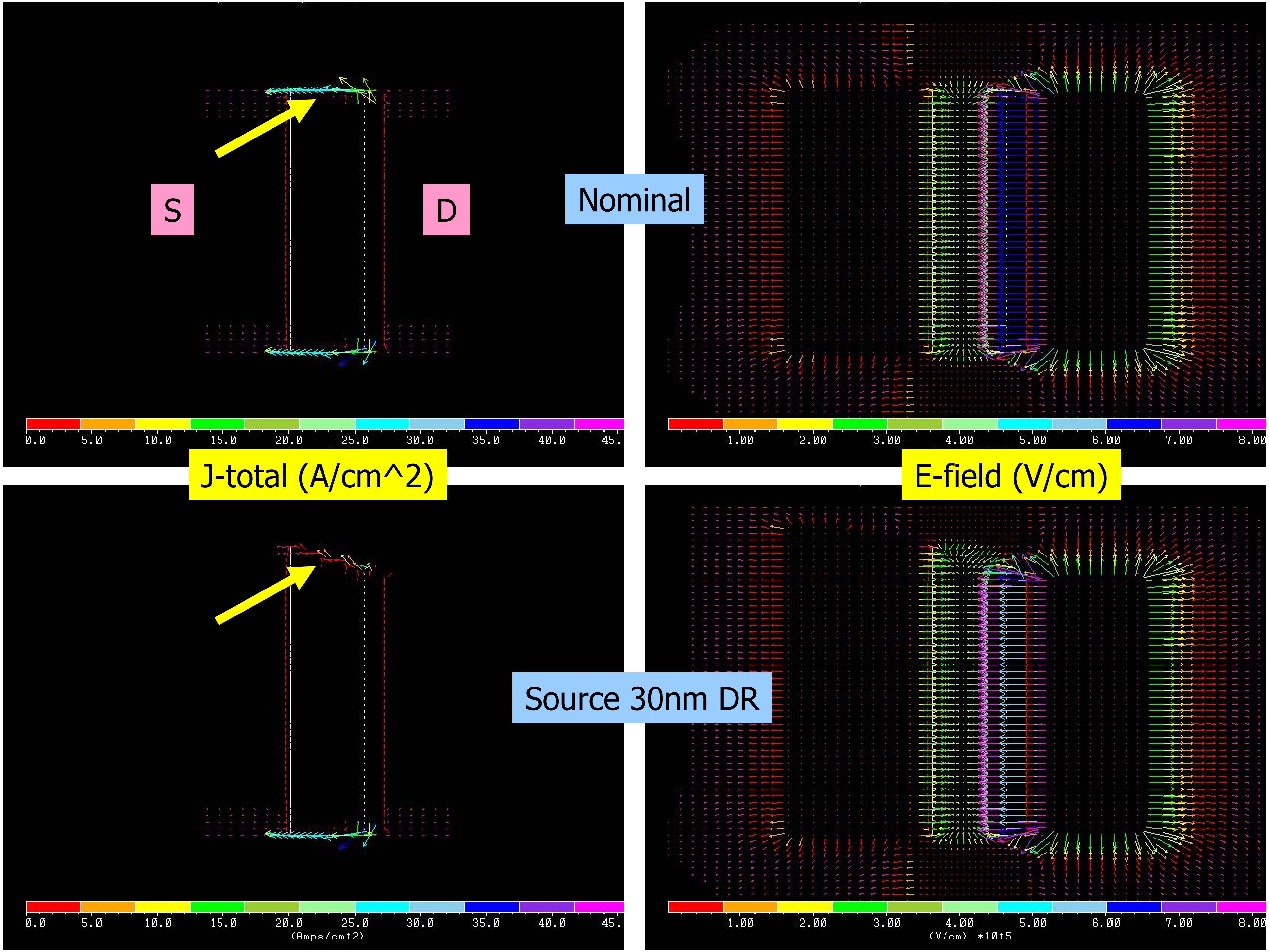


		nominal (w/o diffusion rounding)	w/ diffusion rounding	*delta (%)*
leakage (nW)		138.69	83.49	***39.8***
clk→q (ps)	fall	70.57	68.54	***2.9***
	rise	76.07	74.07	***2.6***
setup time (ps)	fall	20.43	18.08	***11.5***
	rise	42.71	35.01	***18.0***

Conclusions and Future Work

- Investigate the impact of the non-rectilinear shape of diffusion on the on- and off-currents
- Diffusion rounding on the source side leads to a fairly appreciable reduction in subthreshold current, while at the same time providing a small boost in on-current.
- Propose simple models to capture the diffusion rounding effects in post-lithography analysis.
- The test patterns show that neglecting diffusion rounding can lead to 7% (40%) error in predicting I_{on} (I_{off}).
- The proposed models show good match to simulation results and are within 2% in Ion and 6% in Ioff.
- Case study of DFFX1 shows that diffusion rounding potentially reduces leakage, CLK-Q delay, and setup time.
- General models for various types of device shape irregularities
  - No LER effect or poly flaring in this analysis
  - LER + poly flaring (necking) + diffusion rounding + etc..

Thank you !!



S
D
Nominal
J-total (A/cm^2)
E-field (V/cm)
Source 30nm DR
0.0 5.0 10.0 15.0 20.0 25.0 30.0 35.0 40.0 45.
(Amps/cm↑2)
1.00 2.00 3.00 4.00 5.00 6.00 7.00 8.00
(V/cm) *10↑5