Exploring High-Speed Low-Power Hybrid Arithmetic Units at Scaled Supply and Adaptive Clock-Stretching

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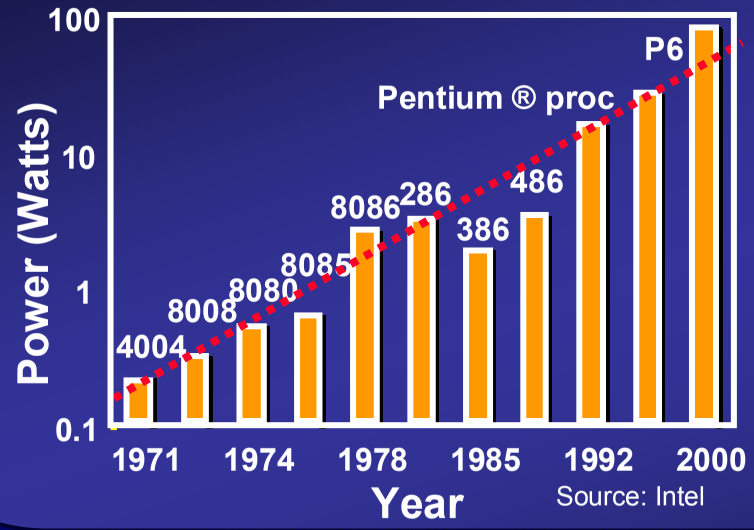
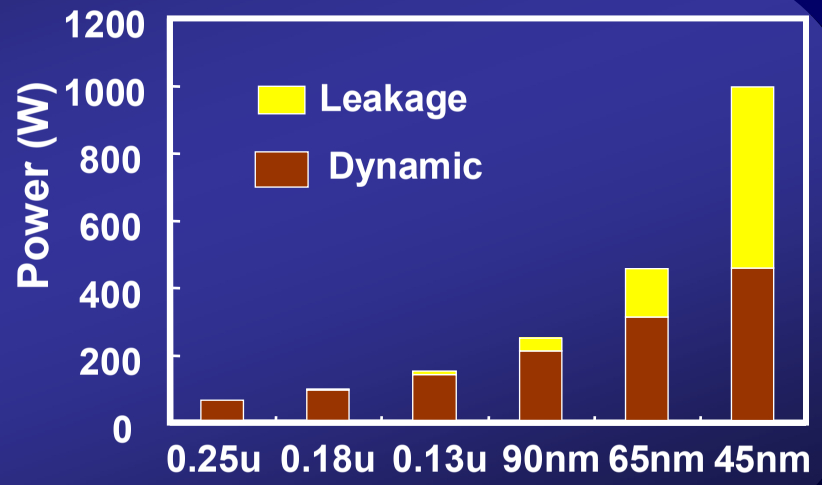
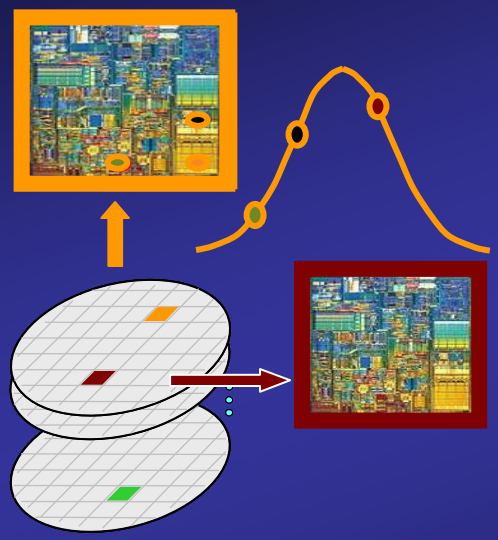
Motivations

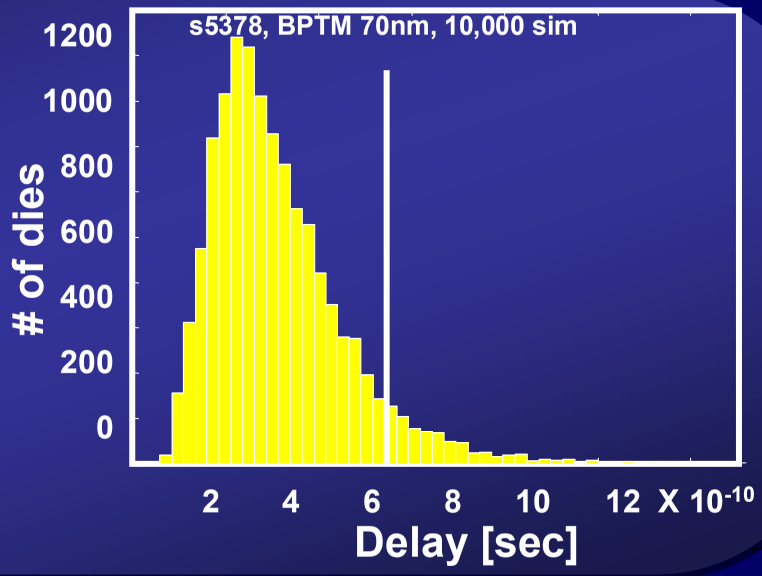
Power





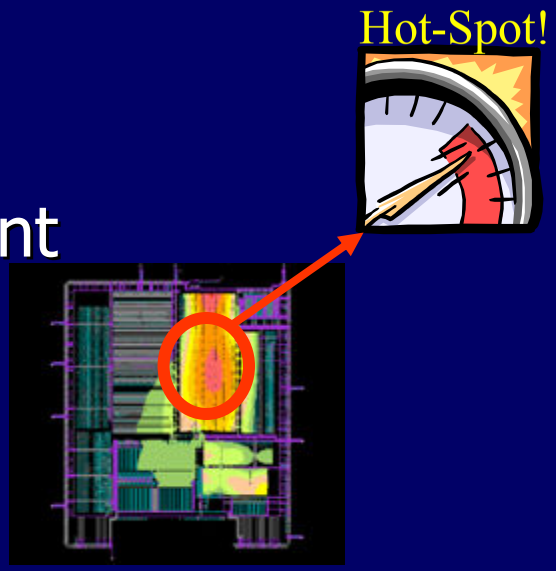
Robustness



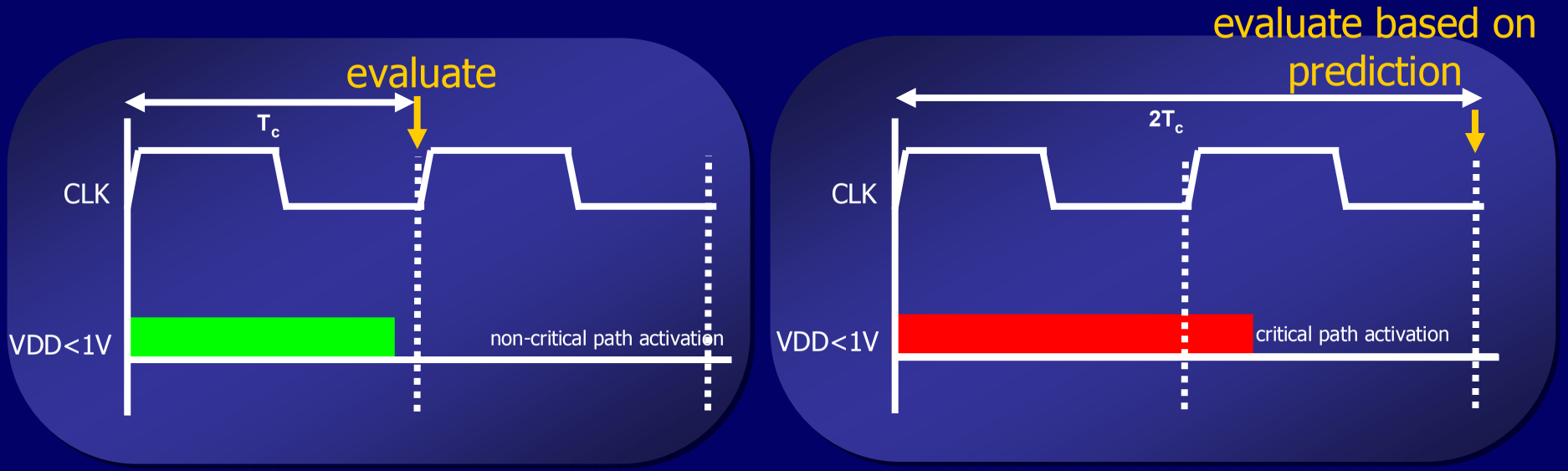


Why Arithmetic Units?

- Typical microprocessor hotspots: integer execution units, floating point units
- Power – performance tradeoffs are critical for such blocks
- Possible solution: tradeoff performance with power → not good for high performance systems
- Our solution: Reduce the power at rated frequency at the cost of small throughput penalty

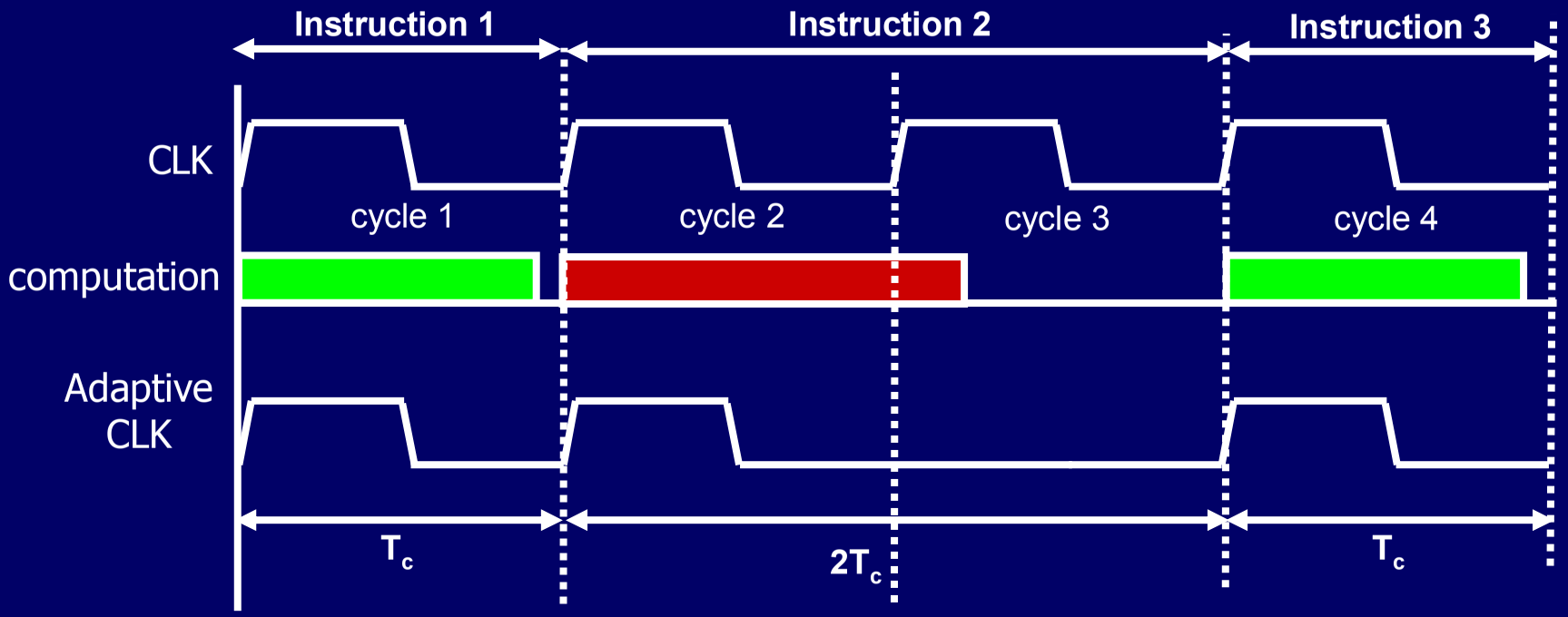


Basic Idea



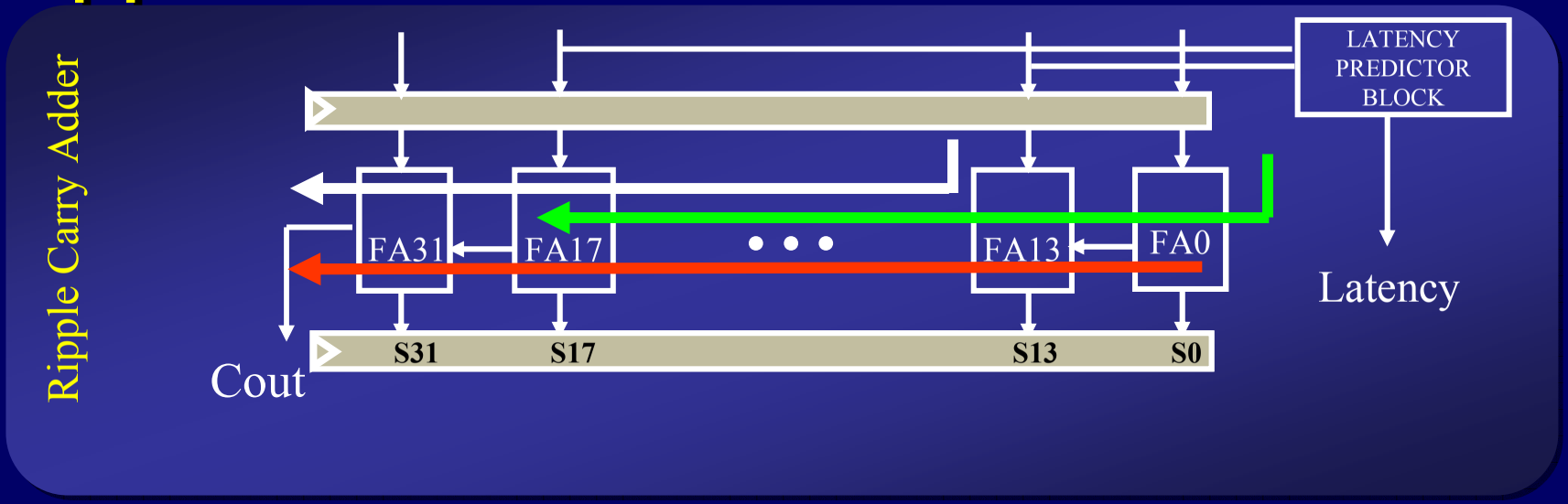
- Important points:
  - Scale down the supply while making *delay failures predictable*
  - *Avoid* the failures by *adaptive clock stretching* while maintaining *rated clock frequency*
  - Ensure that critical paths are activated *rarely*

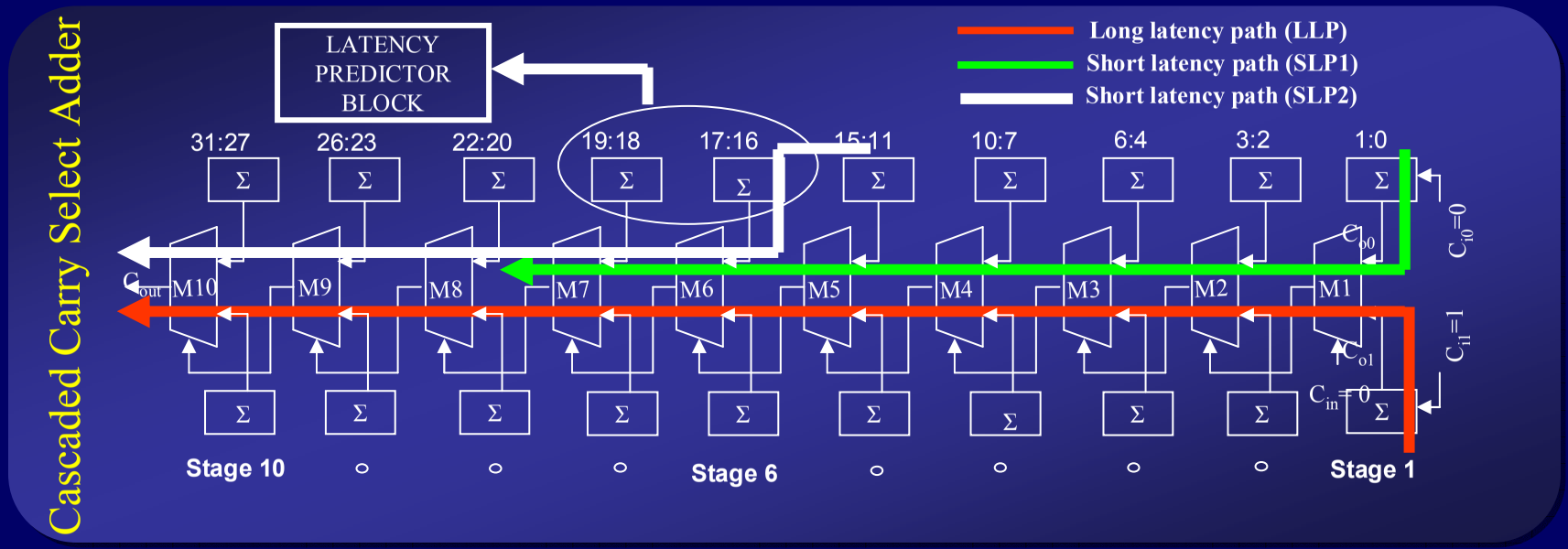
Adaptive Clocking



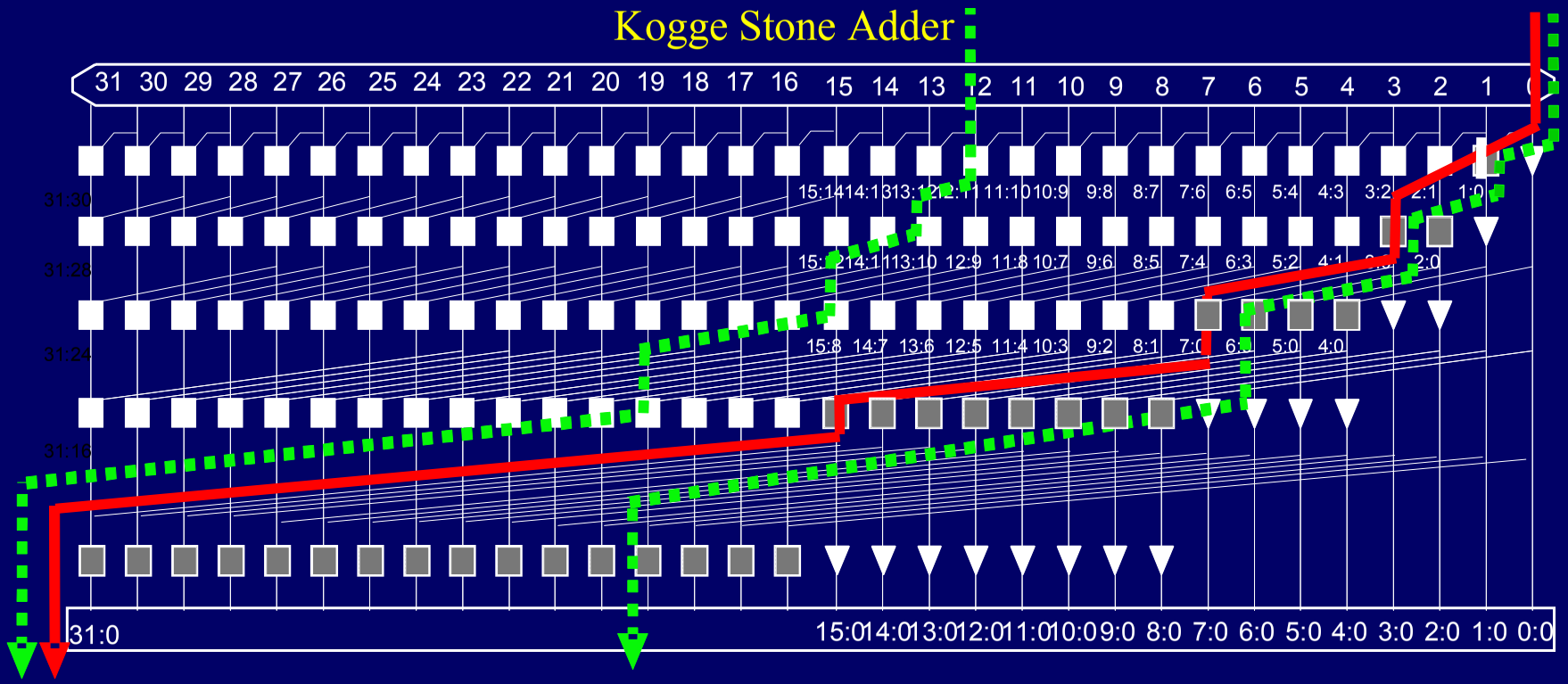
- Reduce the supply voltage
- Knock-off clock pulses occasionally

Application in Arithmetic Circuits



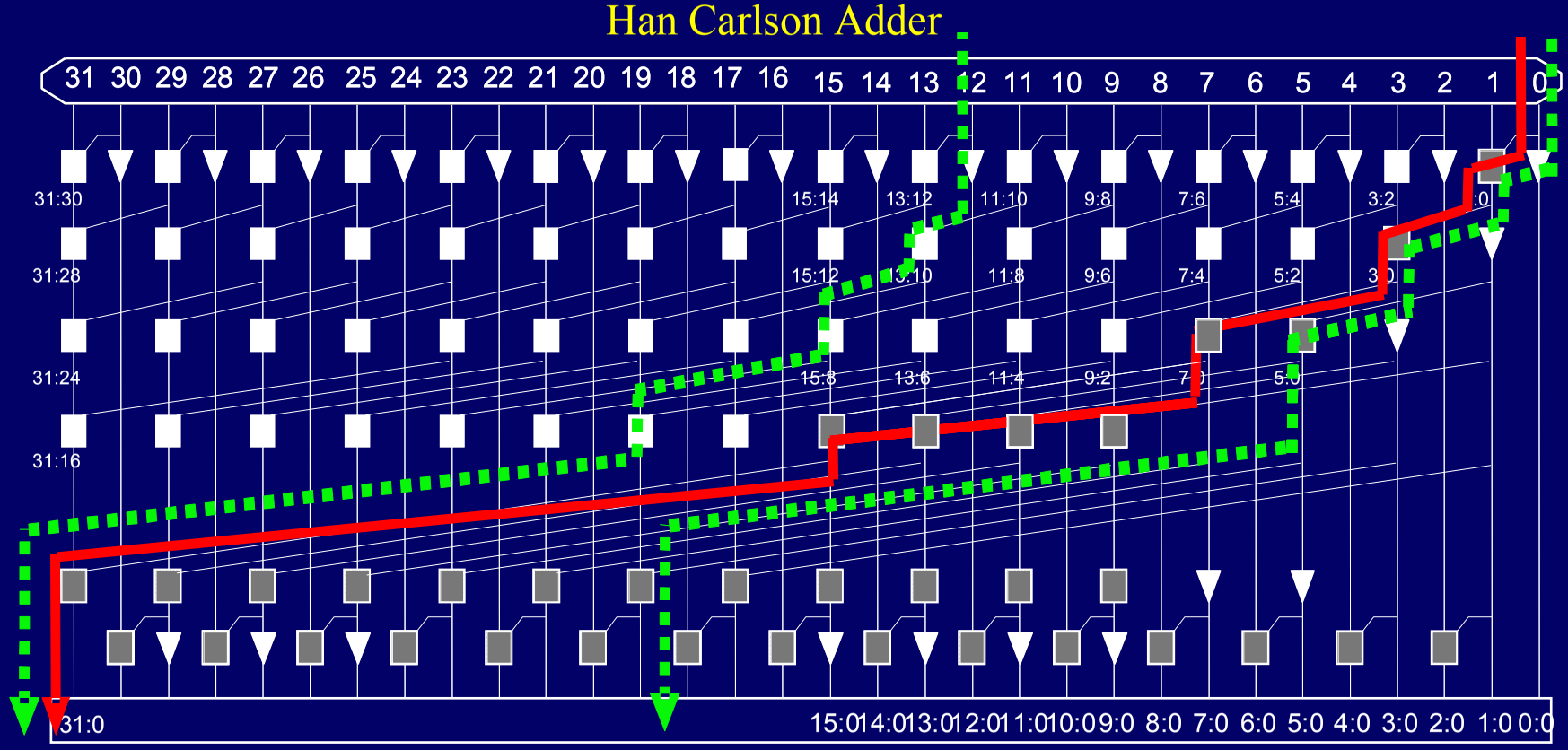


Application in Arithmetic Circuits



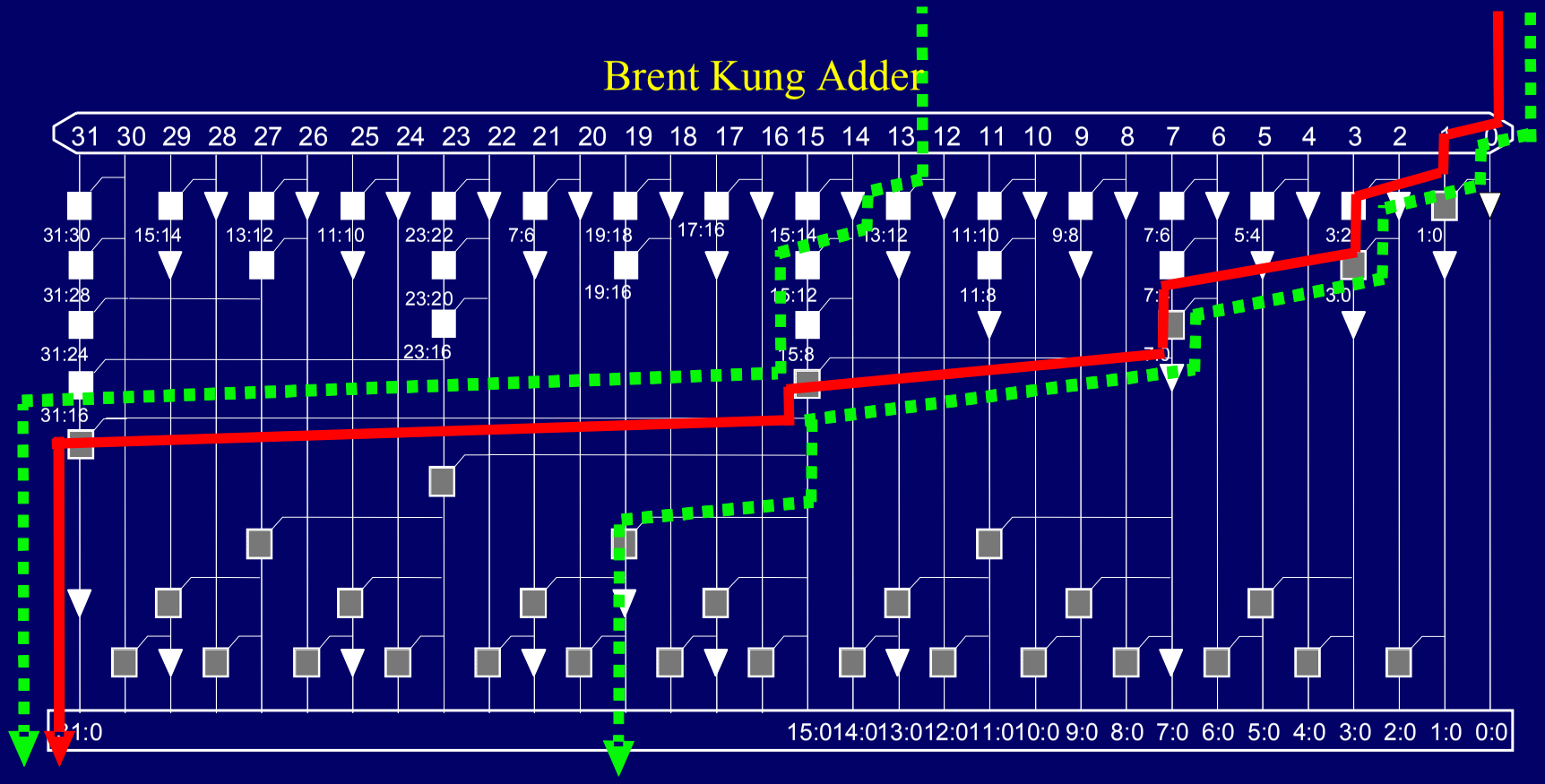
- Less timing slack between critical and off-critical paths

Application in Arithmetic Circuits



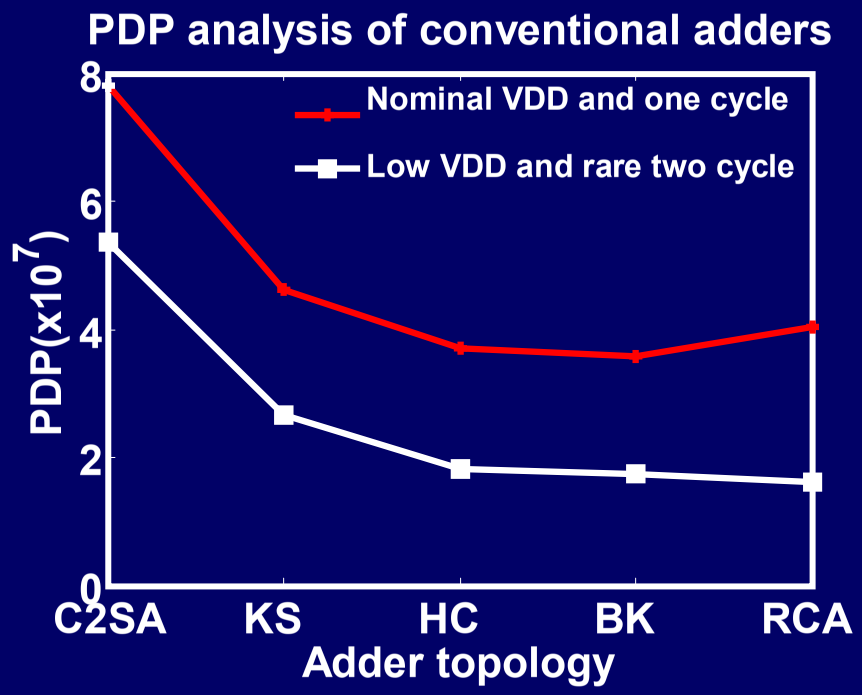
- More timing slack between critical and off-critical paths compared to Kogge-Stone

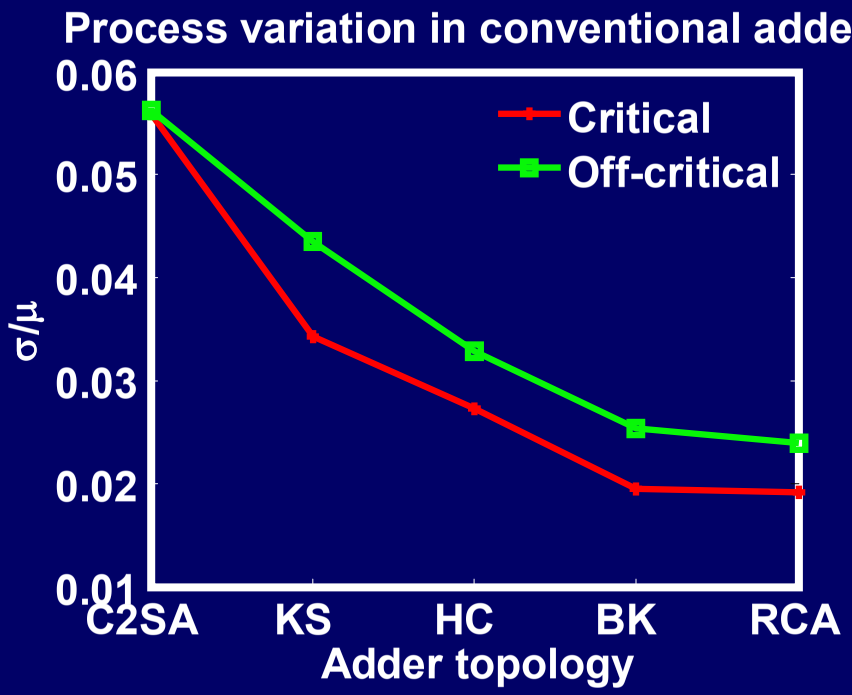
Application in Arithmetic Circuits



- More timing slack between critical and off-critical paths compared to Kogge-Stone/Han-Carlson

Simulation Results

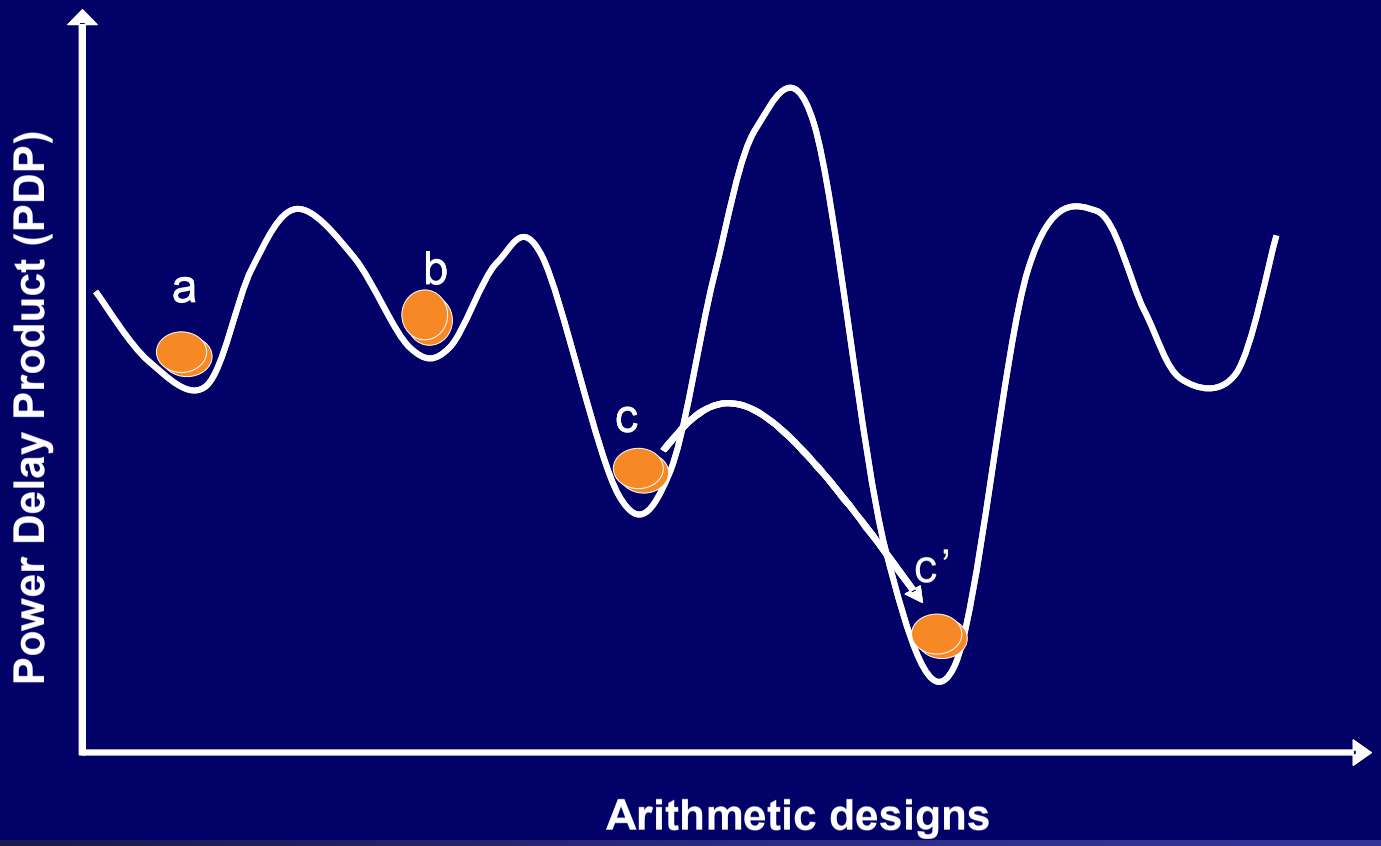




- Han-Carlson is better in terms of PDP and process variation

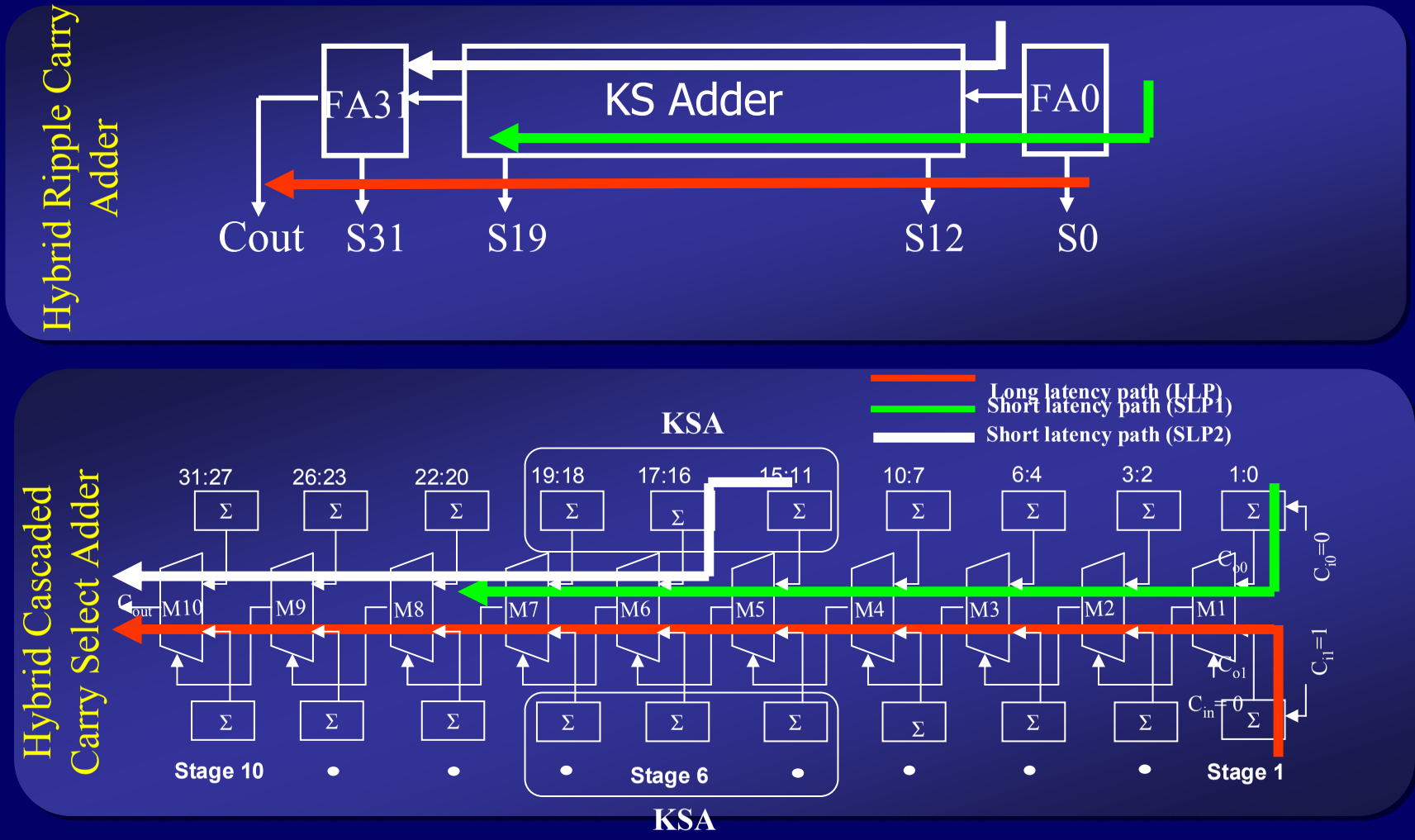
Can we make the design suitable for supply voltage scaling?

Hybrid Arithmetic Units: Concept



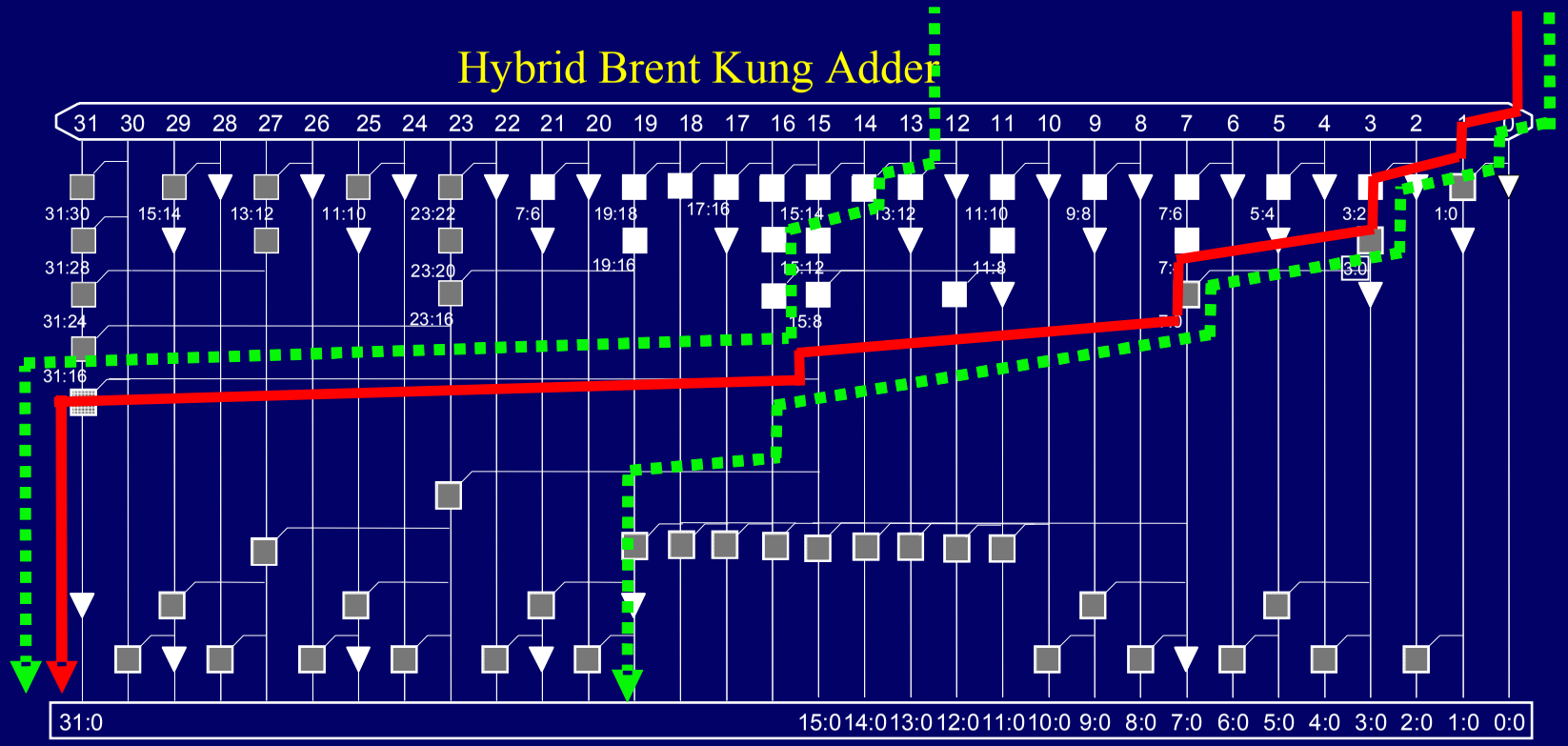
Hybrid designs can take us to better optima in PDP plane

Hybrid Arithmetic Units



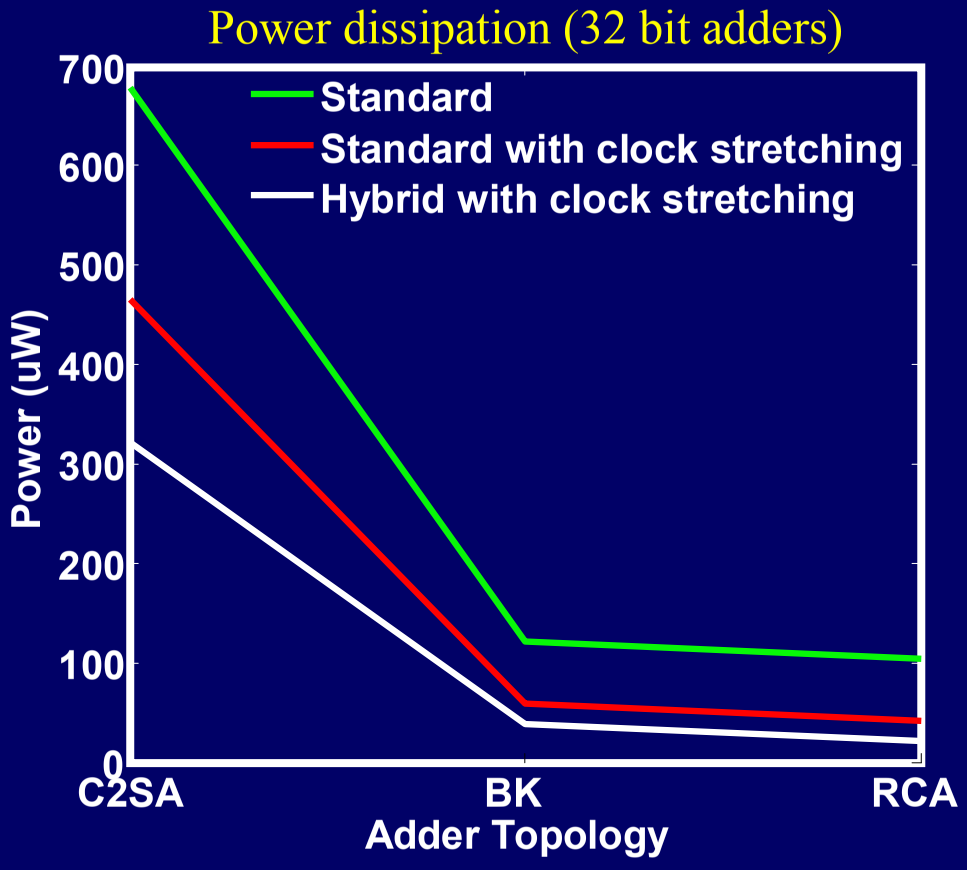
- Make the off critical paths *faster* by employing fast adders

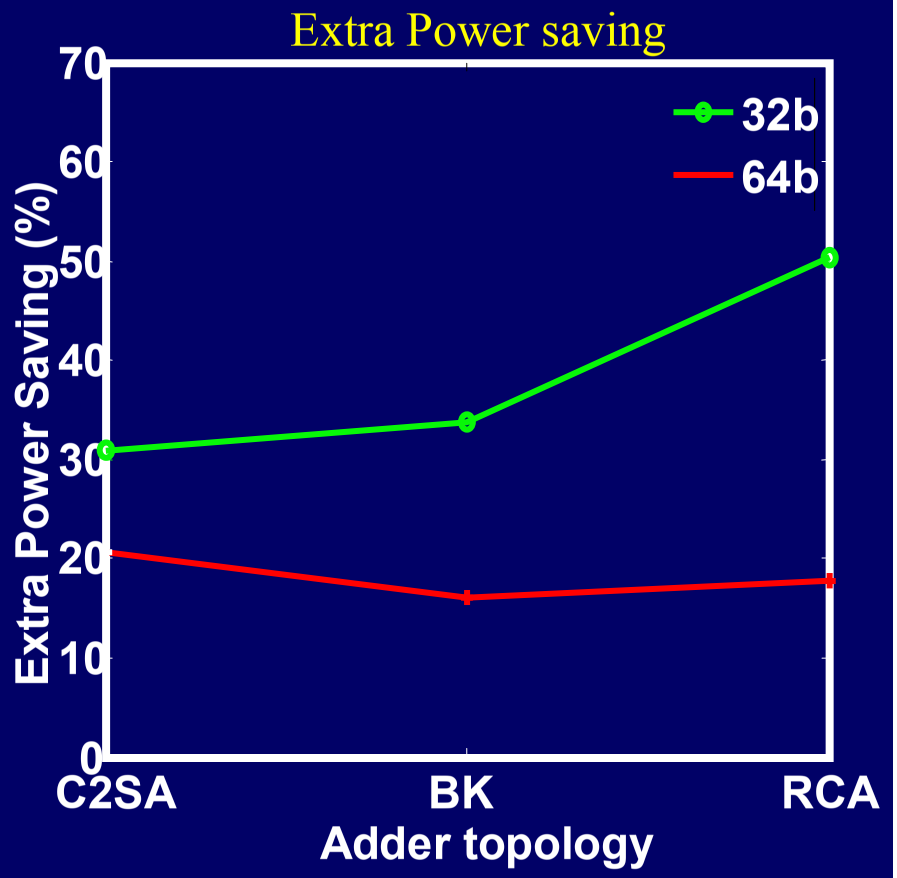
Hybrid Arithmetic Units



- Off critical paths are *sped-up* by Kogge stone type computation

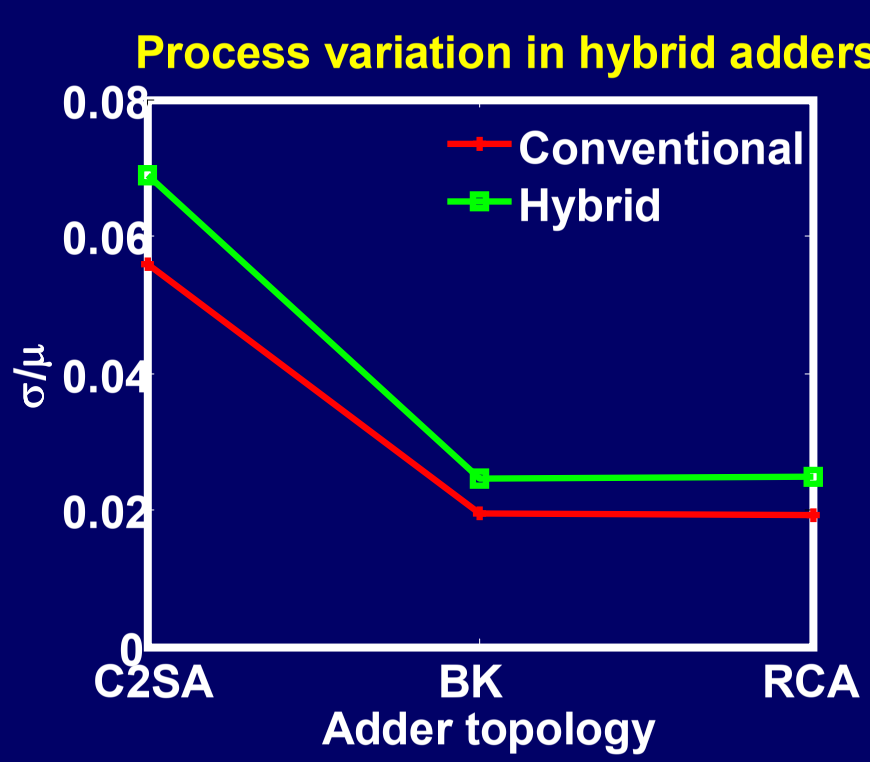
Simulation Results

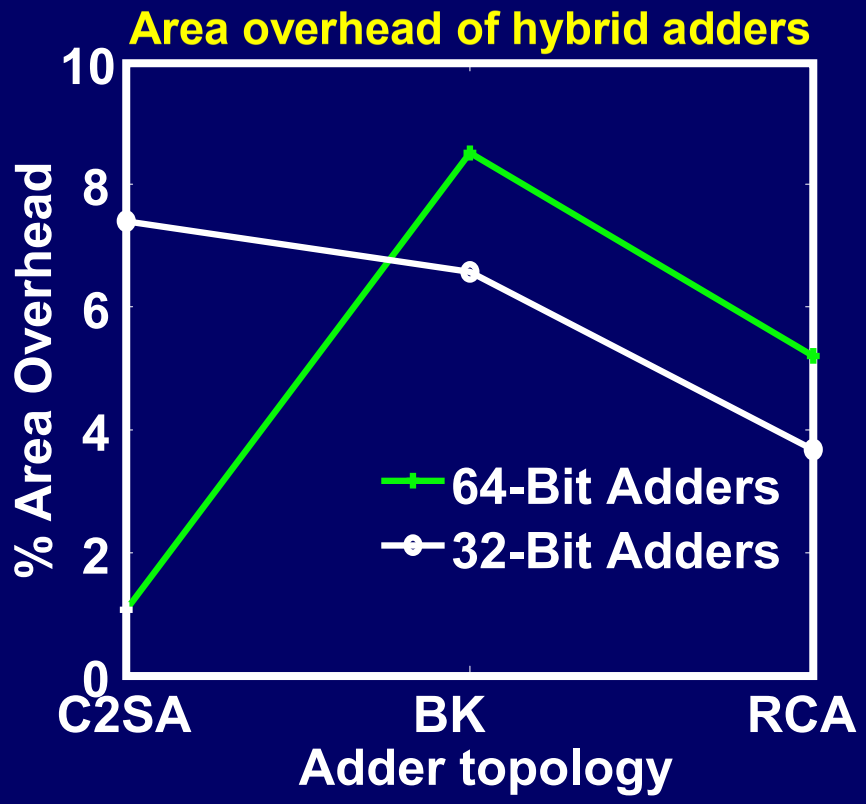




- Hybrid adders are very good in terms of supply scaling

Simulation Results

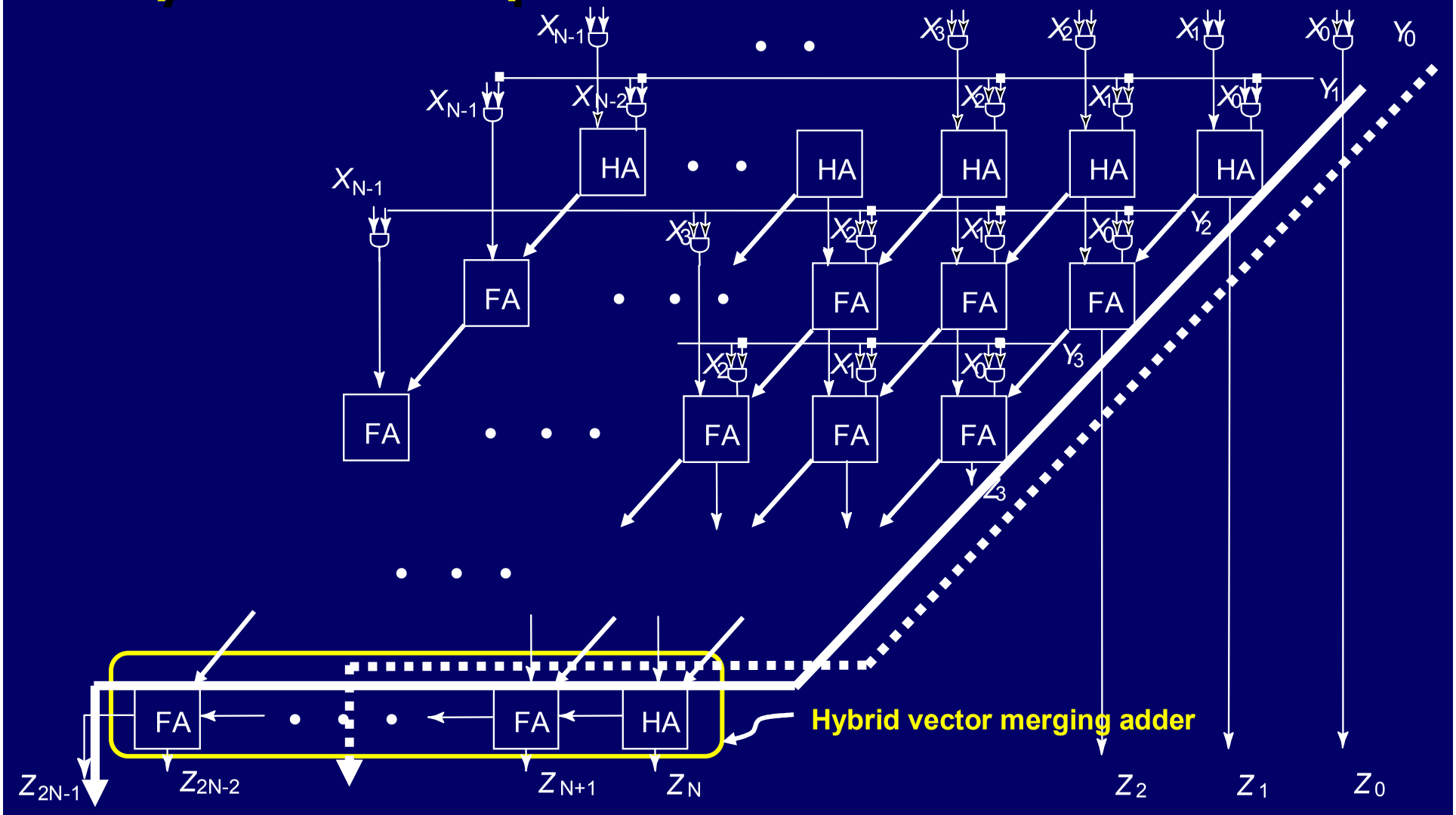




- Area overhead associated with hybrid design is minimal

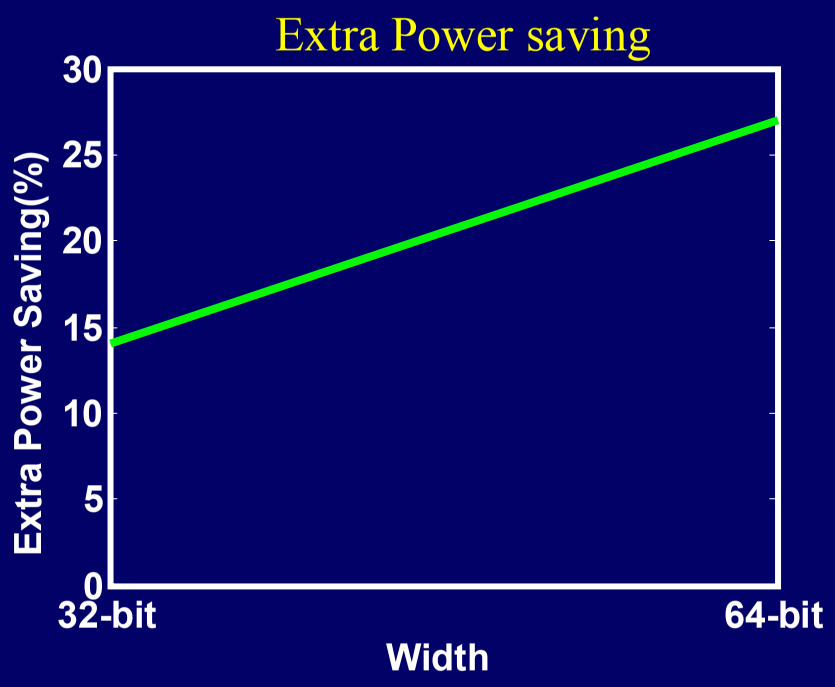
Can we apply similar technique to multipliers?

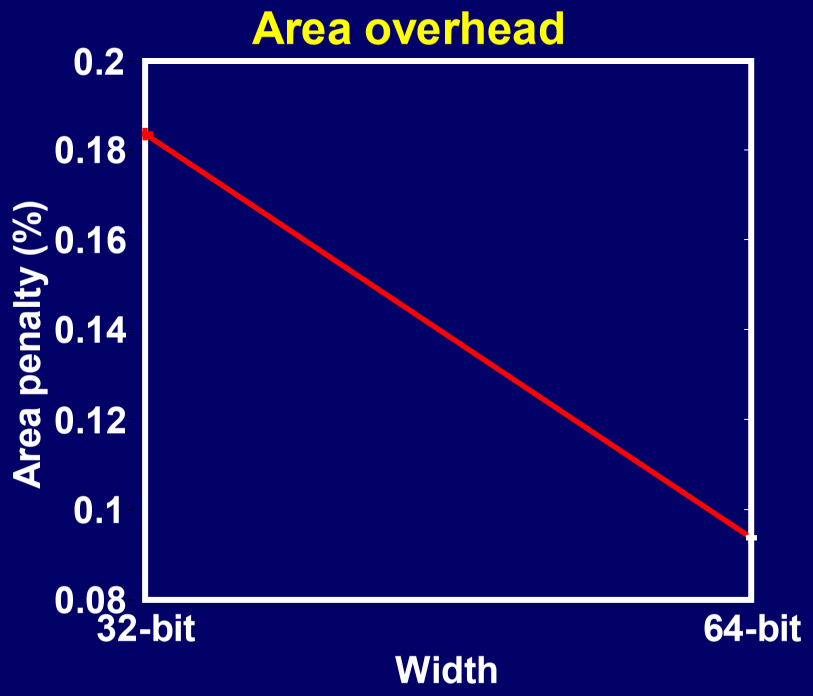
Hybrid Multiplier



- Use hybrid adder in the vector merging stage

Simulation Results





- Area overhead associated with hybrid design is minimal
- Hybrid design can be more beneficial for wide multiplier

Conclusions

- We explored various topologies of arithmetic units for aggressive supply voltage scaling/clock-stretching
- We proposed hybrid adder design for low power and improved yield
- We implemented hybrid adder for low power and high yield multiplier design

Thank You!

Acknowledgements

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