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NBTI Induced Performance Degradation in Logic and Memory Circuits: How Effectively Can We Approach a Reliability Solution?

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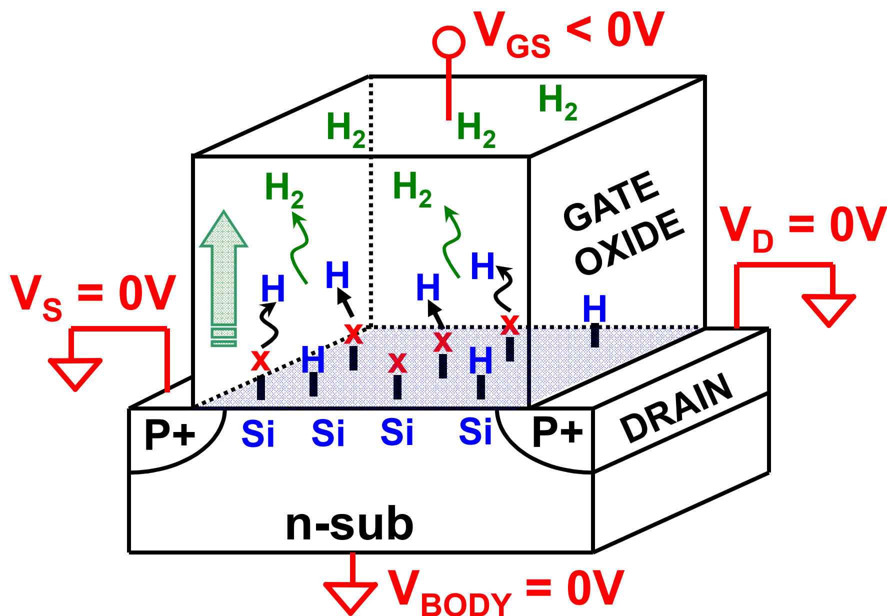
Purpose

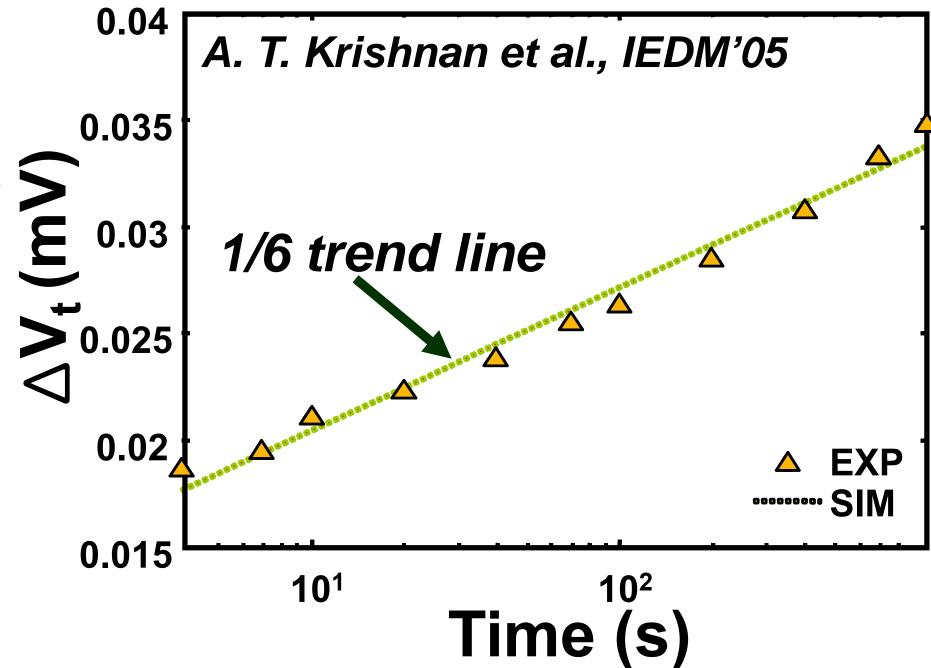
- Temporal NBTI degradation of MOSFET is an essential design challenge in Nano-Scale Technology
- Various design techniques
- Comparison & Evaluation of different approaches for random logic circuits and memory arrays
- Establish a realistic, yet efficient circuit design solutions under NBTI

Outline

- **Modeling NBTI**
  - Device level model based on Reaction-Diffusion framework
  - Circuit compatible simulation model
- **NBTI in Random Logic Circuits**
  - Impact in circuit f_{MAX}
  - Reliability-Aware Design Techniques
- **NBTI in Memory Array**
  - Impact in READ & WRITE stability
  - Reliability-Aware Design Techniques
- **Conclusion**

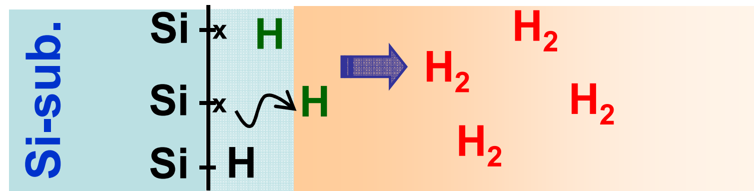
Negative Bias Temperature Instability

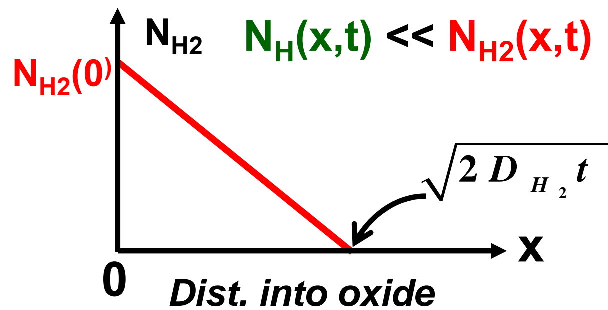


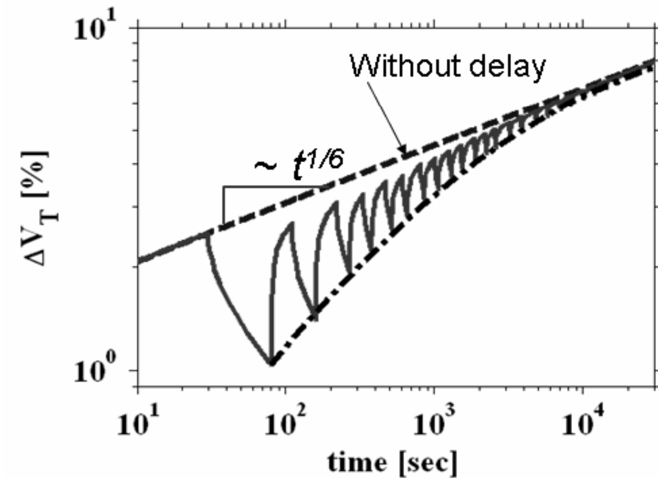


- Generation of Interfacial trap (N_{IT}) generation at Si/SiO_2
- With time, V_T ↑, subthreshold slope (S) ↑, mobility ↓
- Drive current (I_{DS}) reduces and affects the PMOS speed
- ***Overall reduction in PMOS life***

Reaction Diffusion Based Model*







Reaction

$$\frac{dN_{IT}}{dt} = k_F[N_0 - N_{IT}] - k_R N_{IT} N_H^{(0)} \approx 0$$

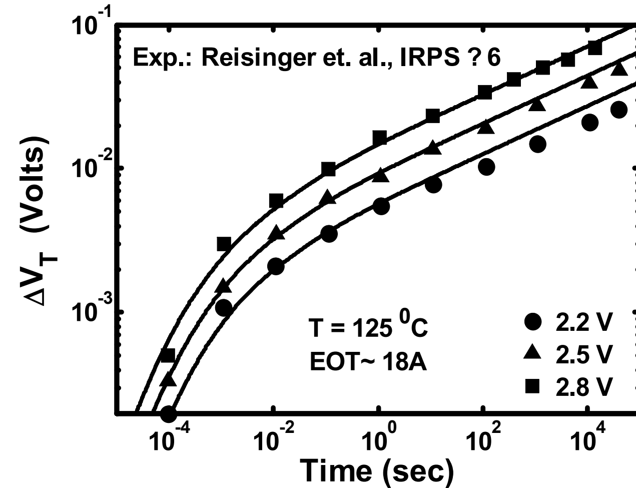
Diffusion

$$N_{IT}(t) = \frac{1}{2} N_{H_2}^{(0)} \cdot \sqrt{D_{H_2} t}$$

H-H$_2$ Conversion

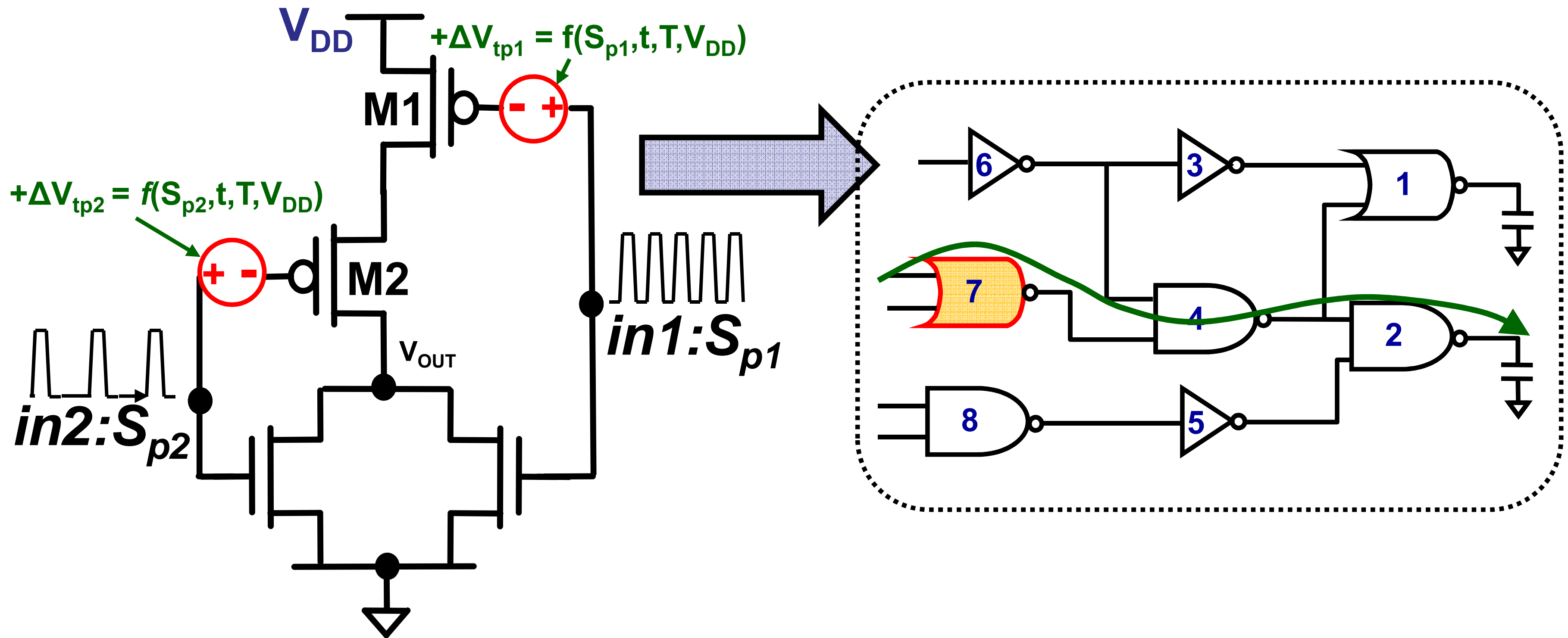
$$N_{H_2}^{(0)} = k_H \left(N_H^{(0)}\right)^2$$

$$N_{IT}(t) = \left(\frac{k_F N_0}{k_R}\right)^{2/3} \left(2k_H^{\,2} D_{H_2} t\right)^{1/6}$$



*Chakravarthi et. al., IRPS '04; Varghese et. al. IEDM '05

Circuit Simulation Model



- NBTI degradation represented in voltage source
- ΔV_{tp} depends on input signal probability (S_p), time (t), temperature (T), and stress voltage (V_{DD})
- Compact circuit simulation model

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NBTI in Random Logic Circuits

RD Model

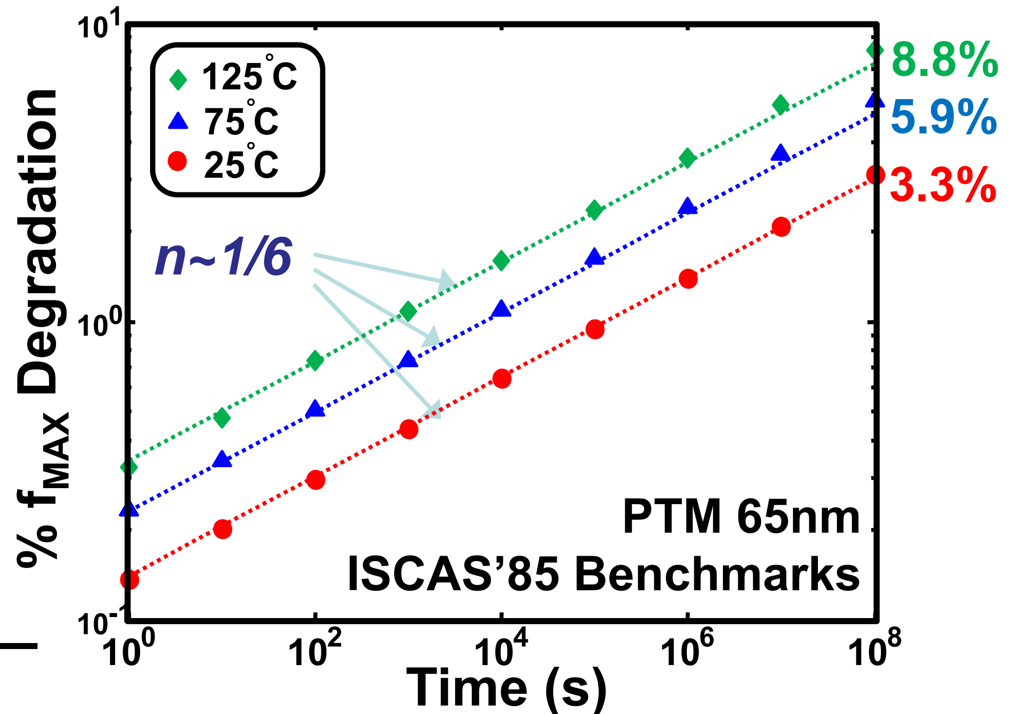
$$\Delta V_t(t) = (m_\mu + 1)\frac{qN_{IT}(t)}{C_{ox}} \simeq K \times t^{1/6}$$

Analytical Gate Delay Model

Delay = f(V_{DD}, Temp., Signal Prob., Time)

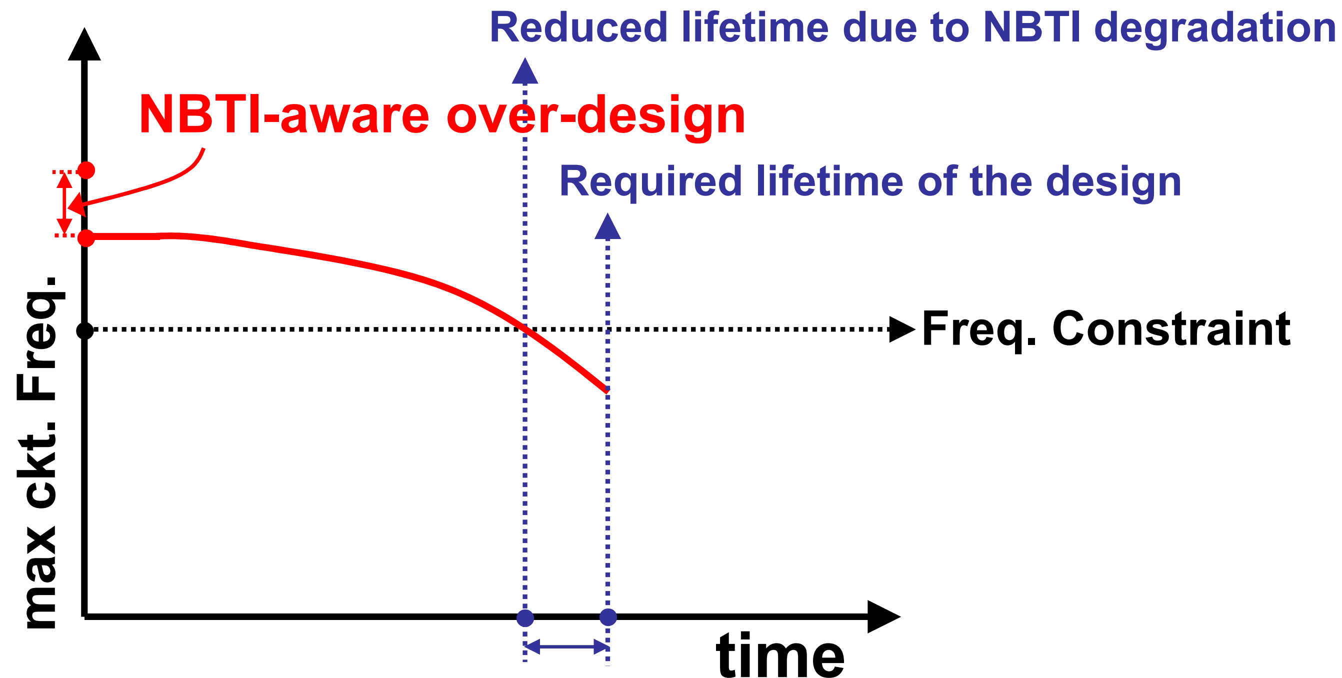
Logic Cell	fanin	Delay (ps)		Δ (%)
		t=0	3 years	
INV	1	13.77	16.77	21.81
NAND	2	16.86	19.88	17.93
NAND	3	19.57	22.45	14.75
NOR	2	17.26	21.89	26.79
NOR	3	23.80	30.19	26.87

**B. C. Paul et al., EDL'05*



- Delay computation for standard cells*
- NBTI aware Static Timing Analysis (STA)
- *n ~ 1/6* for circuit f_{MAX}

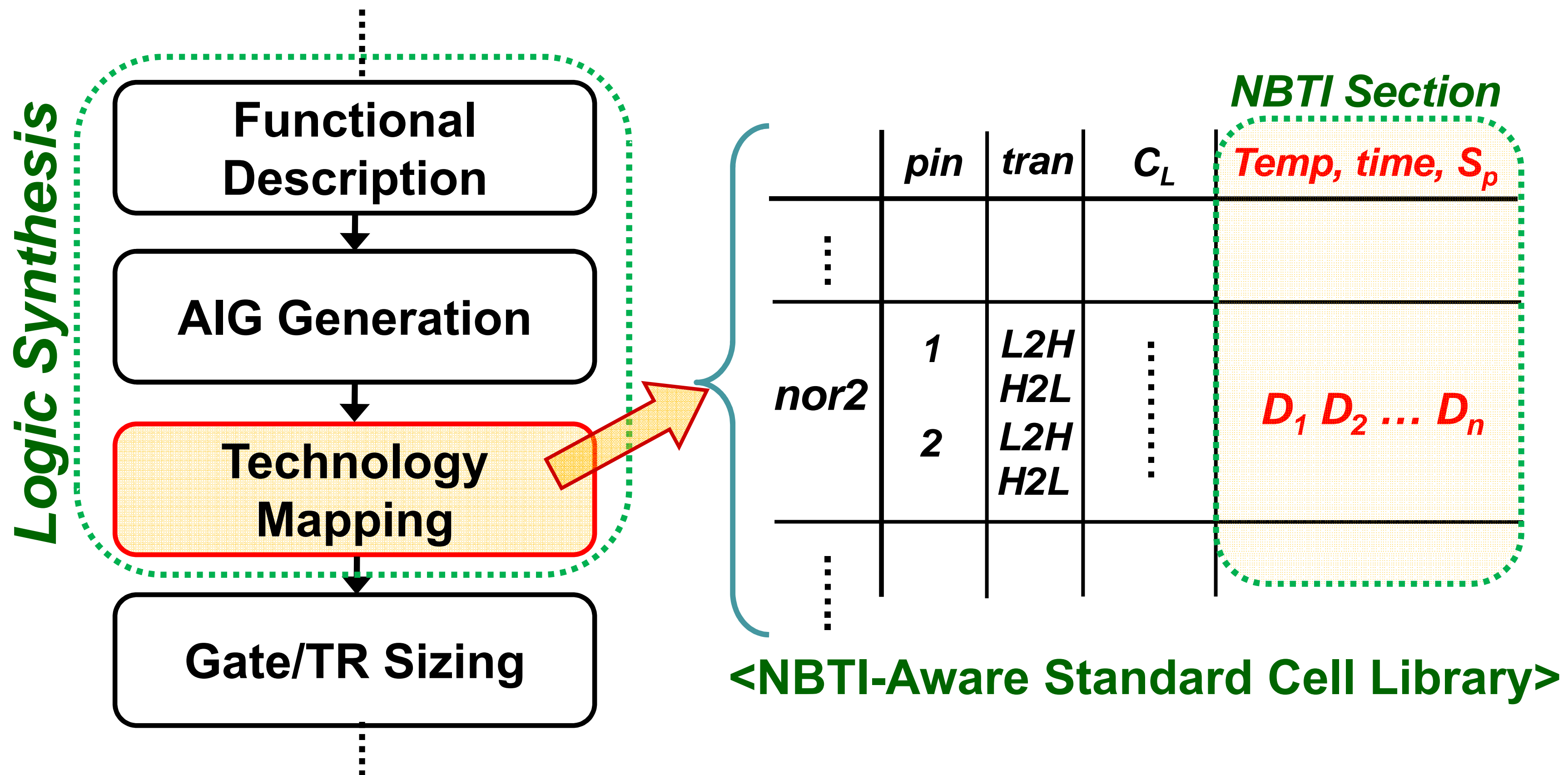
Solution #1: Optimal Sizing*



- **Calculated over-design is required to guarantee a lifetime stability of the circuit**
- **LR sizing is used to optimize the circuit**
  - **Size the circuit considering the worst-case V_t degradation over the lifetime**

**B. C. Paul et al., DATE'06*

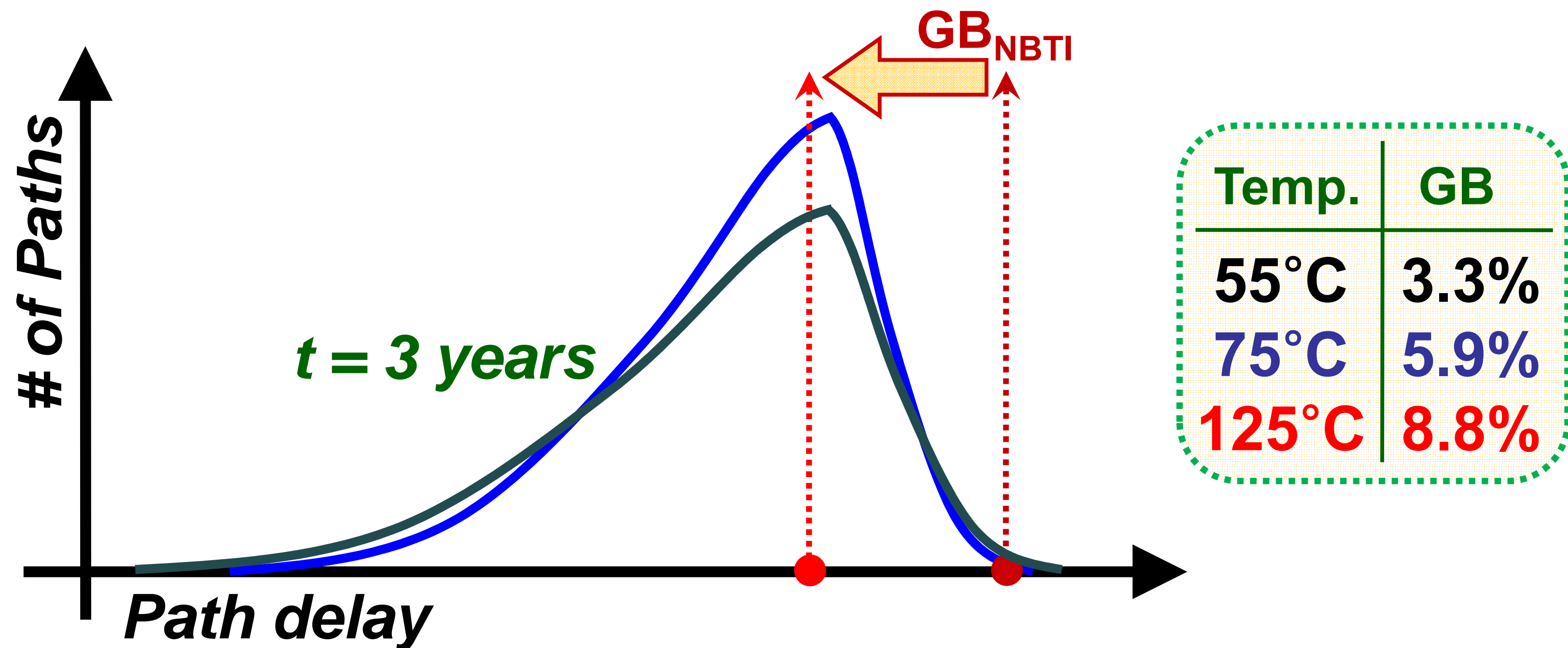
Solution #2: Technology Mapping*



- NBTI is considered during technology mapping
- Sensitivity of different gates w.r.t NBTI is considered

*S. Kumar et al., DAC'07

Solution #3: Delay Guard-Banding



- Simple delay guard-banding at initial design phase
- Low-cost, low-complexity, ignore NBTI sensitivity
- May not be an optimal solution

Comparison Result

*PTM 65nm, scaled LEDA library cells

Circuits	# of gates	Nominal Design (um)	Area overhead @125C				Area overhead @75C			
			WC-Sizing	Opt-Sizing	Guardbanding	Synthesis	WC-Sizing	Opt-Sizing	Guardbanding	Synthesis
c432	184	225.7	**8.59**	**6.13**	**7.98**	**4.25**	**5.35**	**4.03**	**4.57**	**1.14**
c1908	466	537.2	**13.79**	**9.17**	**10.21**	**10.38**	**7.62**	**5.72**	**5.70**	**4.40**
c499	534	567.7	**15.25**	**8.75**	**9.81**	**6.45**	**7.39**	**5.34**	**5.04**	**2.02**
c2670	686	801.5	**7.16**	**5.33**	**5.55**	**5.01**	**5.07**	**2.26**	**2.45**	**2.54**
c3540	1134	1392.7	**6.36**	**3.41**	**4.27**	**0.40**	**2.85**	**1.98**	**1.92**	**0.20**
Average			***10.23***	***6.56***	***7.56***	***5.30***	***5.66***	***3.87***	***3.94***	***2.06***

- **WC-sizing >> GB > Opt-sizing > Synthesis**
- **Result from GB is comparable to other methods**
- **In low temp., the difference gets even lower**
- ***GB can be an efficient yet effective solution***

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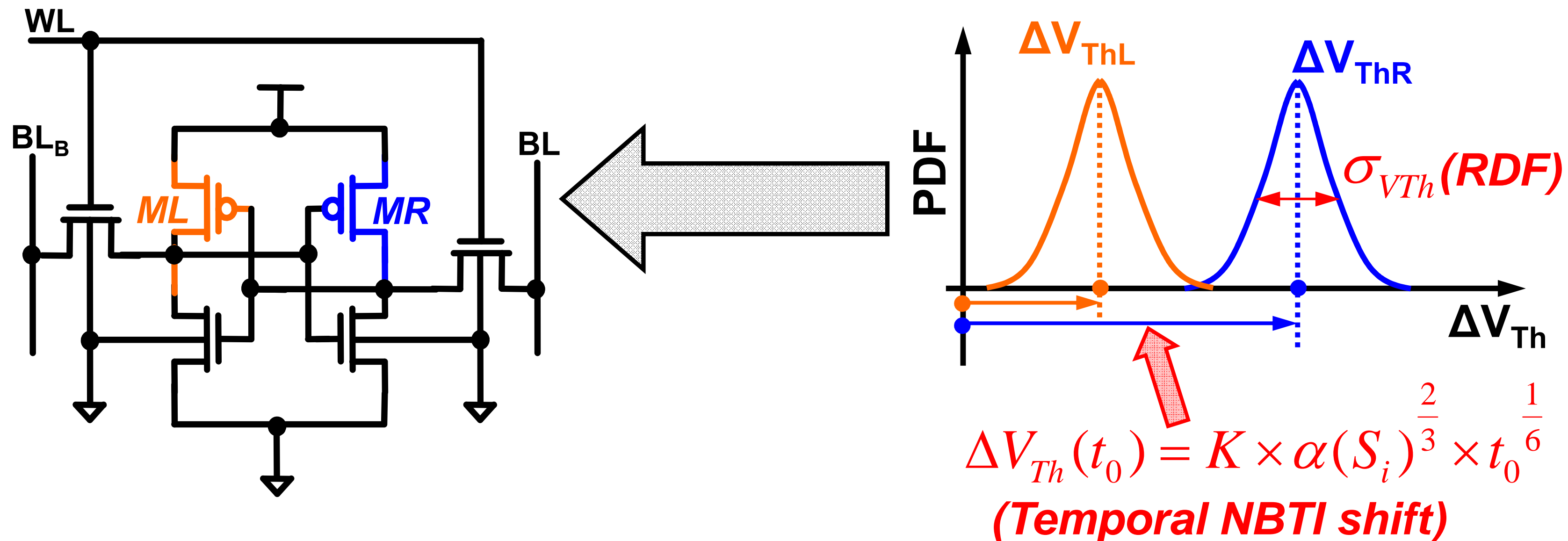
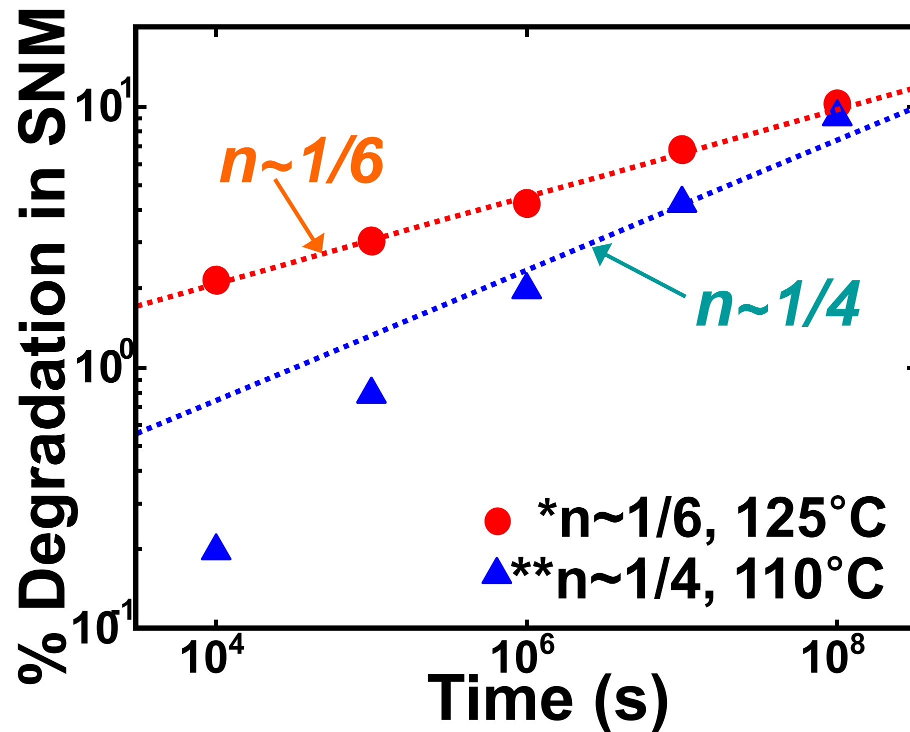
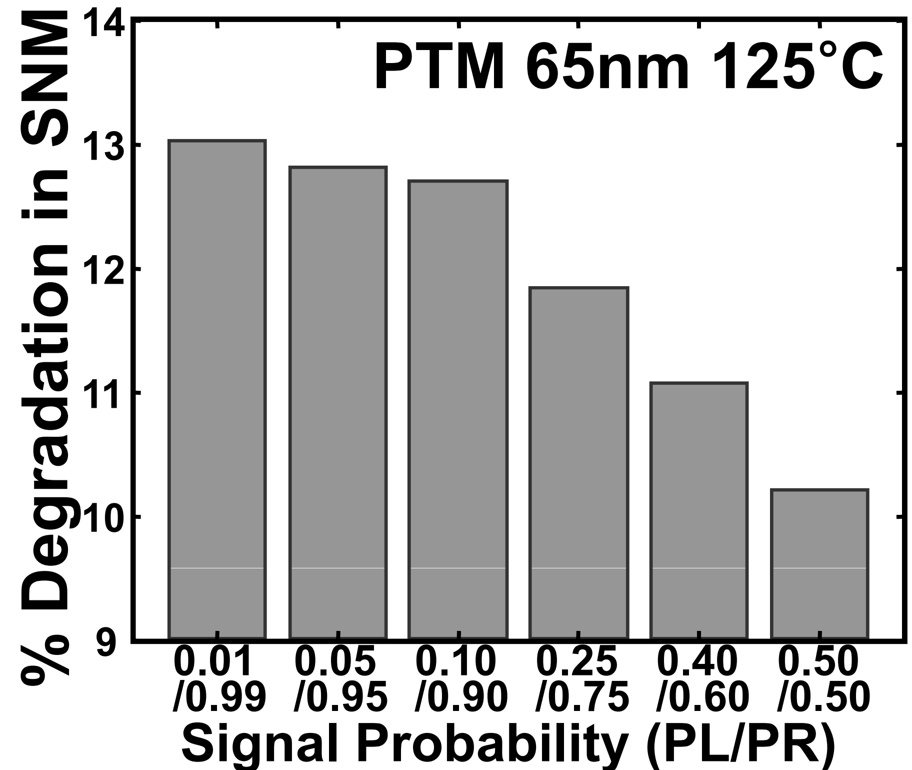
NBTI in Memory Arrays



- ***Mismatch between TRs*** **are critical in SRAM cell**
- **Two sources of mismatches**
  - **Spatial Source: Process Variation, RDF**
  - **Temporal Source: NBTI in PMOS TR**
- **SNM, read & write stability, parametric yield**

Degradation in Cell READ Stability





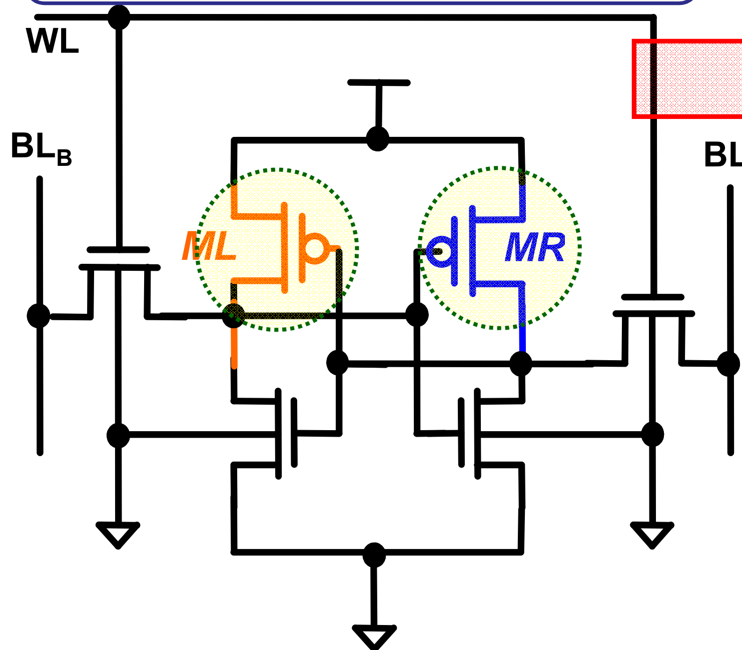
- **Static Noise Margin (SNM) reduces with time under NBTI**

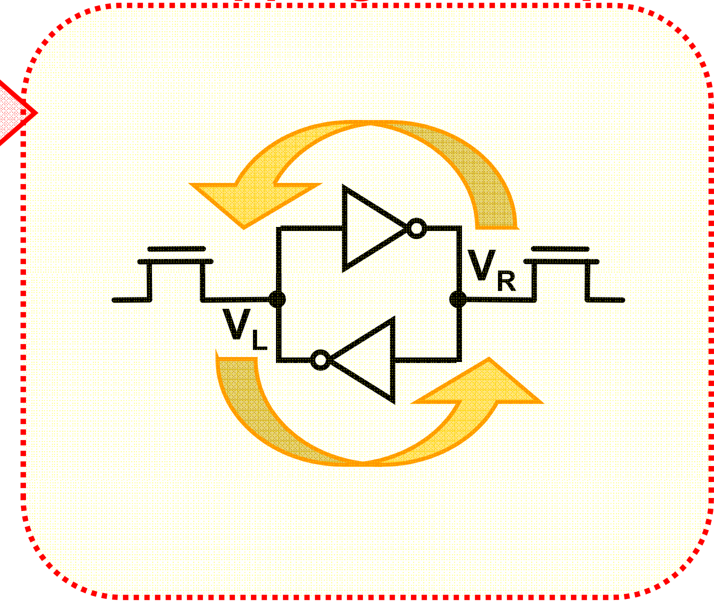
→ ~10% in 3 years static stress

- **NBTI becomes a critical issue in memory arrays**

**K. Kang et al., ITC'07, **S. Kumar et al., ISQED'06*

Solution #1: Periodic Cell-Flipping*



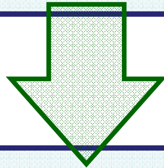


- Balance the signal probability on both side of the cell → $S_L = S_R$
- Still incurs close to **10% degradation in SNM**

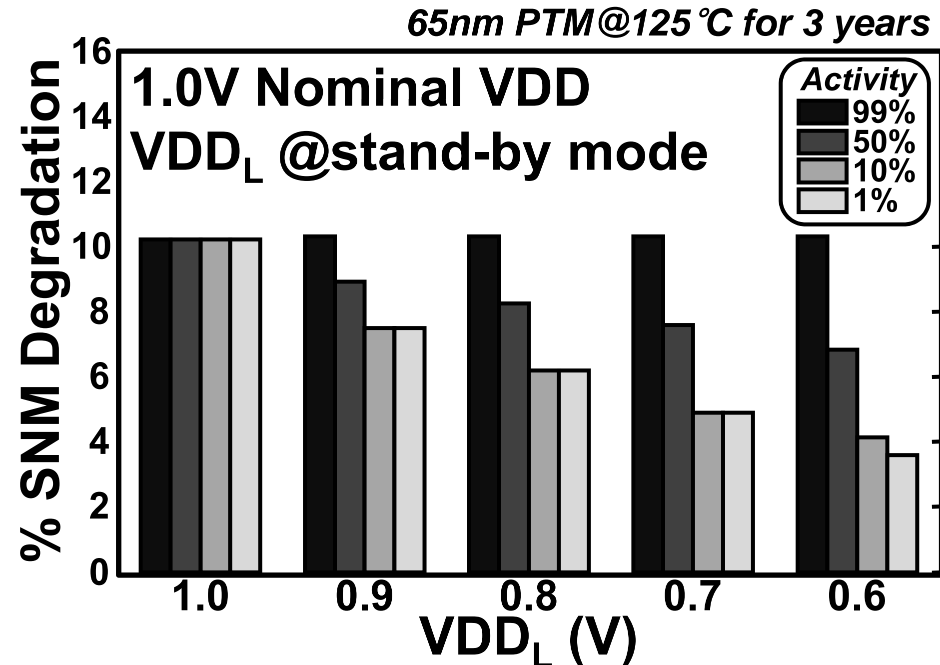
*S. Kumar et al., ISQED'06

Solution #2: Standby V_{DD} Scaling

- Normal Mode → VDD
- Standby Mode → VDD_L

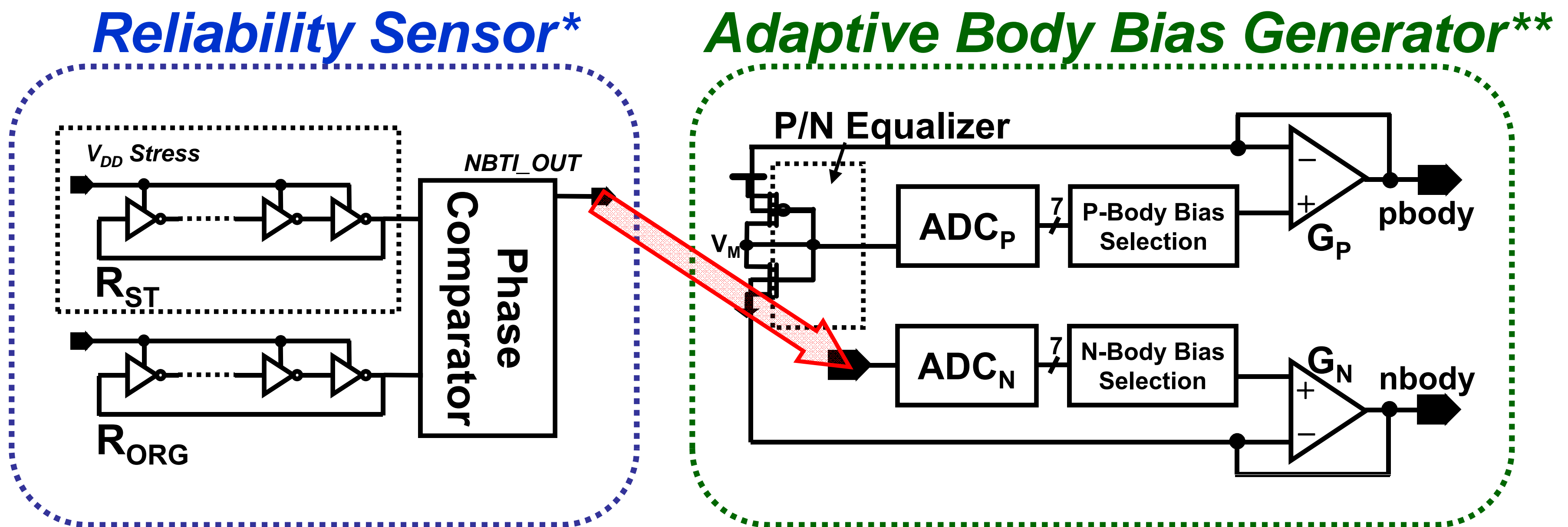


- Normal Mode → NBTI
- **Standby Mode → Min. NBTI**



- NBTI is a strong function of V_{DD}
- Lower V_{DD} during standby mode → MIN V_{DD}
- ***Effective solution with low design effort***

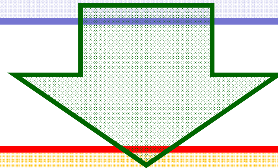
Solution #3: Sensing & Correction



- Sense reliability degradation → adaptive correction using circuit techniques
- *T. Kim et al., VLSI Circuit Symposium 2007
- ** K. Kang et al., Design Automation Conf. 2007
- ***Need to properly consider design overhead***

Future of NBTI

- Increasing T_{ox} scaling → E_{ox}↑
- High-k / metal gate transistor
- 3D device structure with increasing surface to volume ratio



NBTI will become an essential design issue in future technology generation

Conclusion

- **NBTI is an emerging Reliability issue in future MOSFET technologies**
- **NBTI can severely impact the lifetime of various digital circuits**
- **Effective & realistic design solution for random logic circuits and memory arrays are proposed**

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