# Experiences of Low Power Design Implementation and Verification

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2 Power Gating

Low Power Verification



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**Dynamic IR Prevention** 

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Conclusion

### **Technology is Driven to Low Power**

#### Force and Impact

- Application, cost, process technology driven
- Complexity, power density, leakage increase
- Trade-off: area, power, performance, reliability, cost, ...



### **Power Optimization**

#### Should be achieved from various fields

 Software, architecture, logical design, physical implementation, IP/library support, process technology, ...



### **Power Gating**

#### Off-chip control

- Take long time to wake-up

#### On-chip control

- Switch-able pad implementation needs extra I/O space
- Power switch implementation becomes more popular



### **MTCMOS Technique**

- The most effective way to manage leakage
  Penalty
  - Incurs power by sleep transistors and have area penalty
  - Has performance degradation issue due to IR drop
  - Needs extra de-cap to reduce the power noise



### **Power Switch Planning**

#### Determine switch allocation, power-up sequence

- Subject to: area, power, ramp-up time and peak current



### **Power Switch Assembly**

#### Partition/Cluster switch cells in banks

- Peak current limit (max concurrence)
- Wake-up time limit (max depth)



### **Effect of Power-up Sequence**





2,400 switch cells partitioned in 20 banks, and assembled in the same configuration (Domino Fashion)

4 root position: BL, BR, TL, TR

BL

TL

## **Power Switch Optimization**

### Sizing/Removal

#### Reordering

To reduce rush current and dynamic IR problems



### **Dynamic IR vs. Power-up Sequence**



### **Verification is a Key to Success**

#### Comprehensive low power verification

- Design quality check
- Electrical check, functional correctness, IR/EM analysis
- Dynamic IR





good decision? incomplete clock gating? missing isolation or shifter? incorrect power domain connection? power routing? incapable sleep control propagation? IR/EM analysis?

#### Enable Shifter

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### **Dynamic IR Drop Affects Yield**

#### Dynamic IR is critical at 90nm and below

- Timing variation becomes more voltage sensitive
- Increasing the power grid width is not efficient enough



It's not only speed degradation problem, but also cause chip failure !

### **Scan Mode Dynamic IR is Critical**

#### Even worst in scan mode

- Delay is more sensitive to IR drop as technology shrinking
- Simulation-based approach is effort consuming
- Analysis at early stage is critical

**Static Analysis** 



VDD: 0% ~ 0.75%



VDD: 17.5% ~ 18.7%

## **Dynamic IR Analysis**

#### Traditional flow is inefficient

- Effort consuming to grab VCD pattern and timing window
- No enough space around hot spots (too late)
- May worsen leakage and yield (inefficient de-cap insertion)





Gain ~1% dynamic IR saving, but pay ~200K de-cap cells.

### **Dynamic IR Failure Prediction**

#### Flip-flop density rule

- Cell padding is applied during CTS and timing opt.
- Dynamic-IR is controlled while maintaining timing
- De-cap cell insertion becomes more efficient



### **Dynamic IR Prevention Flow**

#### Preliminary planning

- Power grid
- De-cap pre-insertion
- Power switch configuration
- Prediction, fixing

#### Power aware DFT

- Clock gating
- Location-based grouping
- Test clocks varying
- Power switch opt.
  - Sizing, removal, reordering



### Conclusion

#### Power efficiency

- Compromise between different mechanisms
- Require good decision, comprehensive verification
- Power-gating is a promising leakage control
  - Challenge of verification among various sleep modes
  - Configuration with dynamic IR consideration
- Dynamic IR prevention flow improves yield
  - Flip-flop density check achieves a good quality
  - Fixing becomes much easier without timing degradation
  - Dynamic-IR is controlled during CTS and timing opt.

