ASP-DAC 2008

Low power architecture and design techniques for mobile handset LSI Medity™ M2

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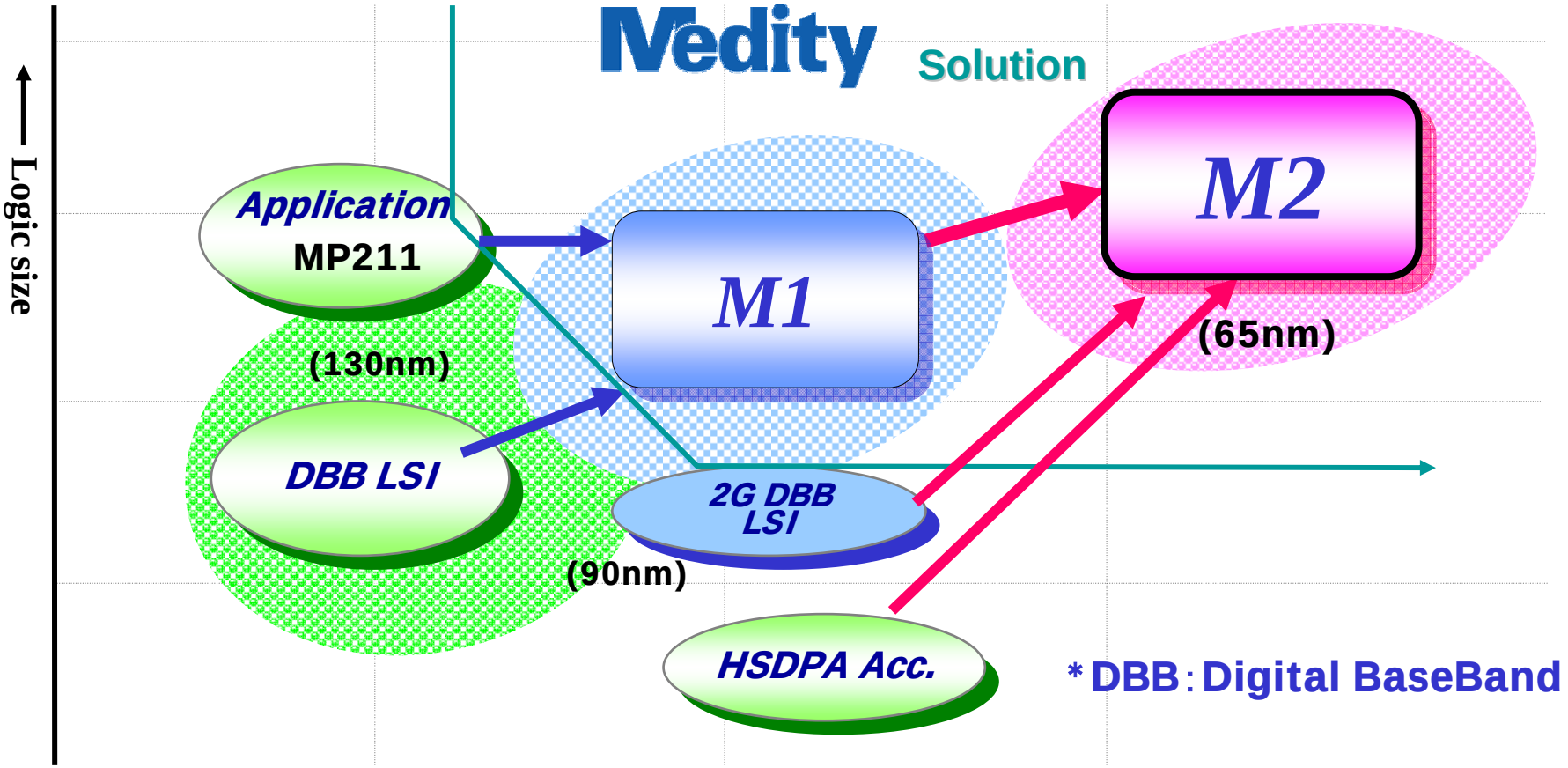
Outline

- Medity™ M2 overview
- Use case analysis and low power issues
  - ✓ heavy workload
  - ✓ light workload
  - ✓ standby mode
- Medity™ M2 low power techniques
  - ✓ Hierarchical clock gating
  - ✓ Automatic frequency control
  - ✓ Multiple Vt transistors and on-chip power switch
  - ✓ Back-bias control (UltimateLowPower™)
- Power measurement Results
- Summary and conclusions

Medity™ M2 Overview

- M2 is second-generation LSI for mobile handset which integrates DBB and Application processor on a chip



M1 and M2 comparisons

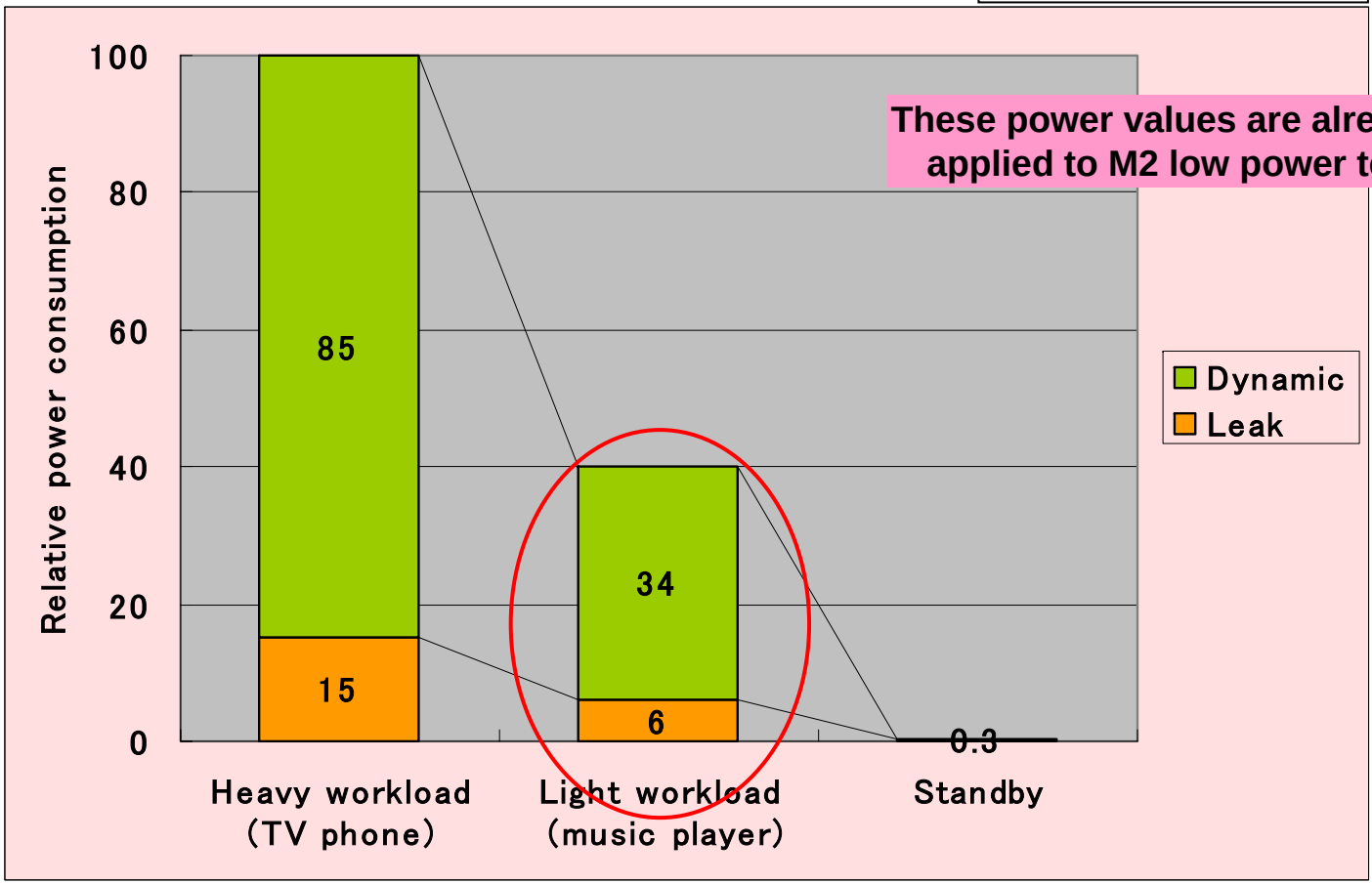
- M2 aims to be same power consumption as M1, although there are big differences between M1 and M2

	Function		M1	M2	M2/M1
DBB	Communication		W-CDMA	W-CDMA	—
			—	HSDPA(3.6Mbps)	new
			—	GSM/GPRS	new
Application	Frequency	CPU/DSP	250MHz (ARM9)	500MHz (ARM11)	2 times
		System Bus (3D graphics, image)	125MHz (AHB)	166MHz (AXI)	1.3 times
	Functions	LCD	QVGA+ 345×240	WVGA 854×480	5 times
		Motion codec H.264	QVGA+ Dec (DSP)	D1 Enc, Dec (Dedicated macro)	new
		3D sound	—	128 chords	new

Power consumptions in three use cases

- Heavy workload
- Light workload
- Standby mode

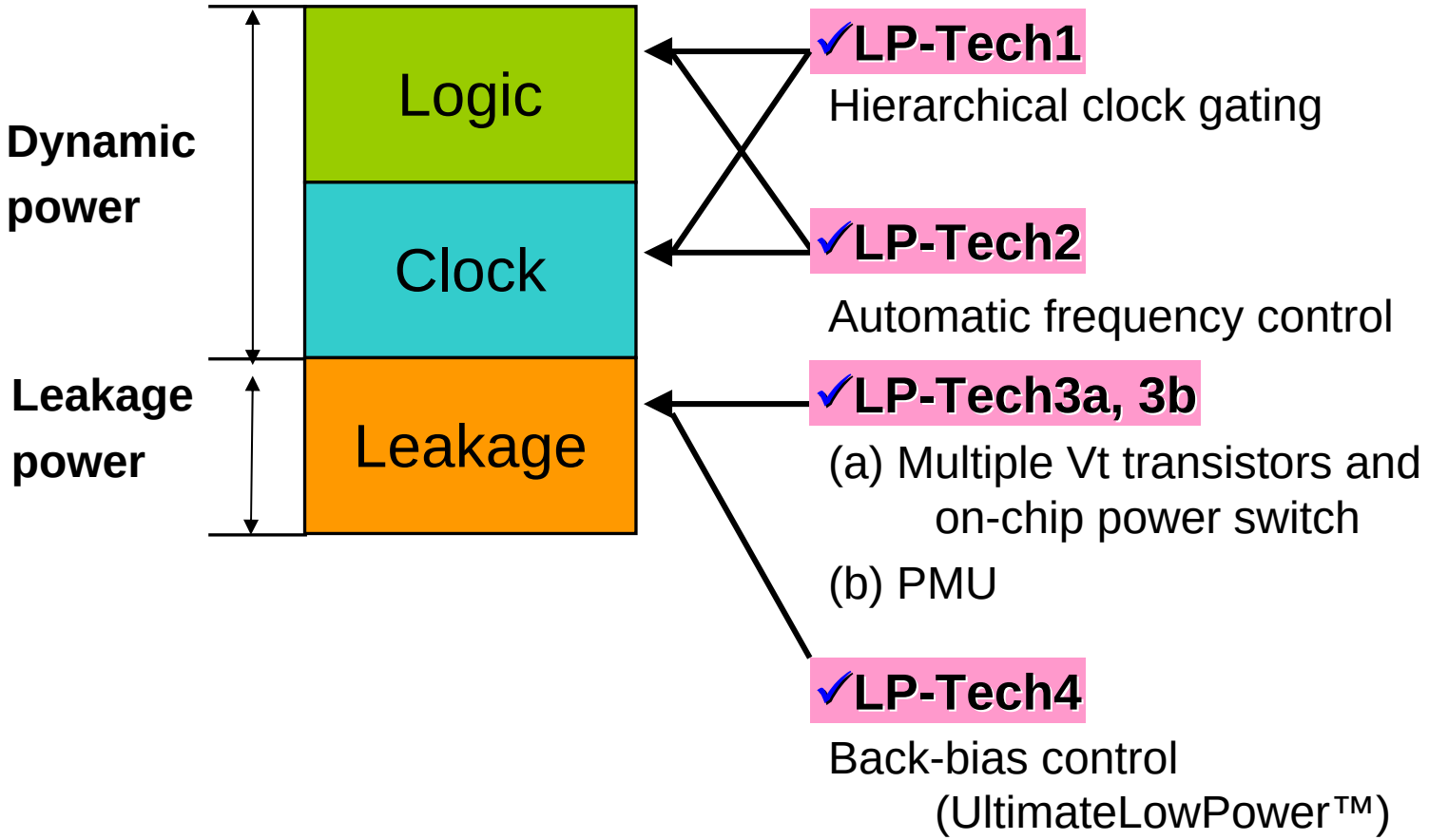
Typ, 1.2V@26C



These power values are already applied to M2 low power techniques

Medity M2 Low power techniques

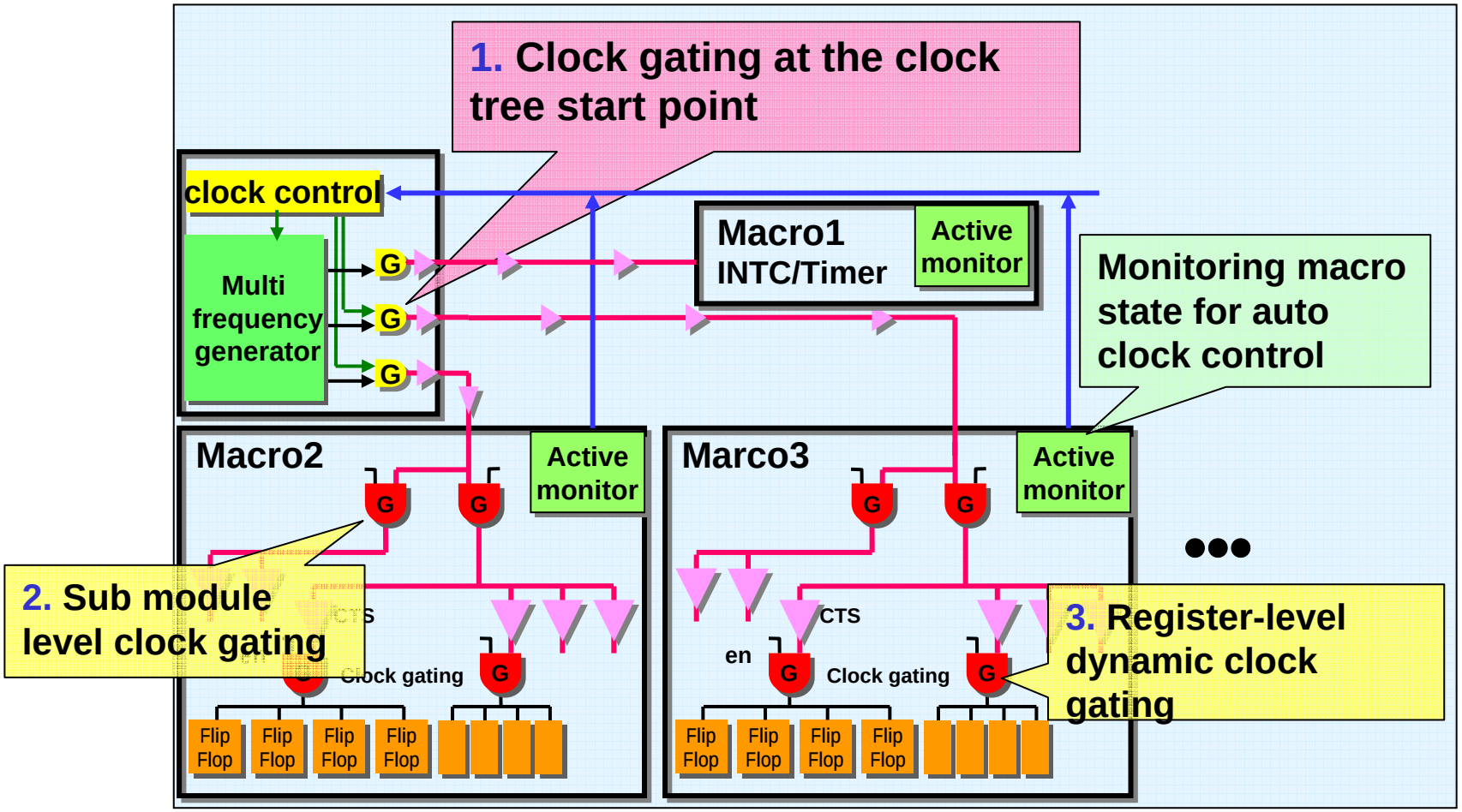
- M2 low power techniques are covered for reducing each element of the power



Hierarchical clock gating

- Reduce the dynamic power of unnecessary macros and clock tree at the clock starting point
  - Active monitor makes clock control condition

✓LP-Tech1

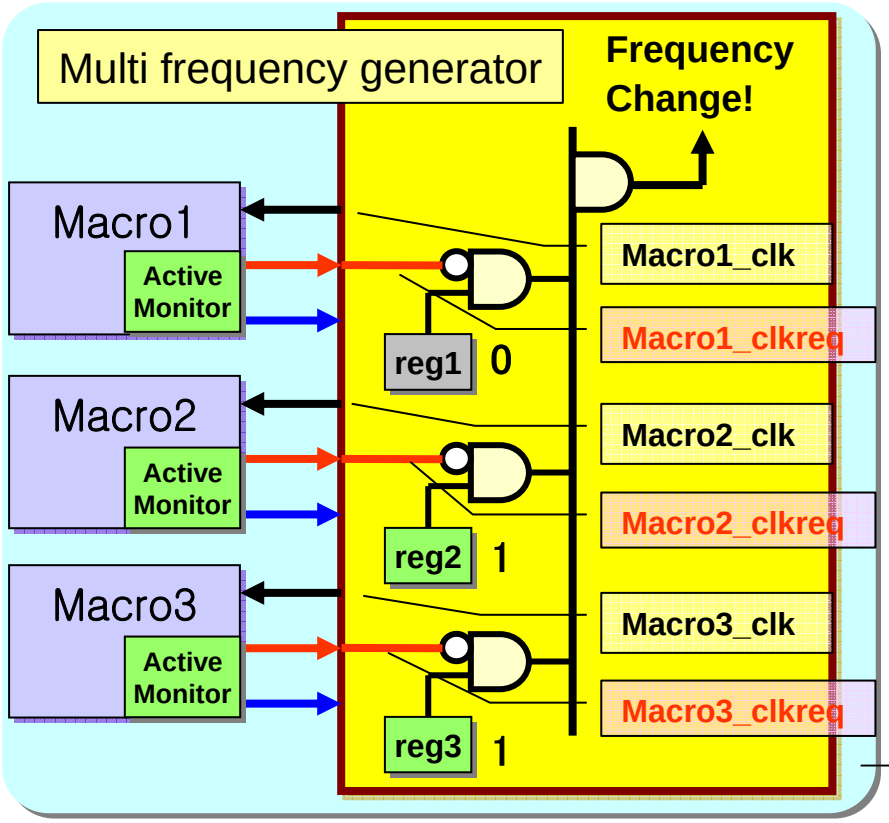


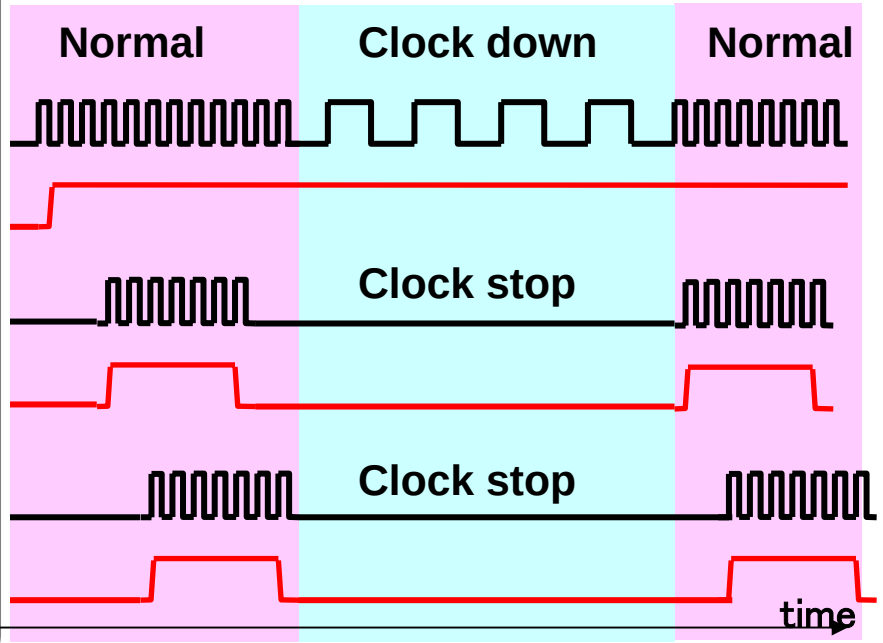
Automatic frequency control

- Reduce dynamic power of a unstoppable clock macro and system bus

  ✓LP-Tech2

  - ✓ Active monitor makes clock control condition for multi frequency generator

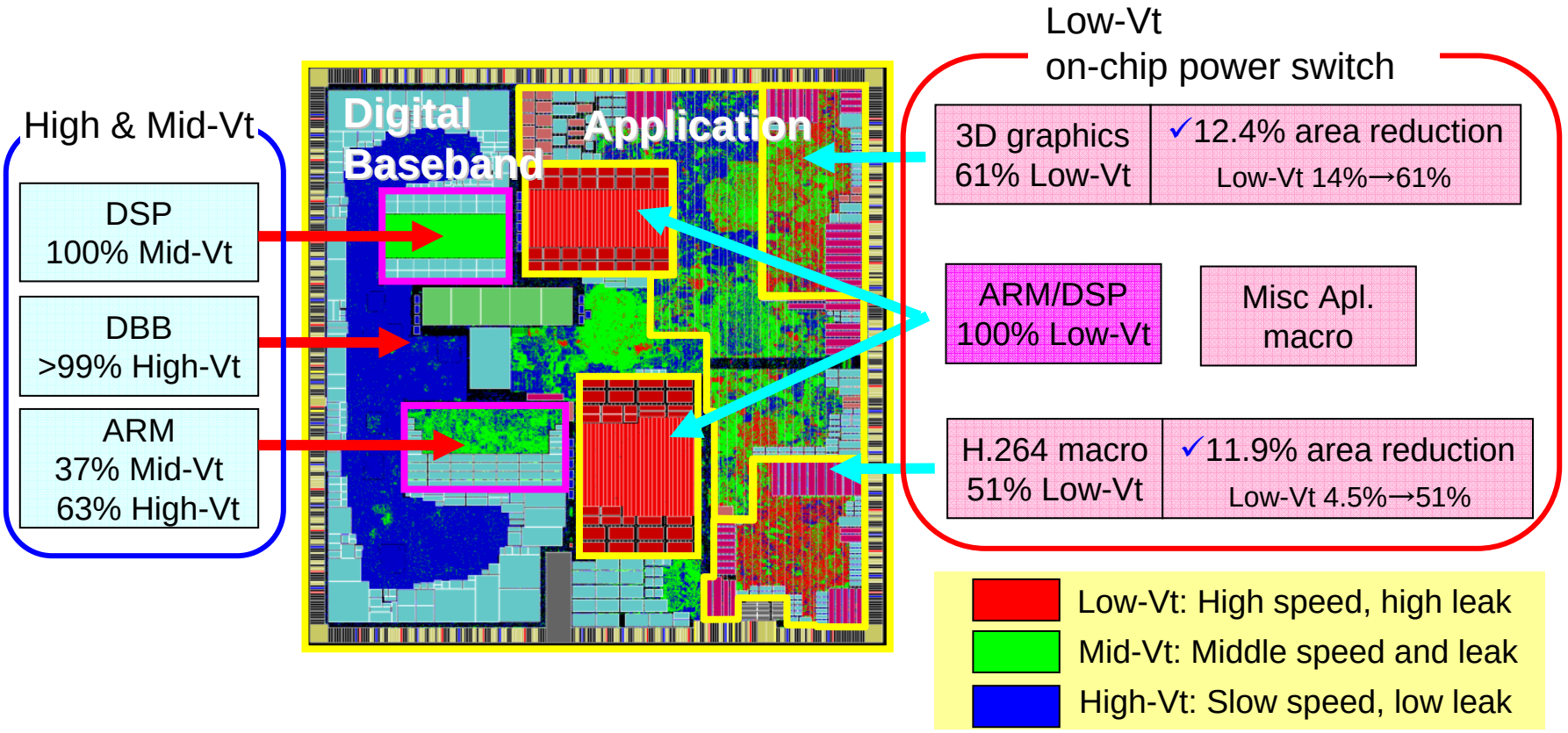




Multiple Vt Transistors & on-chip power switch

- Achieve target speed (Low-Vt)
- Reduce the area (Low-Vt)
- Reduce the leakage power (High-Vt & on-chip power switch)
- Reduce the external materials (on-chip power switch)

✓**LP-Tech3a**
✓**LP-Tech3b**

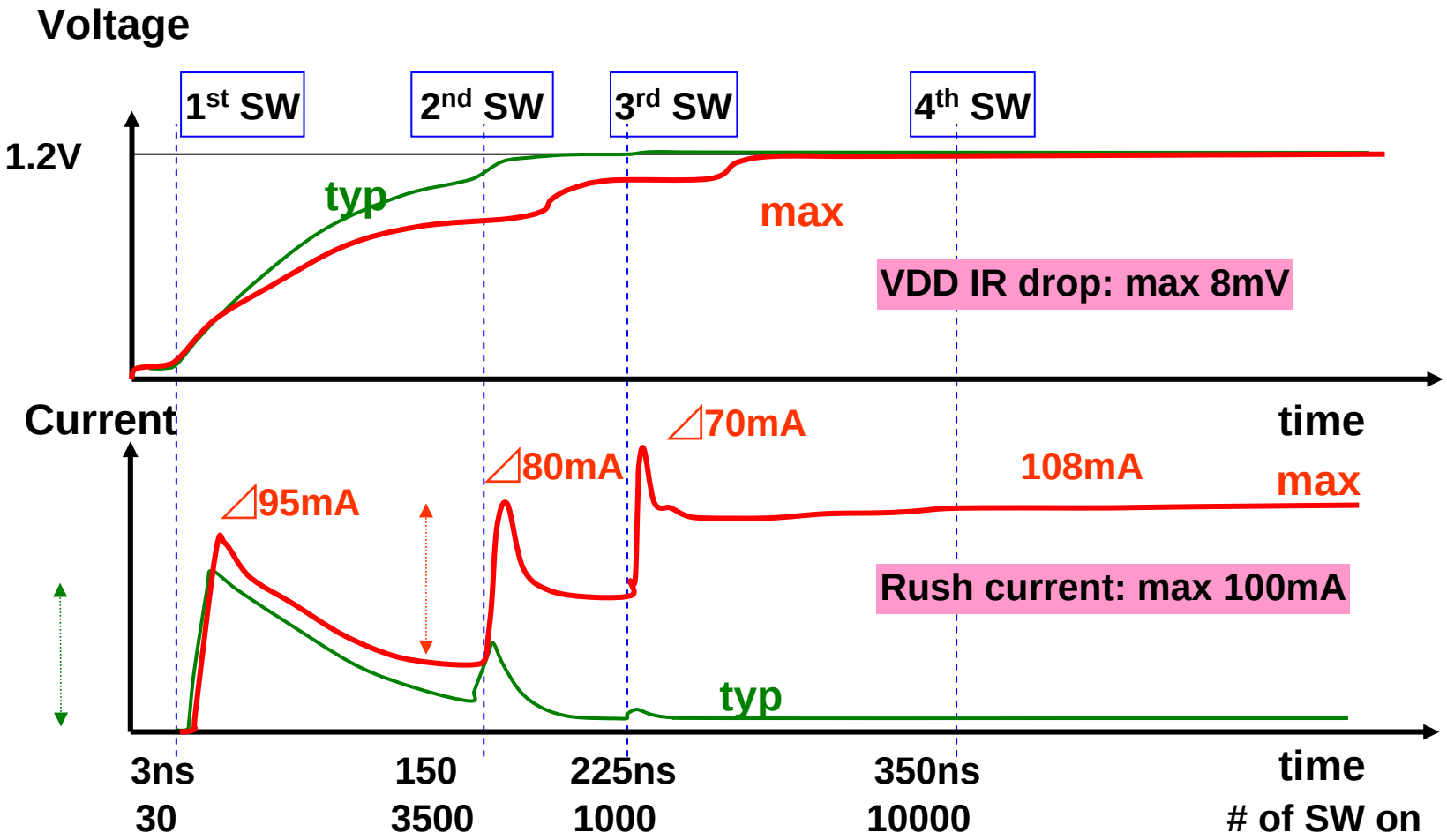


Power-on switching sequence

- Power-on switching sequential is divided 4

✓LP-Tech3a

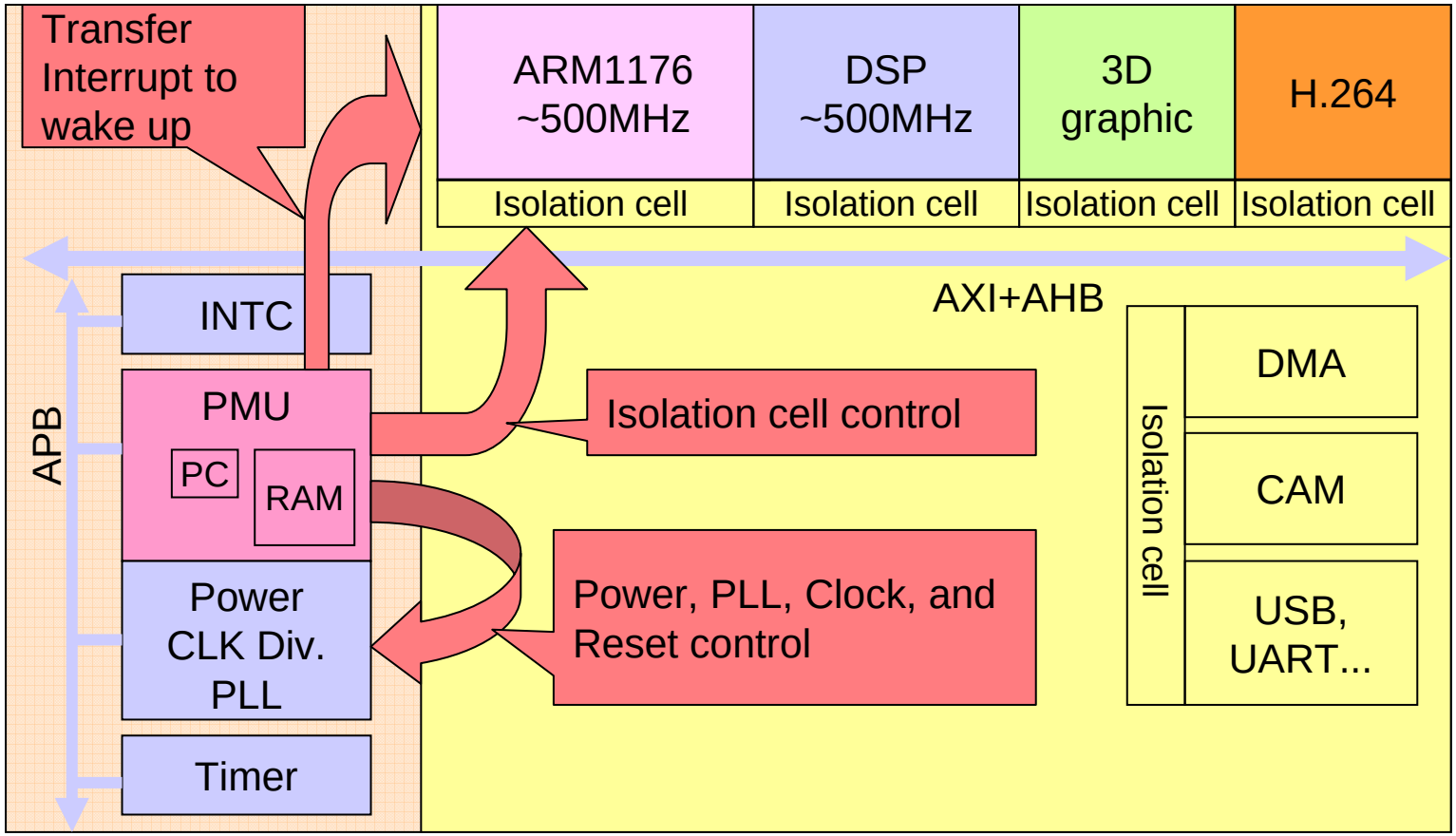
  - ✓ Preventing the rush current for IR Drop



Power Management Unit :PMU

- Could migrate to various power mode sequence flexibly and smoothly by PMU SW

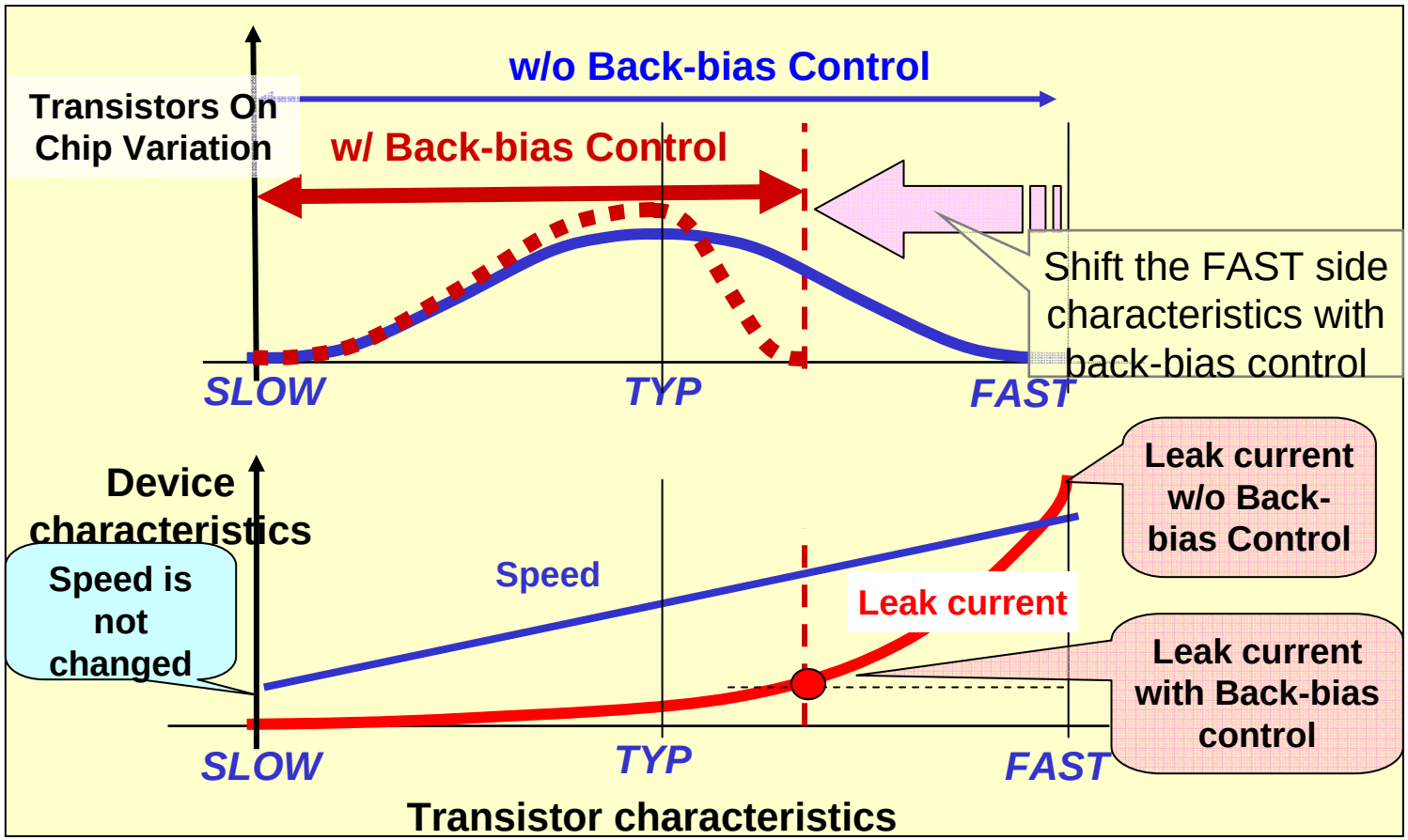
✓**LP-Tech3b**



UltimateLowPower™ (1)

✓LP-Tech4

- Reduces the leakage power using back-bias
- Improve the leakage yield to manage FAST side samples to be around TYP side samples, no effect to SLOW side samples

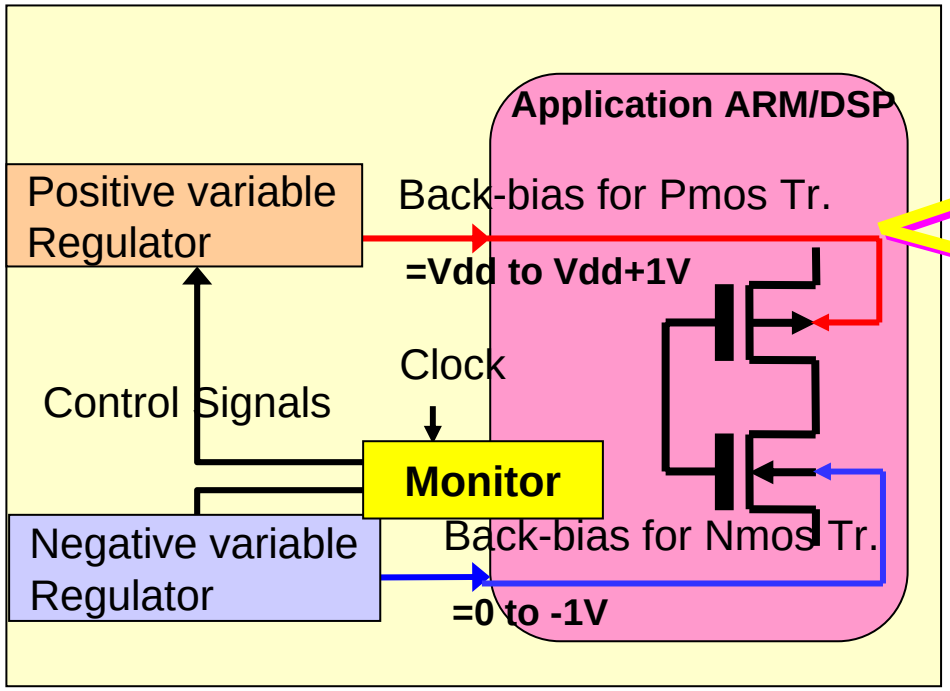


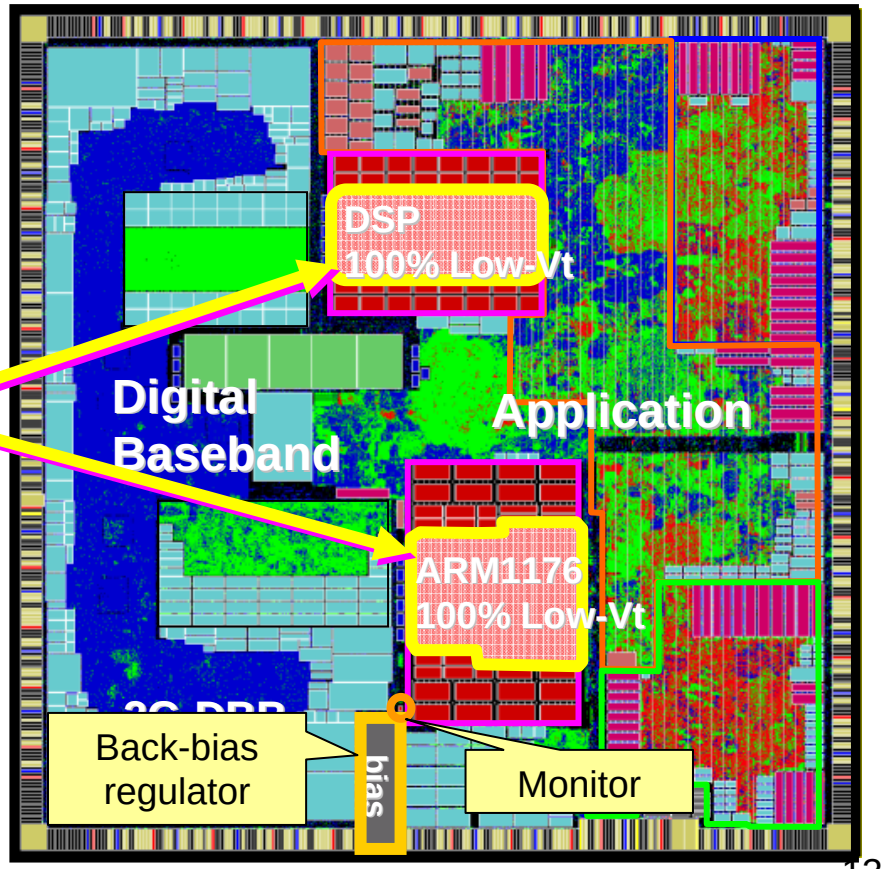
UltimateLowPower™ (2)

- Apply to application ARM/DSP macros

✓LP-Tech4

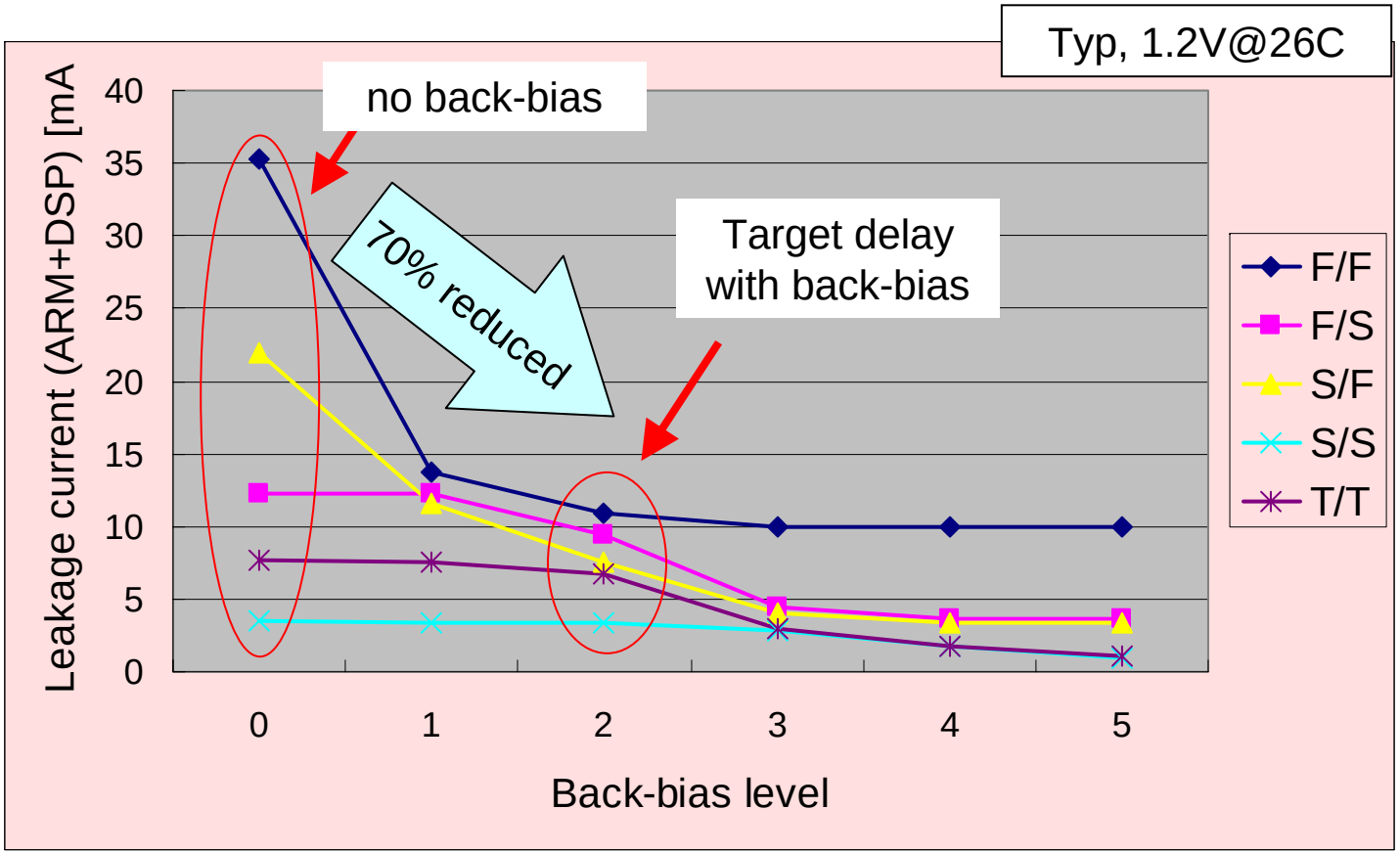
  - ✓ Use 100% optimized Low-Vt which more sensitive for leakage current with respect to back-bias voltage
  - ✓ Multi-Vt in same region is not suited for UltimateLowPower





Leakage current with back-bias

- The Leakage current of Fast sample (F/F) is 70% reduced
  - ✓ the characteristics of Slow (S/S) samples are not changed ✓**LP-Tech4**



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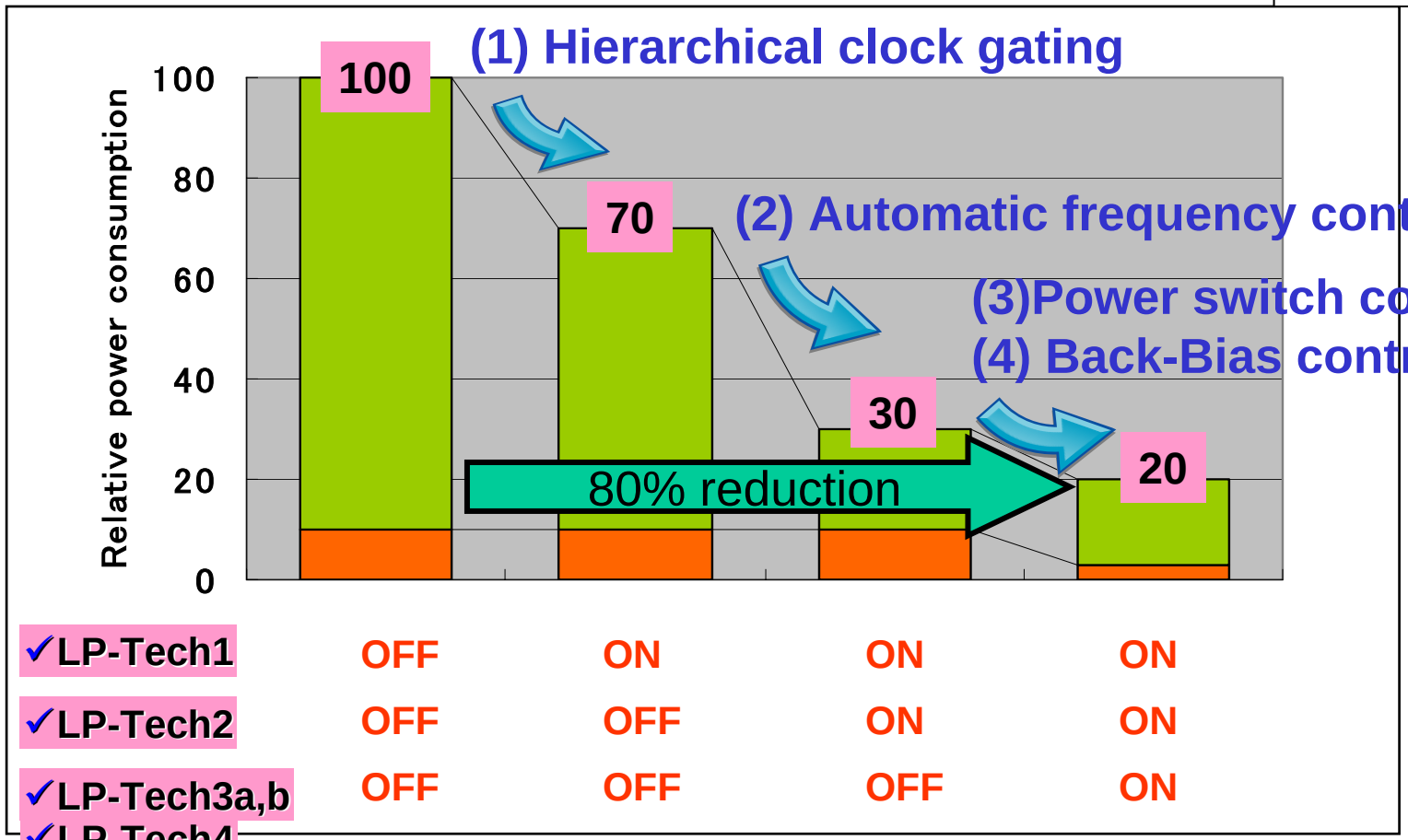
Power consumptions in light workload

- 80% power reduction is achieved
- Music player (AAC) with WVGA displaying

Typ,
1.2V@26C



Power Consumption results

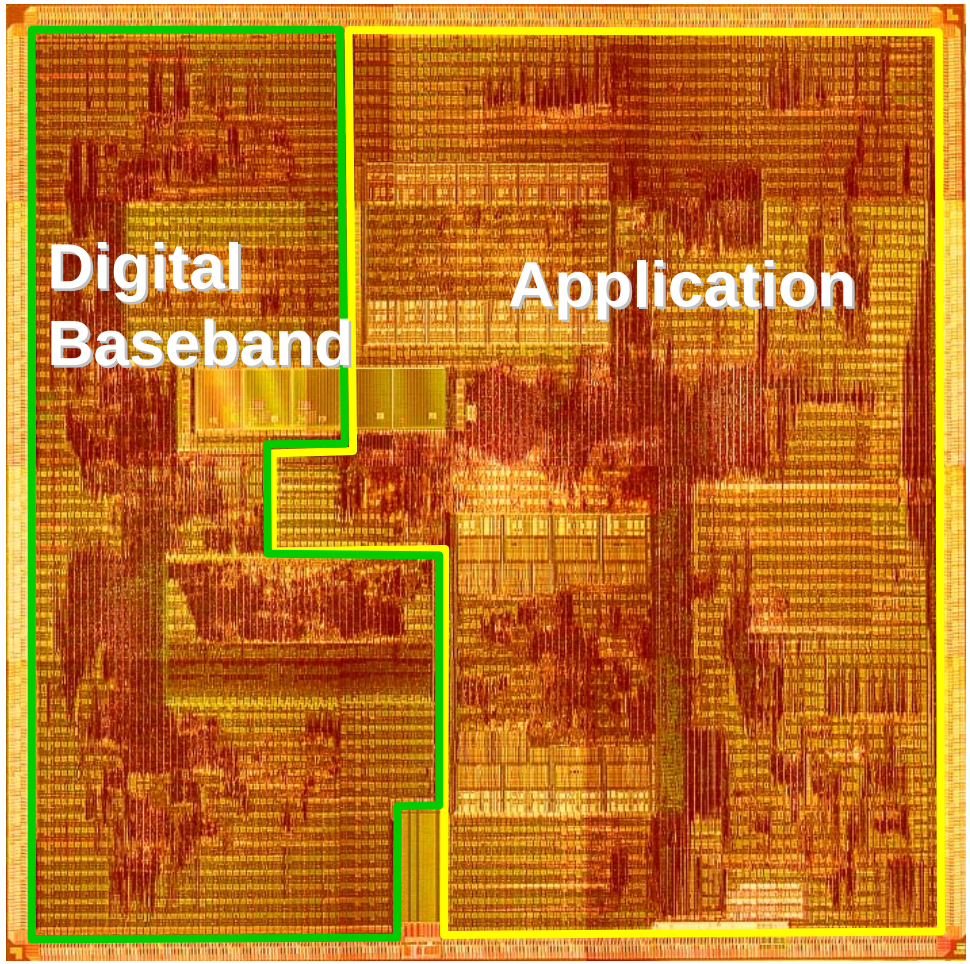
- Low power consumption is achieved in heavy and light workload

✓**LP-Tech1**
✓**LP-Tech2**
✓**LP-Tech3a, 3b**
✓**LP-Tech4**

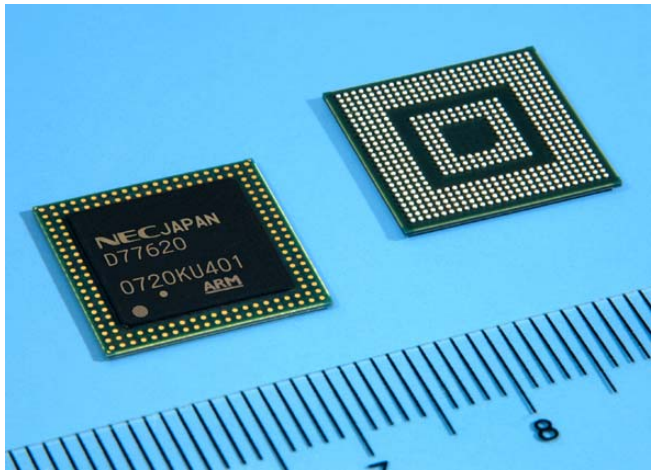
Application	typ, 1.2V@26C (w/o I/O)
VGA still image displaying	5.2mA
Audio dec. (Enhanced AAC+, 48Kbps)	23.8mA
Video dec. (H.264, QVGA, 30fps)	22.3mA
Video dec. (H.264, D1, 30fps)	66.5mA

M2 die Photo

- Logic 15Mgate, SRAM 12Mbit
- 8.52x8.52mm@65nm



- FPBGA PKG
  - ✓ 529pin
  - ✓ 14x14mm□



M2 Products Photo

NTT DoCoMo
N905i μ

NTT DoCoMo
N905i

Summary and Conclusions

- Achieve 80% power reduction in light workload
  - ✓ Hierarchical clock gating and automatic frequency control by HW
  - ✓ Muti-Vt transistor and on-chip power switch which is controlled by PMU
  - ✓ Back-bias by UltimateLowPower
- Expectation for EDA tools
  - ✓ Maturity and stability
  - ✓ Reducing performance variation
  - ✓ Enhancing automatic optimization
- To realize truly ultimated low power,
  - ✓ Study the elements of power consumption in use cases
  - ✓ Apply the knowledge to the design from front-end to back-end phase