Best Ways to use Billions of Devices on a Wireless Mobile SoC

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Kyung-Ho Kim, Vice President
Telecommunication R&D Center,
Telecommunication Network Business,
Samsung Electronics Co., LTD.

Wireless Mobile SoC Trends

- The state-of-the art SoC for Wireless Handheld Devices

Samsung's SPH-P9200

Samsung's Armani Phone

Samsung's P2

One-Chip Integration (SoC/SiP)

• Application Processor

- Ever-increasing performance (over 1GHz)
- Diverse applications: VoIP, Video, Audio, Graphics, Game, Navigation, Web-browse, Email
- Multiprocessors: MPCore CPUs + Graphic Processors

• Samsung's mDirac / SAVm Processors
• Marvell PXA / TI's OMAP3

• Baseband Processor

- Ever-increasing communication data-rate (over 100Mbps)
- Diverse Standards: 2G/3G/WMAN/WLAN/WPAN/MobileTV
- Multiprocessors: CPU + DSPs
- One-Chip RF Integration

• Samsung's 802.16e / Marvell's 802.11n

Requirements of Wireless Mobile SoC

- Wireless application has different requirements than other computer or embedded applications.
  - Higher Clock Speed does NOT guarantee the Higher Air Throughput.
  - Integration density is not so high as computer application SoCs.
    because Ultra-Low-Power/Heat/form-factor design is more important.
  - Inter-Operability Test may take the most time of chip development.
  - Communication Protocol SW development is larger scale and costly.

	Computer SoC	Embedded SoC	Wireless Mobile SoC
Speed	Very High	High ~ Medium	Medium
Density	Very High	High ~ Medium	Medium
Power	Very High	High ~ Low	Very Low

Engineering Issues for Baseband Processor

1. System-level Low-power design

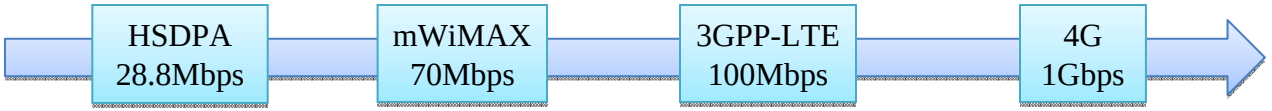
- Performance is ever-increasing but battery is never sufficient.
- Top-down low-power design is needed from system-level to physical-level

2. Programmability and Reconfigurable design

- Multi-standard support on a single chip
- Early development before the standard fixed
- Flexible Repair and debugging without silicon re-spin!

3. Higher-speed Wireless Signal Processing

- ASIC+DSP design for PHY processing, CPU for protocol processing
- Seamless Data Flow via RF → **BP** → **Host (AP)** → Storage or Display



4. System Integration

- SoP / Embedded PCB Integration of AP+BP or BP+RFIC

SoP : System on Package

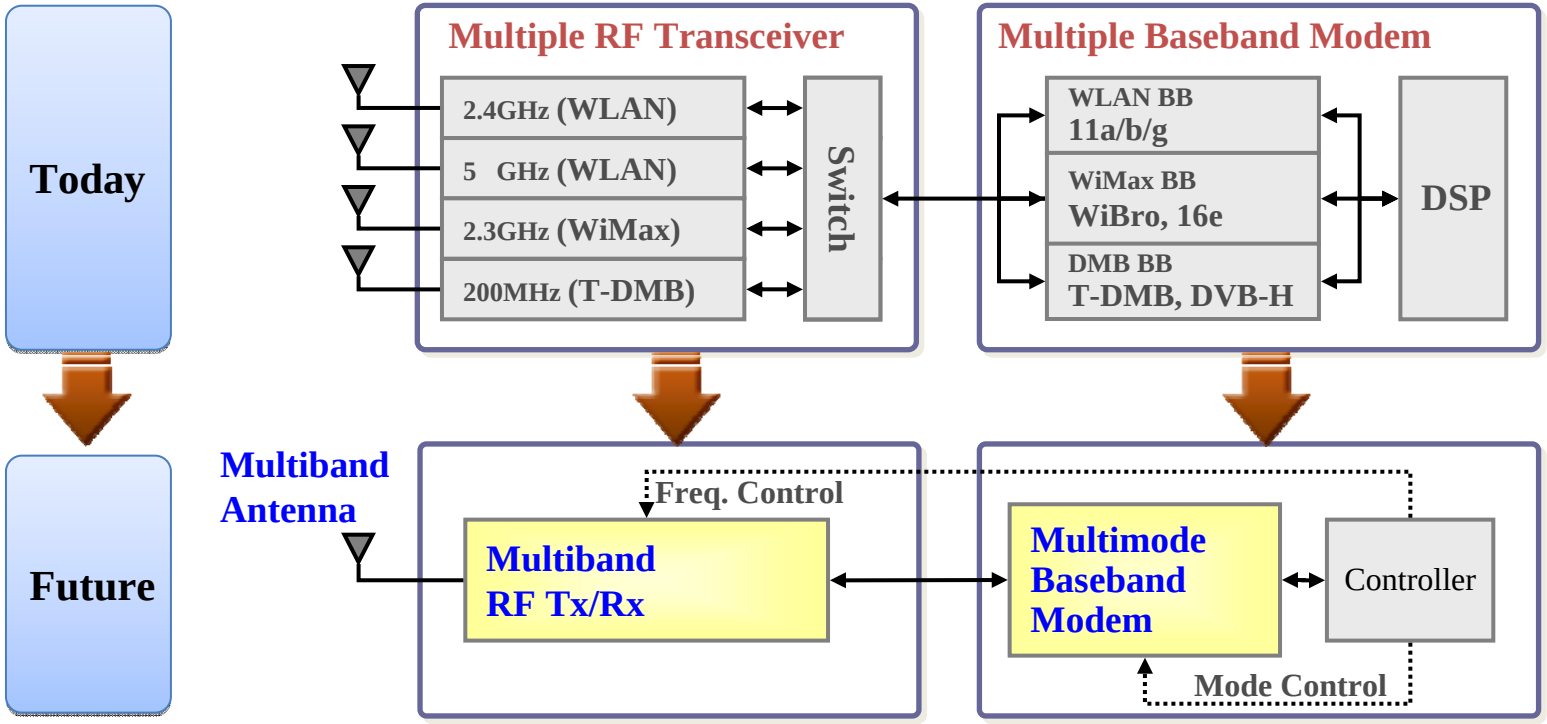
Low-Power Issue for Handsets

		Smart Phone		Ultra Mobile PC		Laptop PC
						
Battery [mAh]		**720 ~ 1200**	x ½	1800~ 2600	x ½	2400~5200
Application Performance	Video	MPEG 2/4 @ 3” + TV-out		MPEG 2/4 @ 7” LCD		HD-DVD/Blue-ray
	Audio	MP3		MP3		MP3/CD
	Comm.	GSM/ WCDMA/ HSDPA + WLAN / mWiMAX		Ethernet + WLAN / mWiMAX		Ethernet + WLAN / mWiMAX

- Many high-end computer applications are running on Smart-Phones.
- Baseband Processing and RF needs more power which always comes with Heat!
  (e.g., MIMO tech.→ Multiple Antennas → Multiple Power Amplifiers)
- Aggressive Low-Power Techniques are being used and will be used in BP.
  - Dynamic Power Reduction: Clock Gating, Dynamic Voltage Freq. Scaling, → Adaptive Voltage Scaling
  - Leakage Power Reduction: Multi-V_{th} Cell, Power Gating, → Sleep Tr., Body-Bias Control
- System-level Low-Power design is more crucial
  - Algorithm: **Power-aware Protocol Standard**
  - Architecture: Low-Power Modem H/W architecture (Less Buffer, Lower Frequency, Modular design)
    Parallel Processing lowers the frequency and voltage.

Reconfigurability Issue for Handsets

- Existing Mobile Chip contains Multiple RF Transceivers / Baseband Modems
- **Multiband RF, Multimode Modem**
  → Provides Multiple Telecom. Mode on a single architecture
  - Multiband RF Transceiver: Variable Frequency Tunable RF structure
  - Multimode Baseband Modem : Reconfigurable structure according to Telecom. Mode



Best Way to use Billions of Devices on a Wireless SoC

Requesting to EDA, Fabrication, IP Industrials and Academia

"Wireless Terminal Manufacturers are facing more urgent challenges than increasing the chip density and its clock speed!"

1. Ultra Low-Power Design Technology
   - Need to **Reduce Power Consumption to a Tenth** !
     - *Completely New* System, Architecture, Circuit and Process technology
   - **IP** Provider should support aggressive **Low-Power Mode and Features**.
     - ex) Sleep-mode support when it is idle, Data-driven clock gating
   - Highly Scalable and **Parallel Architecture** is preferable.

2. Reconfigurable Technology
   - Highly Scalable & Flexible **Multicore/Multithread DSP** architecture
   - Ultra low-power & less-area **embedded FPGA** and its compiler support
   - Various Multimode-supporting IPs for Wireless Modem

GALS: Globally Asynchronous Locally Synchronous