Quo Vadis, BTSoC*?

**BTSoC = Billion Transistor SoC*

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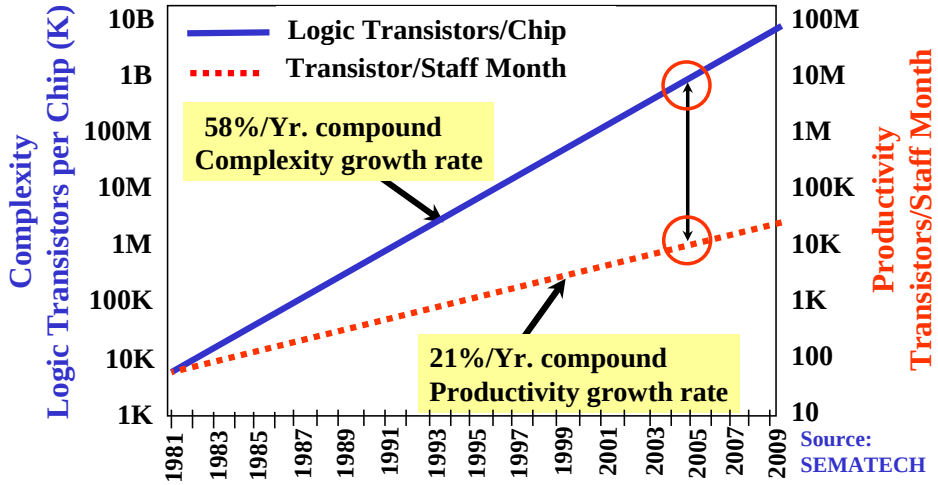
BTSoC Challenges

- Designer Productivity Gap
  - How to quickly design BTSoCs?



- BTSoC = **B**arbecued **T**ransistor**S** **o**n **C**hip?
  - Temperature, Power and Reliability:
    - **first-class concerns!**

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Best Ways to Proceed? (1/2)

- Rethink MPSoC: Multi-***PLATFORM*** Systems-on-Chip
  - Configure + execute
  - "Processors as gates" model
  - Recoup MPSoC development cost over a larger range of applications/volume

- Focus on ***Error-Aware*** Design
  - Errors *will* happen, how to deal with it?
  - Tradeoff quality for errors
  - Exploit redundancy at ***multiple*** levels
    - SW, Platform, Processor, RT,….
  - Aggressive use of on-chip memory for fault tolerance

Best Ways to Proceed? (2/2)

- **"Do Less with more"**
  - Use simple building blocks
    - **Eases composition, hierarchy**
    - **Enables robust validation/verification**
    - **Scalability, and de-activation (lowering energy)**
  - Focus on communication-centric & interface-based design
    - **Simpler blocks ease integration**
    - **Holisitic use of hybrid interconnect technologies**
      - **E.g., bus-based, NoC, emerging optical links etc.**
  - Simplify Thermal, Power and Reliability (TPR) management
    - **Easier control of simpler building blocks**
    - **Compositional strategies for TPR management**

Worst Ways to Proceed?

Worst way: Business as usual

- "Do More with Less"
  - Blindly add more "processors"
    - **Where's the parallelism? How to express/extract/harness it?**
  - Blindly add more "memory"
    - **Quality, not quantity!**
      - ***Customize memory according to needs: traffic patterns, access modalities, etc.***
- Worry only about specific constraints
  - E.g., focus on power minimization
    - **Need holisitic treatment of multiple constraints simultaneously**
      - **Including temperature, reliability, performance, energy, etc.**

Thank you!

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