The Future of Semiconductor Industry – A Foundry's Perspective –

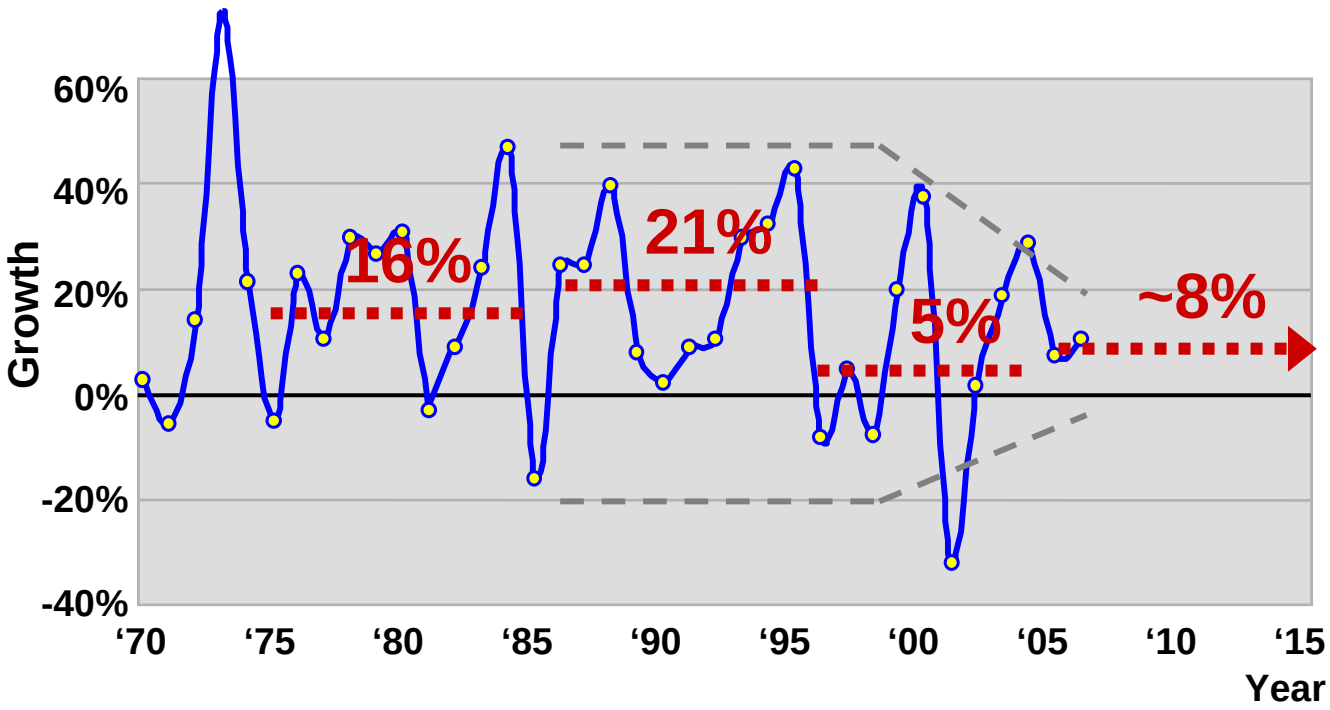
Dr. F.C. Tseng
Vice Chairman
TSMC

January 24, 2008

Outline

- Semiconductor Market Outlook
- Challenges and Solutions
  - Economic
  - Technology
- Summary

Semiconductor Market Will Continue to Grow

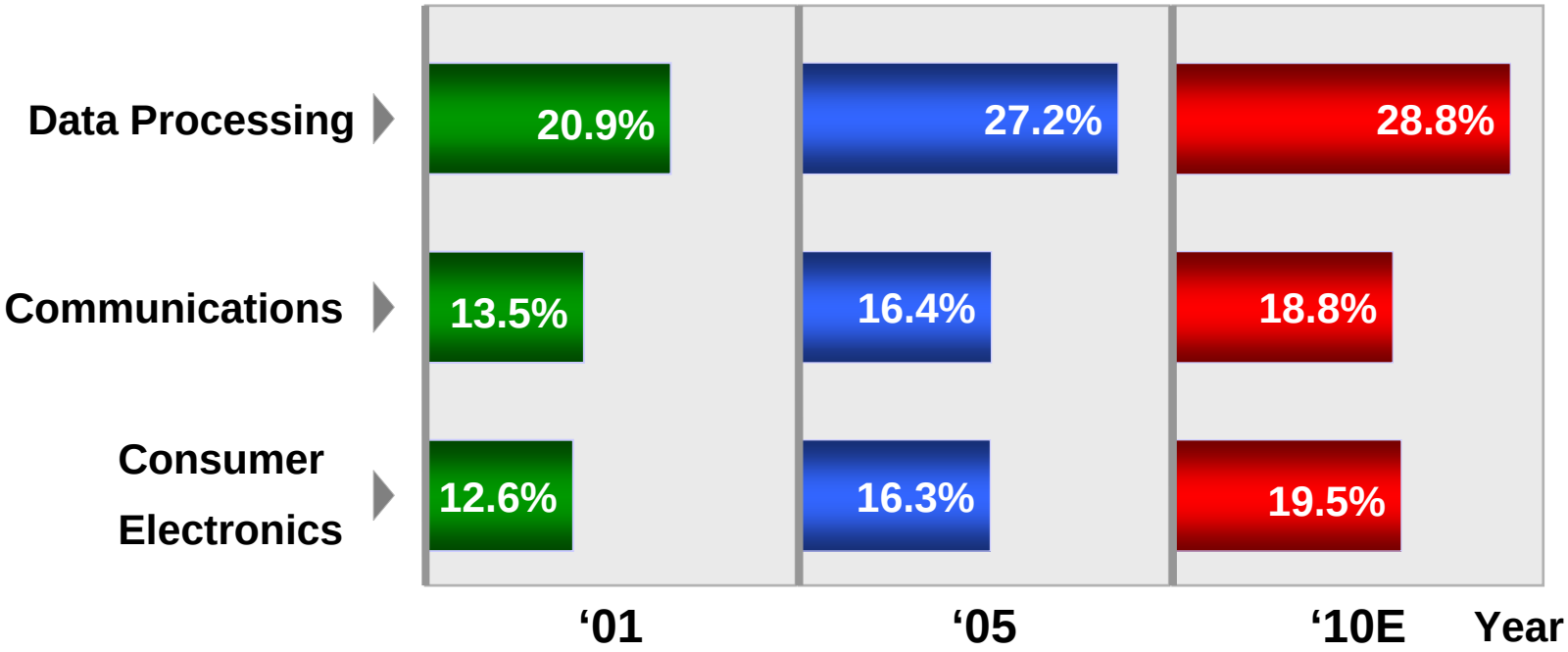


Year	Growth
'02	+1%
'03	+18%
'04	+28%
'05	+7%
'06	+9%
'07	+4%
'08E	+7~9%

Source: SIA

Steady Market Expansion

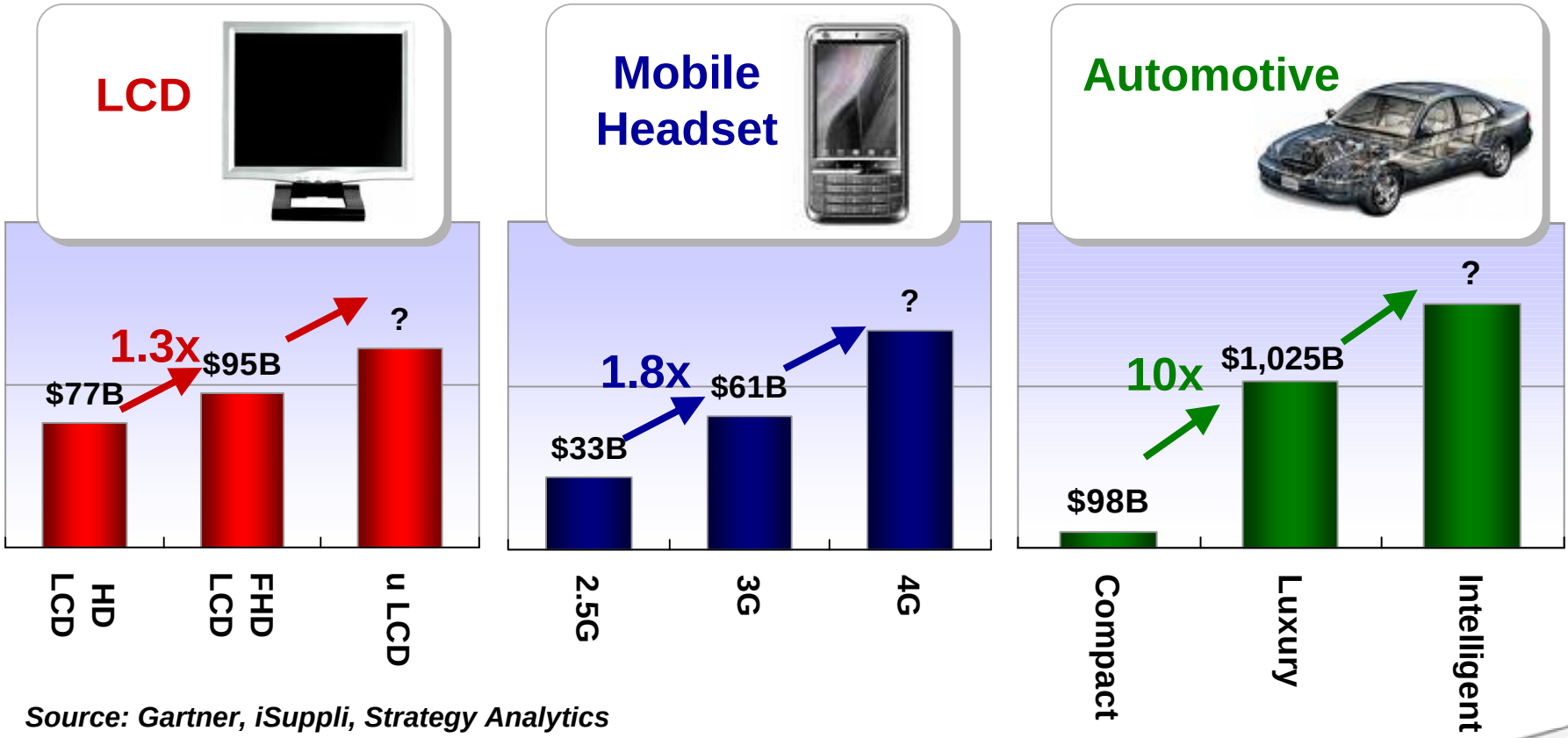
Increasing semiconductor penetration in electronics



Source: WSTS, IC Insights, TSMC estimates

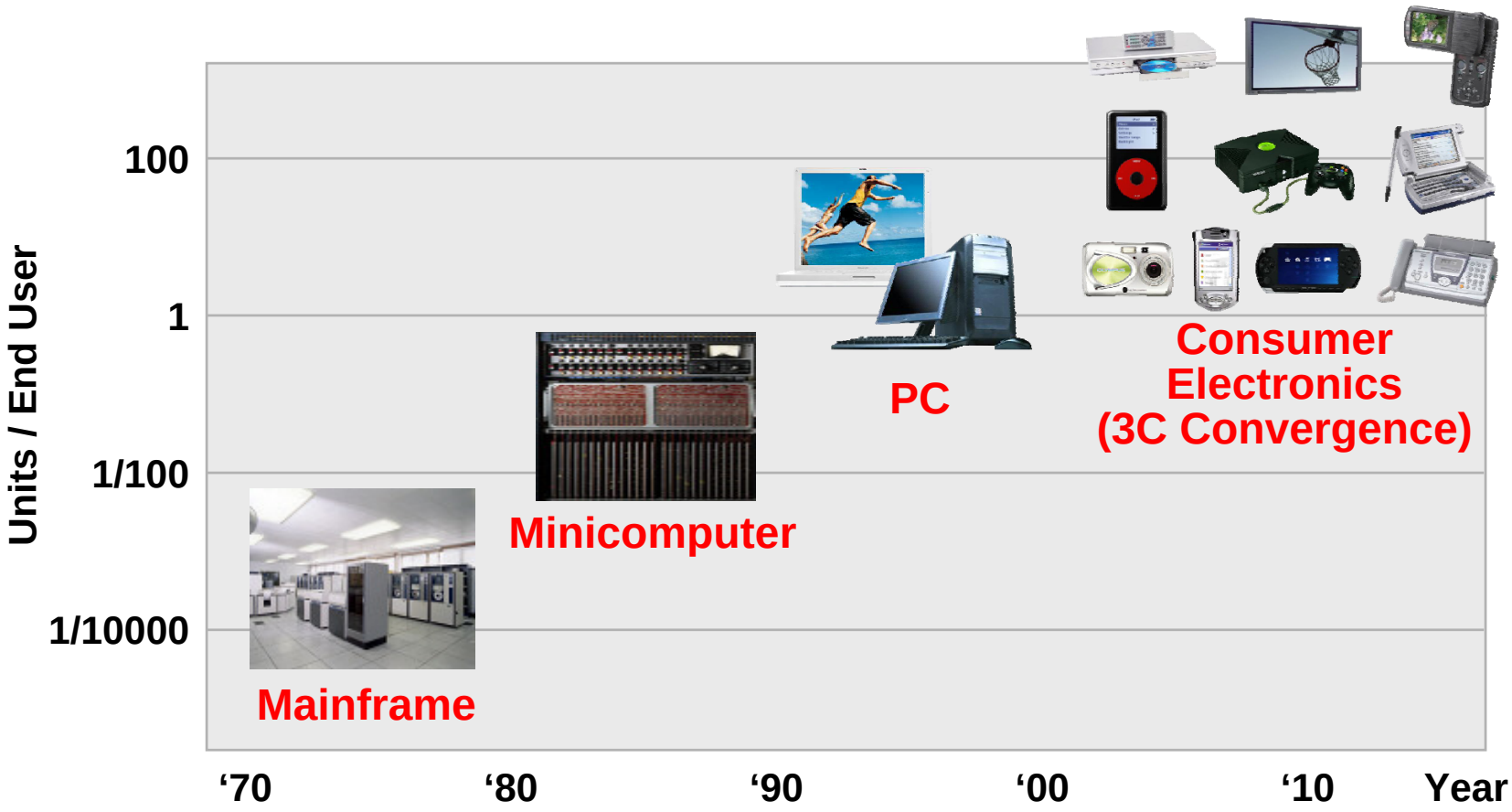
Increasing Semiconductor Content in Systems

– Functionalities and performance

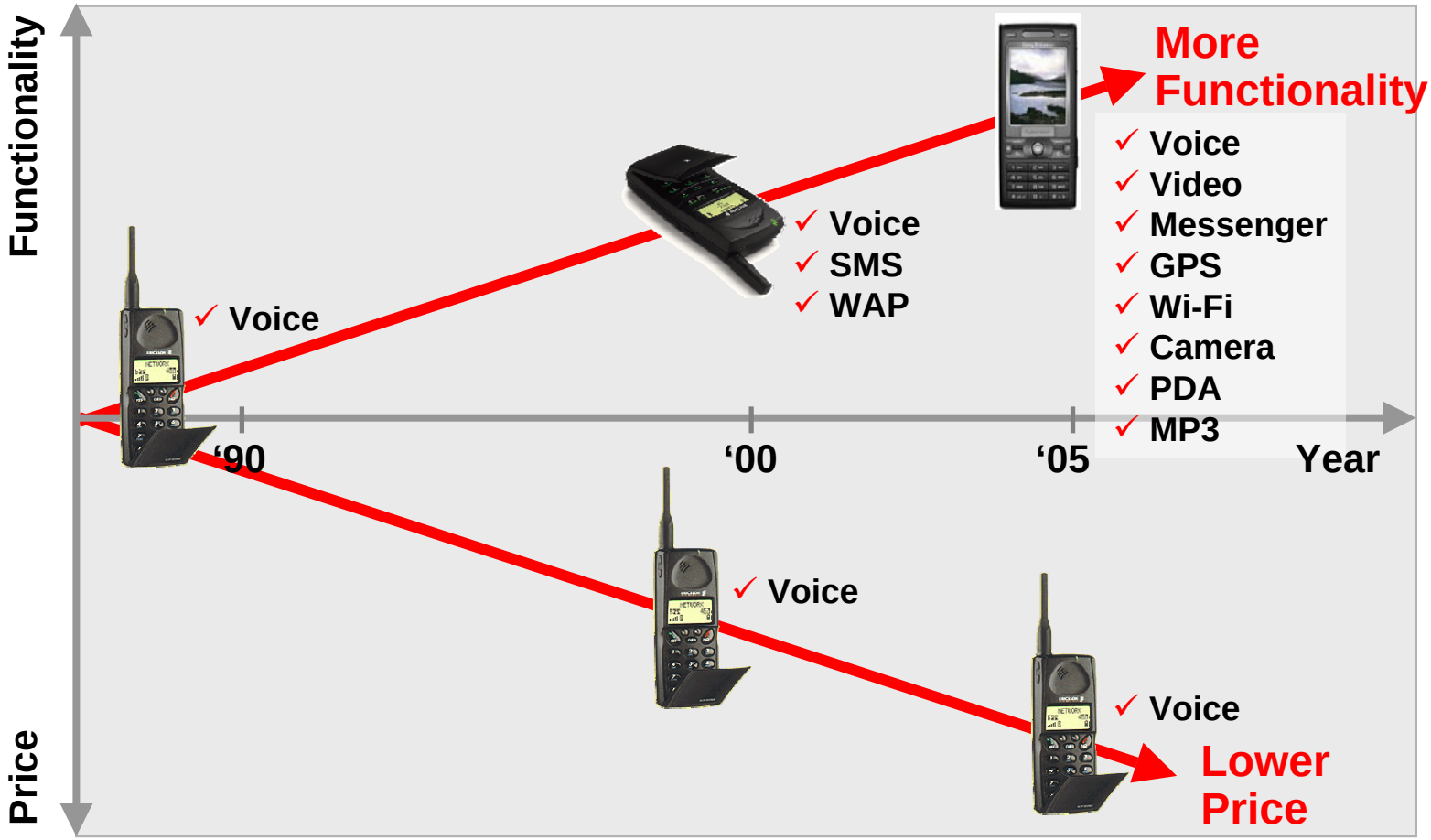


Source: Gartner, iSuppli, Strategy Analytics

New Applications as Growth Drivers



Demand from High-end and Low-end Markets



In Search of A PC to Serve “The Next Billion”

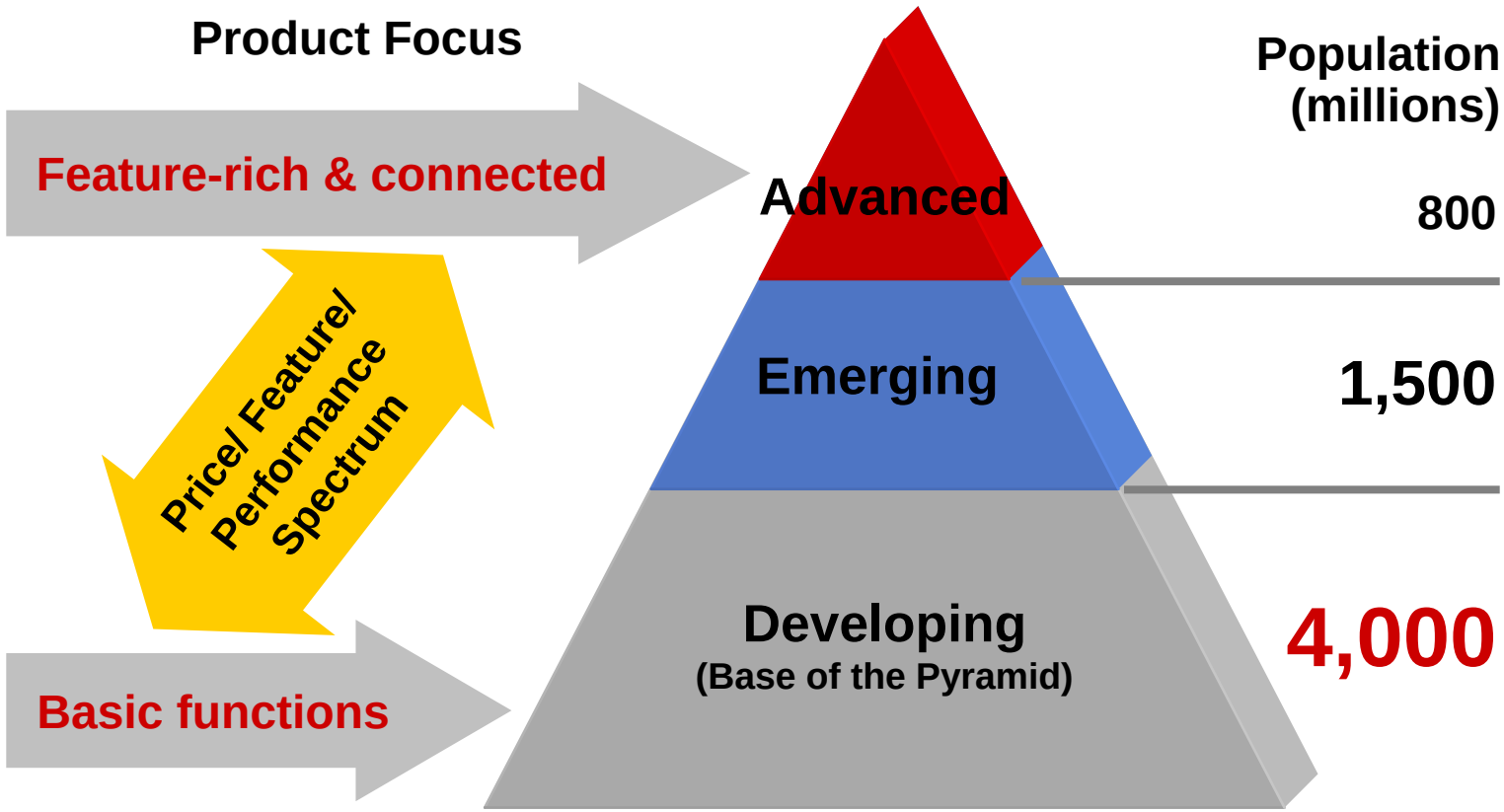
- **The low-cost PCs for the developing nations:**

INTEL
“ClassMate”

ASUS
“Eee”

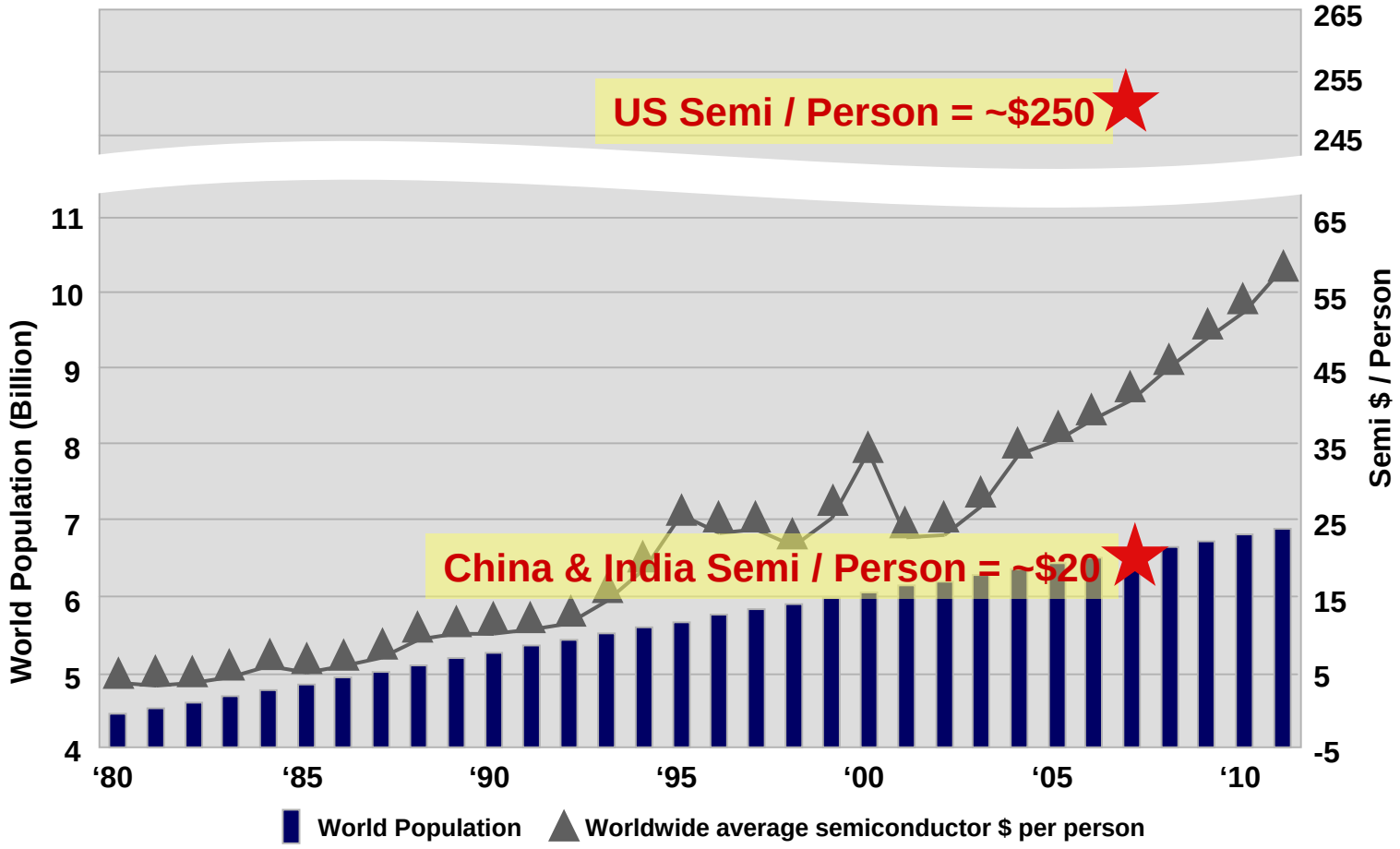
One Laptop Per Child
“XO”

Growth Opportunities are Global



Source: "The fortune at the bottom of the pyramid" by C. K. Prahalad, and IMF

Plenty of Opportunity Ahead



Source: US Census Bureau; IC-Insights; TSMC estimates

Outline

- Semiconductor Market Outlook
- Challenges and Solutions
  - Economic
  - Technology
- Summary

Challenges

Economic

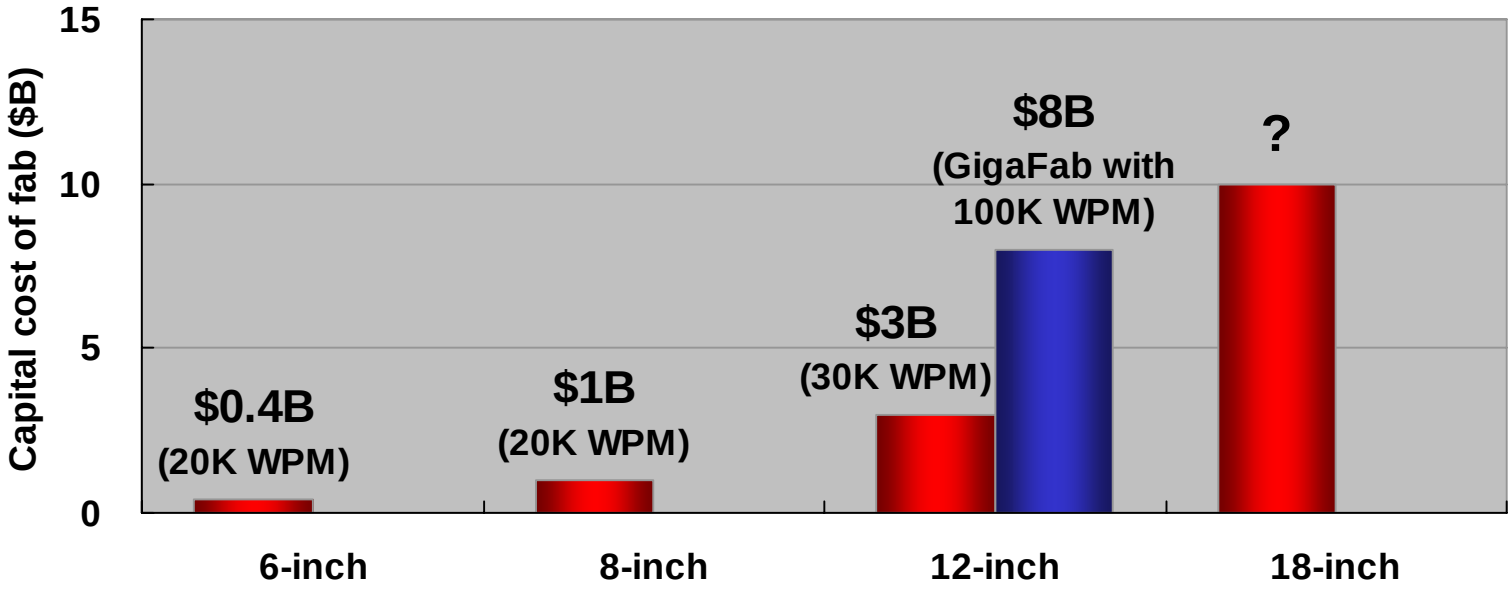
1. Huge CapEx
2. ROI Risk – Process
3. ROI Risk – Product

Technology

4. Nanometer Manufacturing
5. Nanometer Design
6. Design Complexity

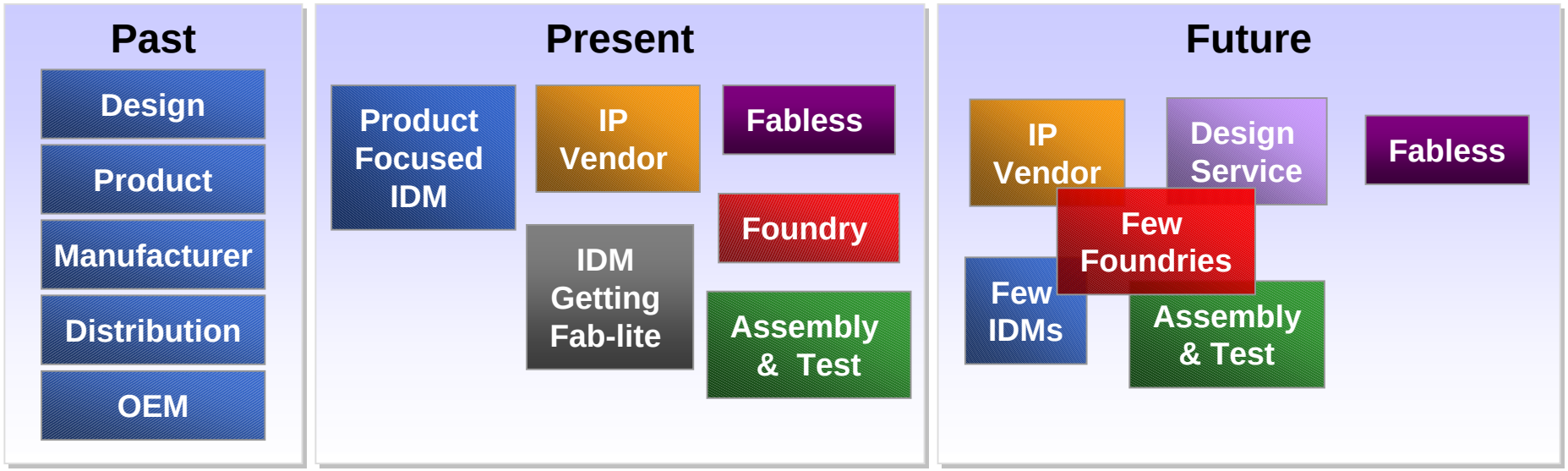
1. Huge CapEx

- **Capital expenditure for constructing a new fab is rapidly increasing**
  - **Major factor for financing and future profit**



Solution – Foundry Based Business Model

- Many IDMs are changing to either fab-lite of fabless
- A wide variety of consolidation and collaboration are inevitable



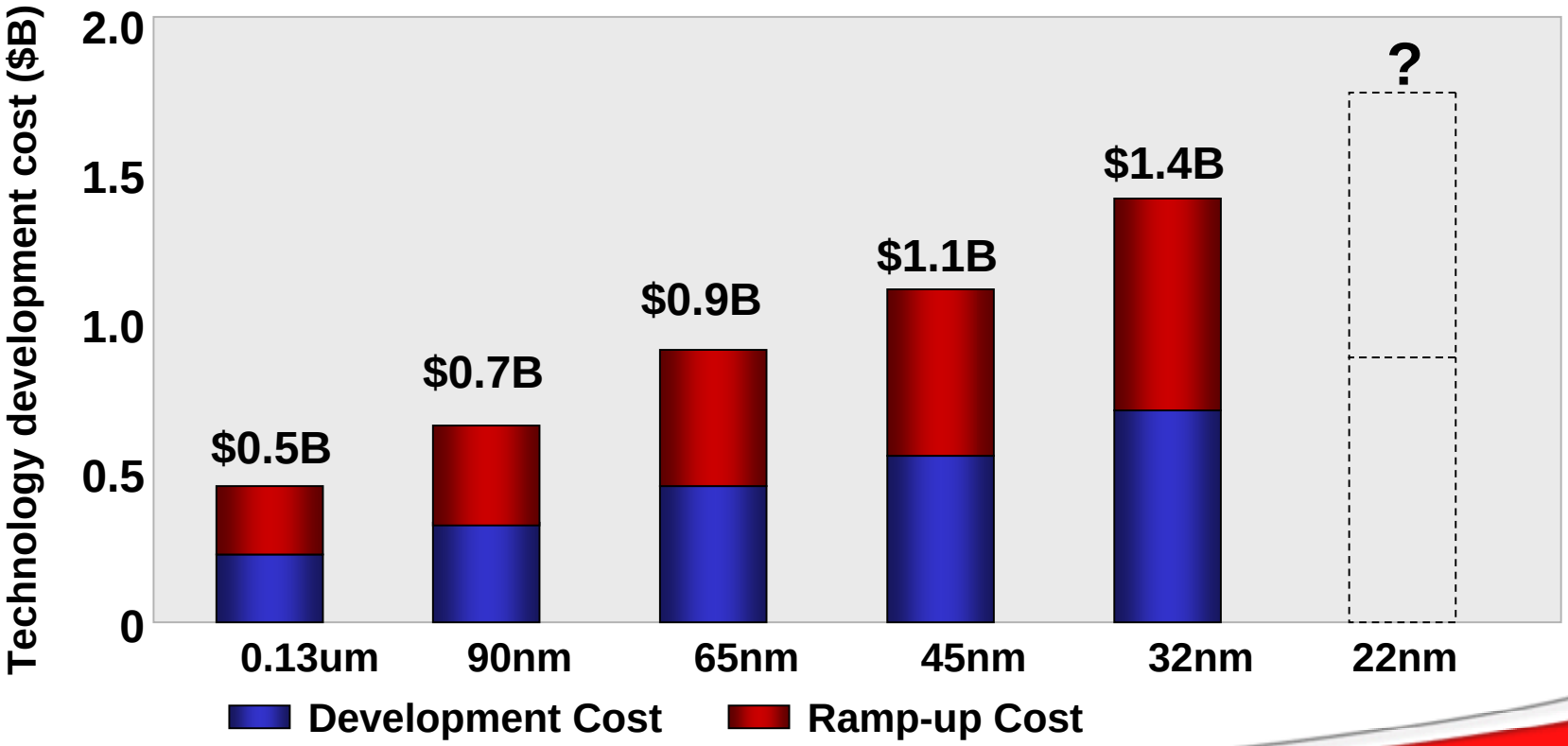
Vertically Integrated

IDMs in Transition, Fabless Getting Bigger

Few IDMs & Foundries, Many Fabless

2. ROI Risk – Process

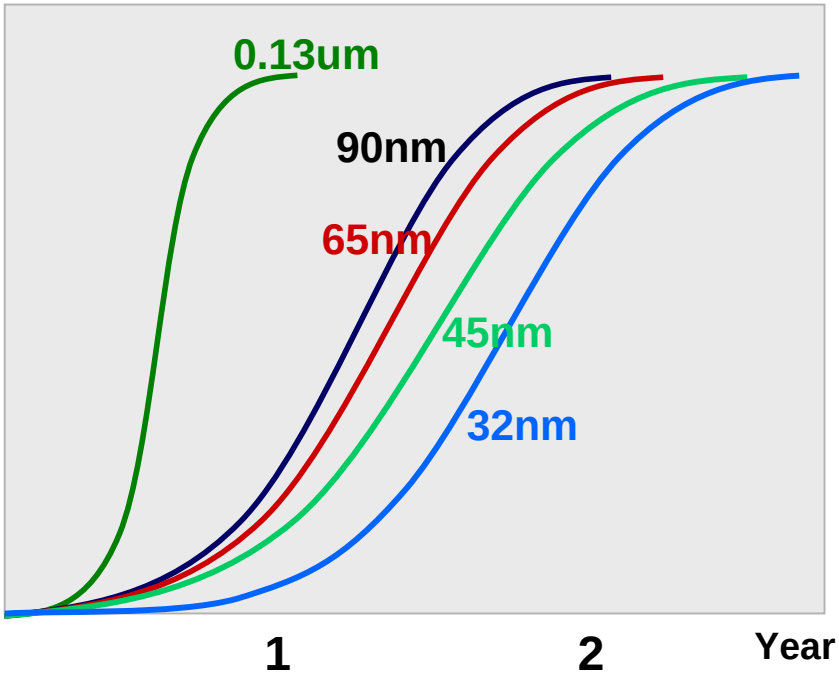
- Incremental challenges in developing next generation processes
- Process technology development costs are continuously increasing



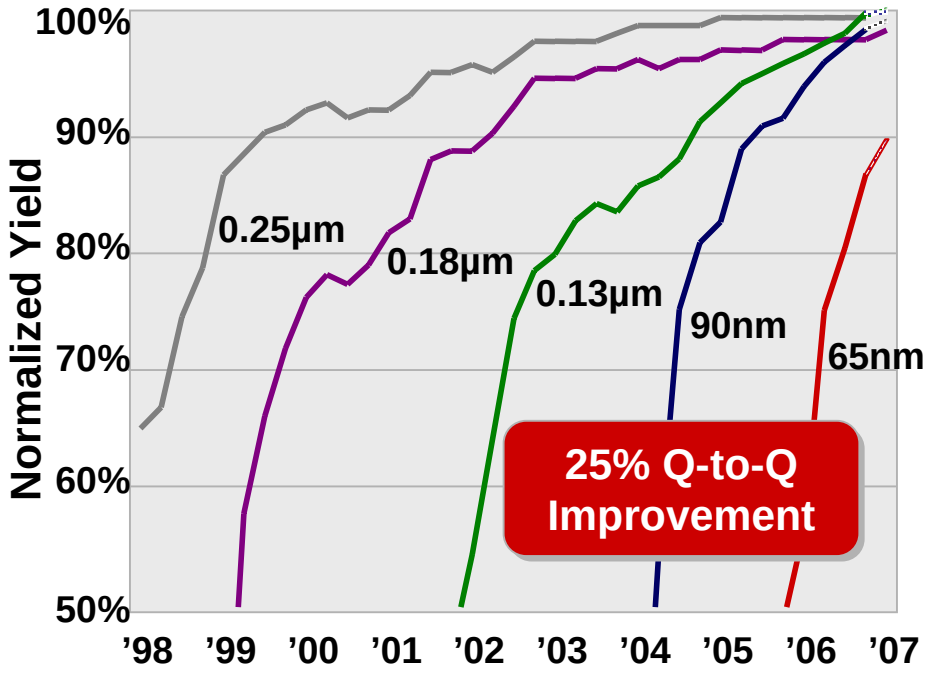
2. ROI Risk – Process (Cont'd)

- **Yield ramp-up requires significant time and investment**

In-house manufacturing with limited products

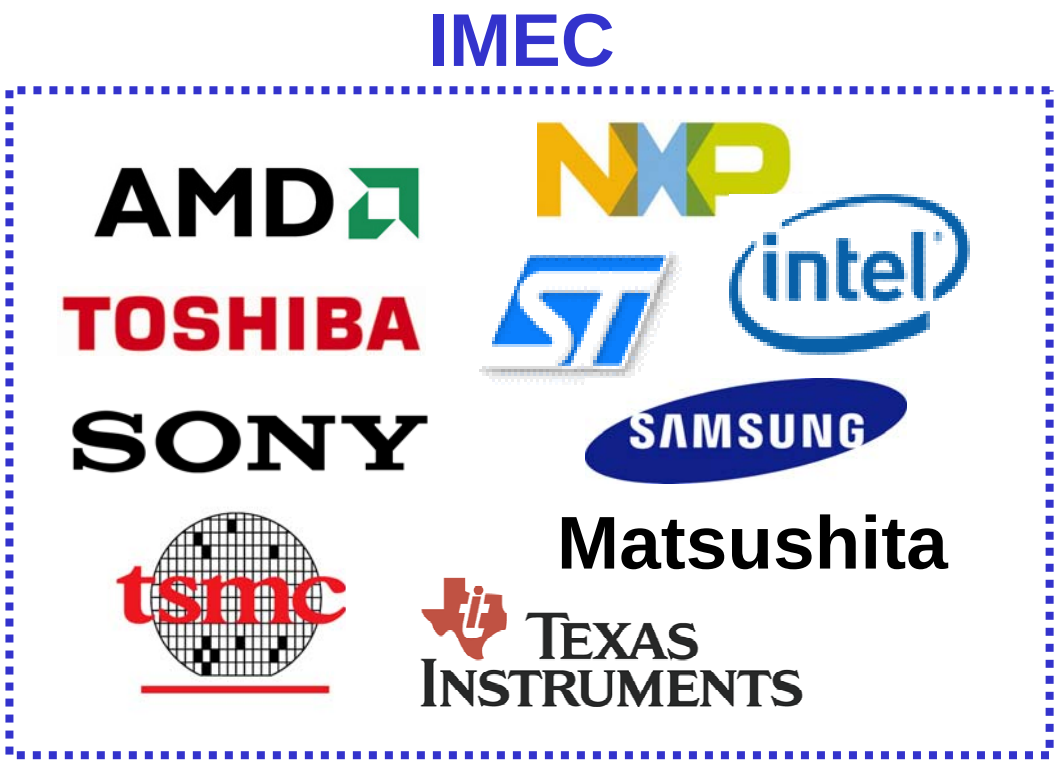


Foundry has the economy of scale



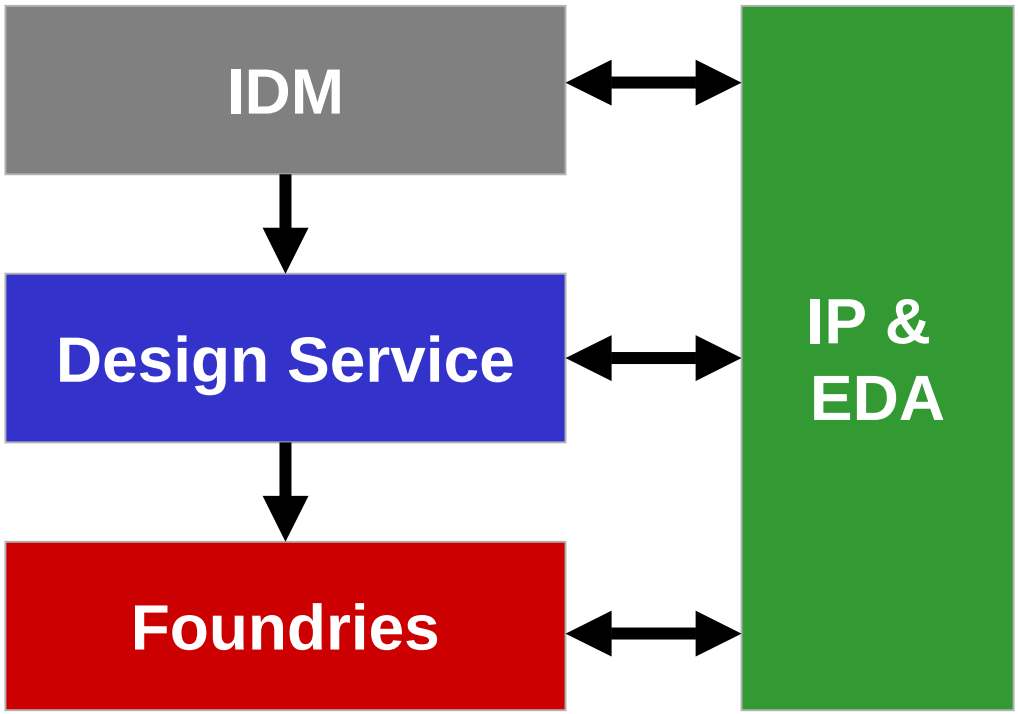
Solution I – Technology Alliance

- Collaboration is required to overcame ever – increasing financial as well as technical challenges



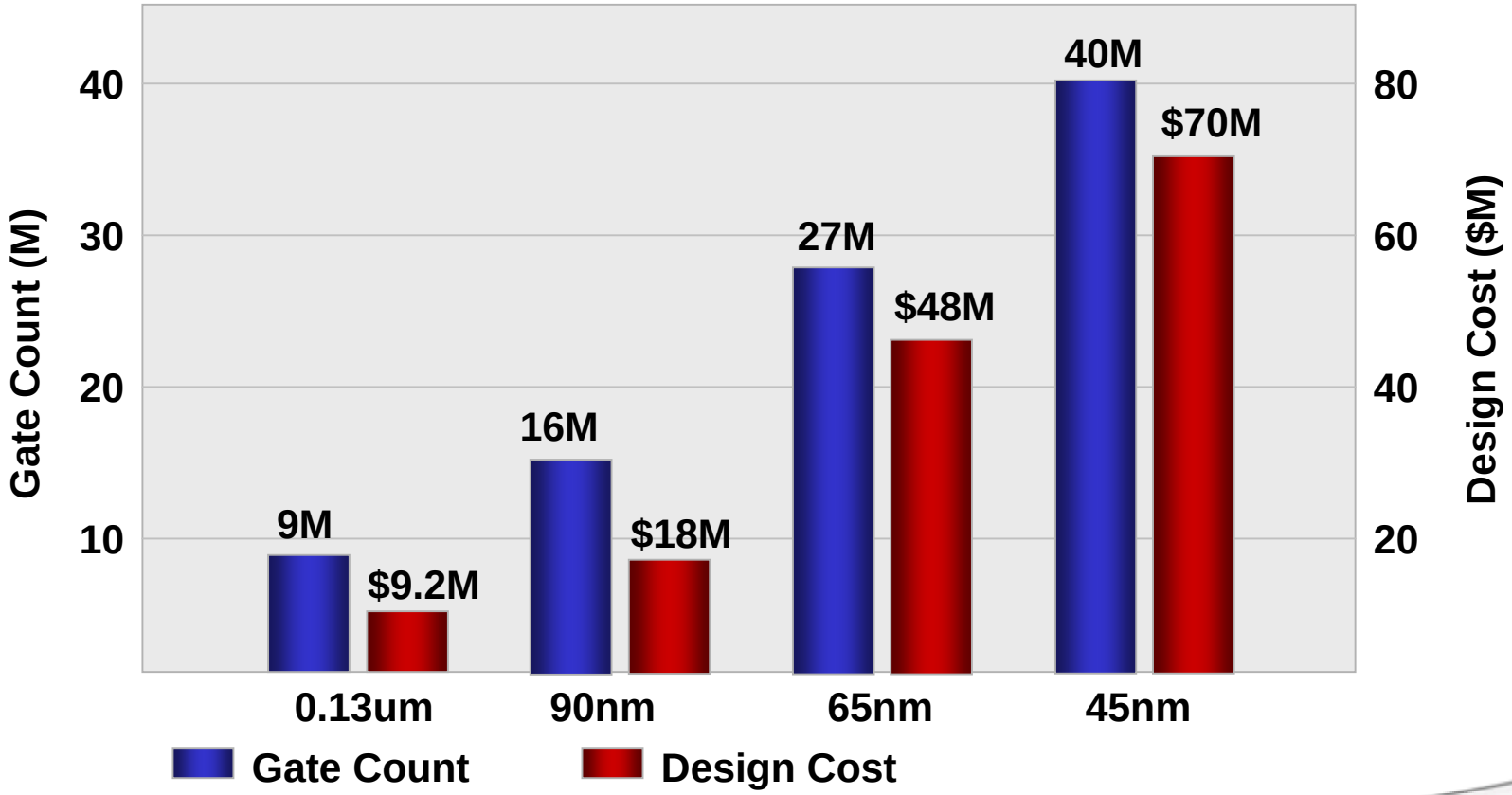
Solution II – Collaboration among Foundry, IP/EDA Vendors, And Design Service Suppliers

- Standardization of IP & EDA tools



3. ROI Risks - Product

- Design complexity and cost increase rapidly
- Short time to market



Solution - Product

- Optimal system partition
- Foundry
  - Design Infrastructure
    - SPICE
    - PDK
    - Foundation IP
  - Prototyping
    - Cybershuttle
    - MLM

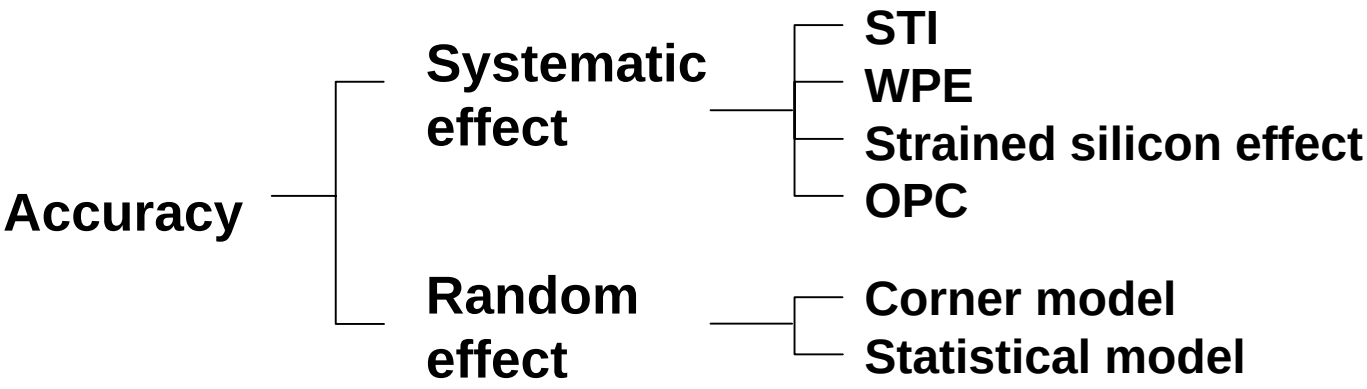
Minimize the product risk and NRE

4. Nanometer Manufacturing

- New materials and device structure
  - High-K gate dielectric
  - Metal gate
  - 3D FINFET
  - Low-K Interconnect
- New EDA solutions for technology modeling and advanced lithography

Solution – Technology Modeling / Advanced Lithography

- Secure accurate SPICE modeling



- Modeling in new material, 3D device and equipment / topography
- Polarization, OPC, double exposure and mask 3D effects

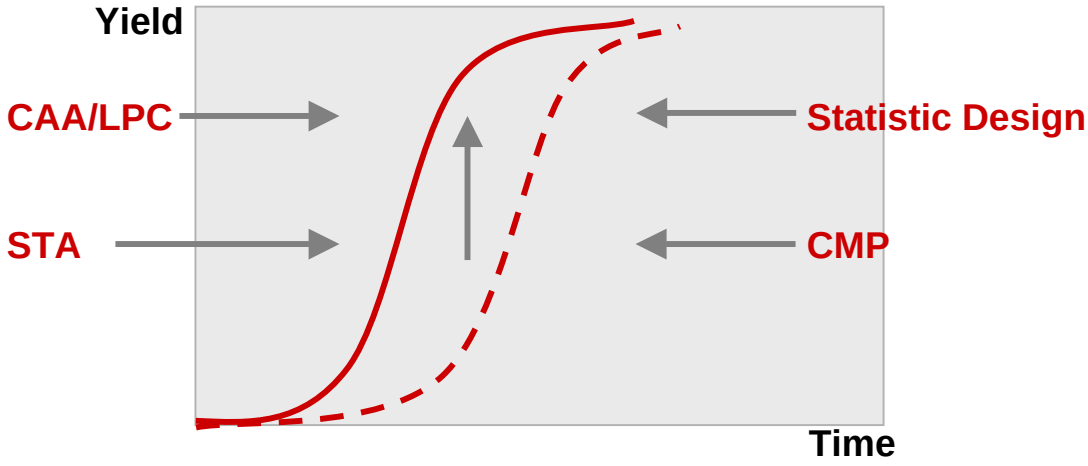
Collaborate with EDA vendors to achieve seamless interfacing hierarchy

5. Design for Nanometer

- **Increasing systematic / parameter / random yield loss due to process variation**
  - **Physical patterning effects, open and short, etc.**
  - **Chemical and mechanical impact, planarity, antenna effect, and via opens, etc.**
  - **Timing, signal integrity and voltage drop**
- **Increasing leakage (quantity, source, variation)**

Solution – Accurate DFM

- **Model & simulation-based approach for physical and electrical DFM that represents Manufacturing accurately**
  - **Physical DFM**
    - **Identify hot spot, fix it and improve geometric yield.**
  - **Electrical DFM**
    - **Identify electrical performance deviation, correct it and improve paramedic yield**

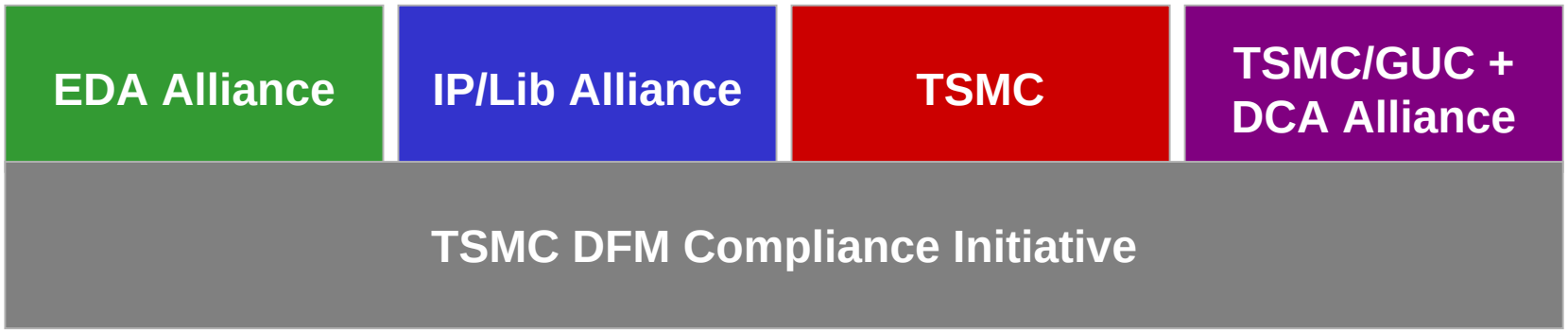


Set-up standard interface between phase and design which is design and layout phase

Solution – DFM Ecosystem

- Foundry to set up DFM ecosystem and open license DUF to reduce cost
- Standard interface between the design infrastructure and manufacturing

Example:



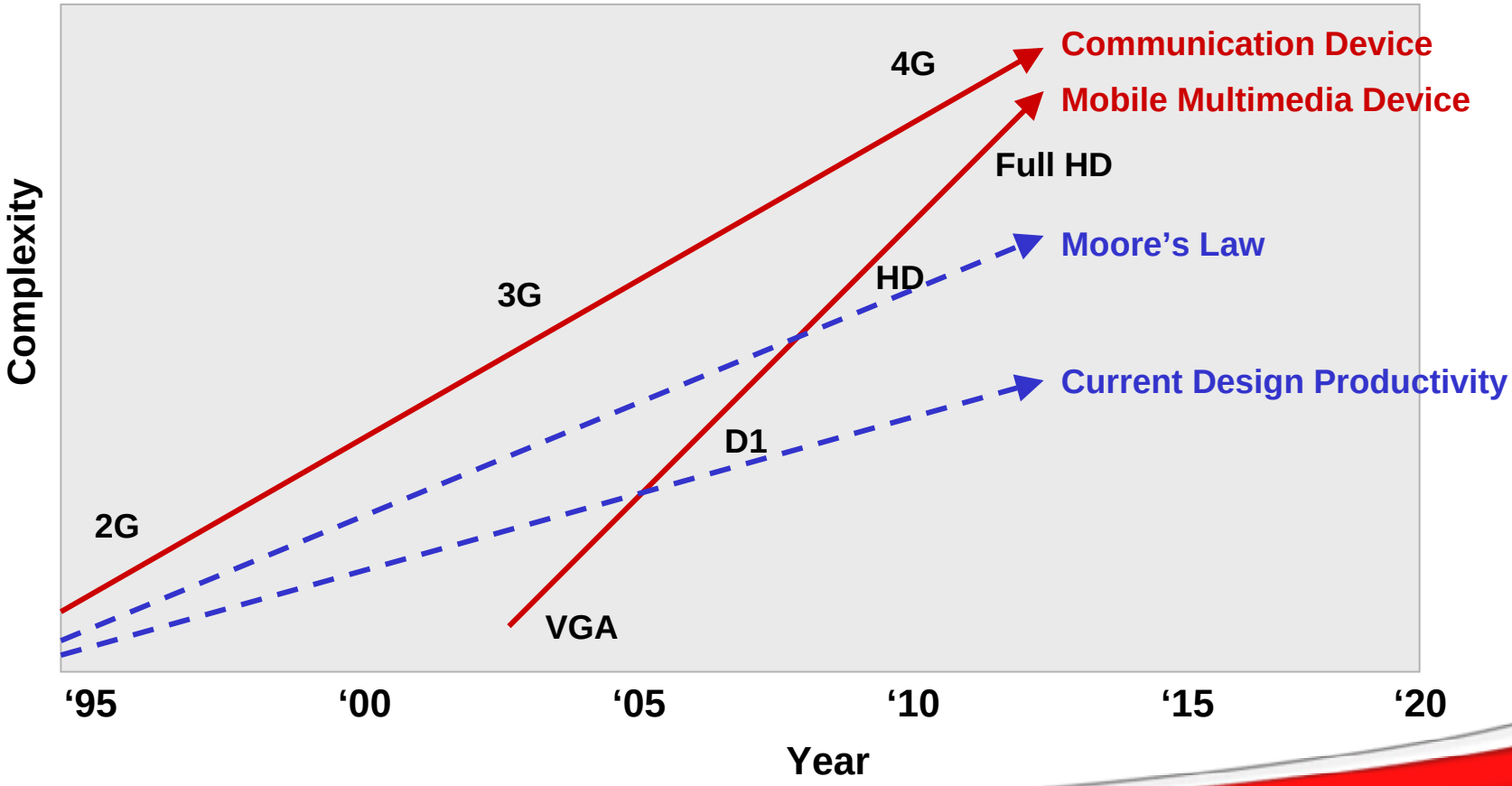
Solution – Low Power

- **Aggressively develop integrated low power solutions for dynamic and leakage power reduction**
  - **Low power process**
    - **Advanced processes with ELK/XLK die-electric: lower voltage, smaller geometry and capacitance for dynamic power reduction**
    - **HK/MG and gate CD bias for leakage reduction**
  - **Low power IP**
    - **Full set of low power foundation IP, dual power SRAM**
  - **Low power design Reference Flow**
    - **Silicon proven design methodologies for TSMC IP and processes**
    - **Voltage scaling (DVFS, AVS), power gating with data retention**
    - **Low power design automation enabling**

Develop vertically integrated solution from system-level to layout and to process

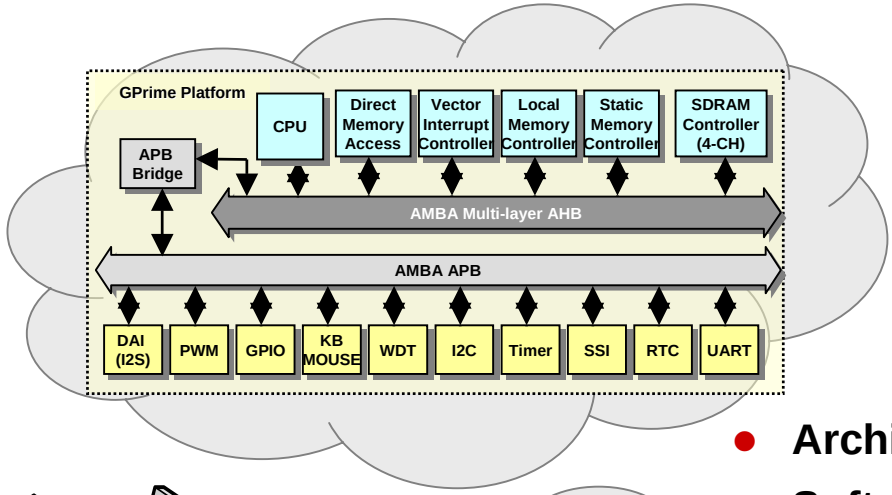
6. Design Complexity

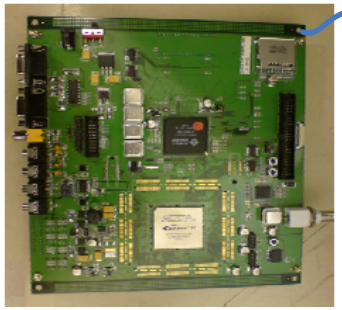
- **Increased design complexity causes longer time-to-market and requires significant effort for verification and software design**

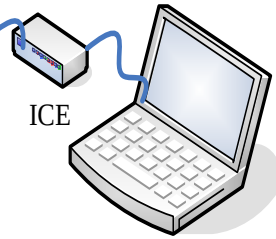


Main Stream vs. ESL Co-development Environment

Main Stream

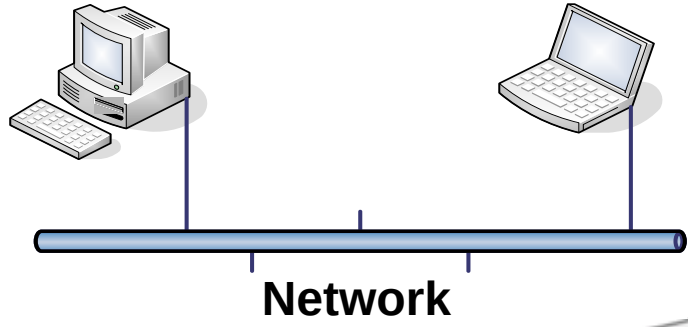






Electronic System Level (ESL)

- Architecture Exploration
- Software Profiling
- Hardware Profiling
- Power Estimation



Solution – ESL

- New ESL design technology to address design complexity, and to provide massively parallel heterogeneous MPSOC design
- SIP and 3D packaging can integrate large capacity memory and analog circuit with short time to market and low cost
- Develop product with chip and PC board at same time to improve success rate

Collaborate with EDA vendors

Summary

- Semiconductor market growth will continue but moderate
- Future growth opportunities will be global but bifurcate
- High ROI risks in design, fab, and technology could be alleviated with the integrated foundry model
- Close collaboration is required between EDA vendors, foundry and IC companies

Thank You

www.tsmc.com