A 65nm Dual-mode Baseband and Multimedia Application Processor SoC with Advanced Power and Memory Management

Tatsuya Kamei, Tetsuhiro Yamada, Takao Koike,
Masayuki Ito, Takahiro Irita, Kenichi Nitta,
Toshihiro Hattori, Shinichi Yoshioka

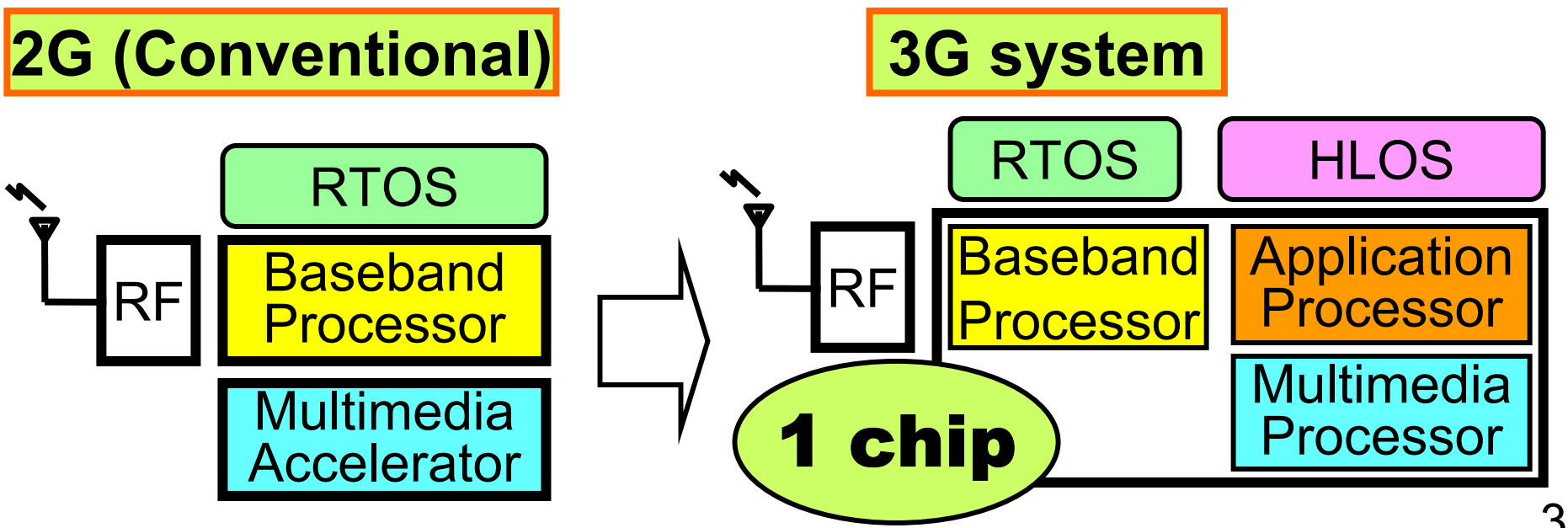
Renesas Technology Corp.

Outline

1. Introduction
2. Chip Architecture
3. Power Management
   - Static Power (Hierarchical Power Domain)
   - Dynamic Power (Partial Clock Activation)
4. Memory Management
   - IP-MMU
5. Summary

Introduction(1) Trend of Mobile phone

- In a 2G handset, a baseband processor executed applications in addition to modem control. (RTOS)
- In a high-end 3G handset, applications require High-Level-OS and rich multimedia functions. 3(BB, AP, and MM) processors in a handset.
- System cost increase ➔ **1 chip integration**



Introduction(2) Challenges

- **Low Power**
  - Limited battery capacity
  - No fan
- **High Performance**
  - Digital TV
  - Mega-pixel camera
  - 3D graphics for games and UI
- **System Cost**
  - Memory capacity (SDRAM, NAND/NOR FLASH)
  - Packaging (SIP, POP)

Introduction(3) History of SH-Mobile G

- **1st generation SH-Mobile G1**
  - In mass production from 2006. 8
  - 141M Transistors, 90nm LP
  - Hierarchical Power Domain for leakage reduction
- **2nd generation SH-Mobile G2**
  - In mass production from 2007. 8
  - 249M Transistors, 90nm LP
  - Inter-Connect Buffer for high-performance multimedia
- **3rd generation SH-Mobile G3**
  - In mass production from 2008. 8
  - 307M Transistors, 65nm LP
  - Partial Clock Activation for dynamic power reduction
  - IP-MMU for memory footprint reduction

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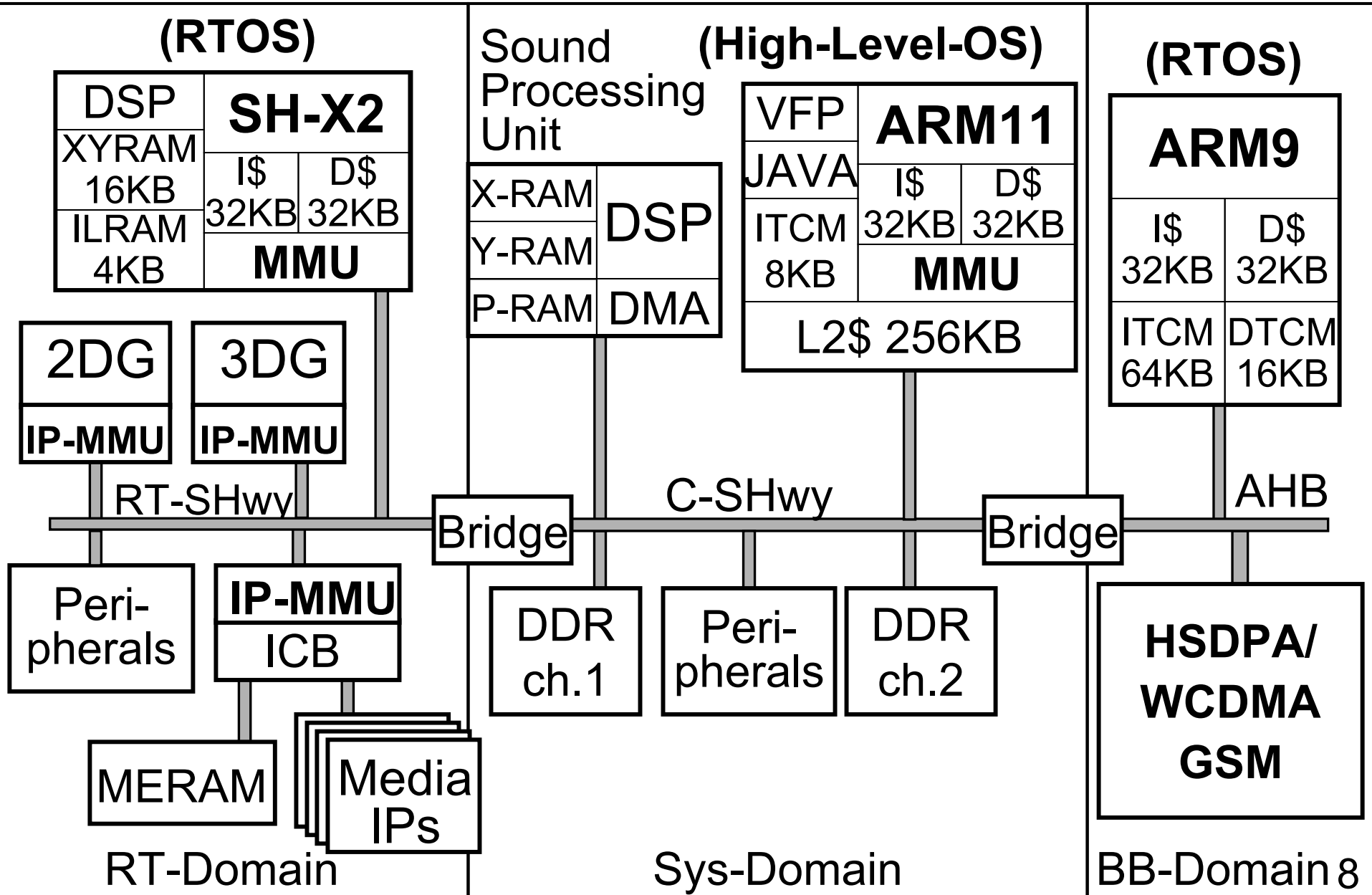
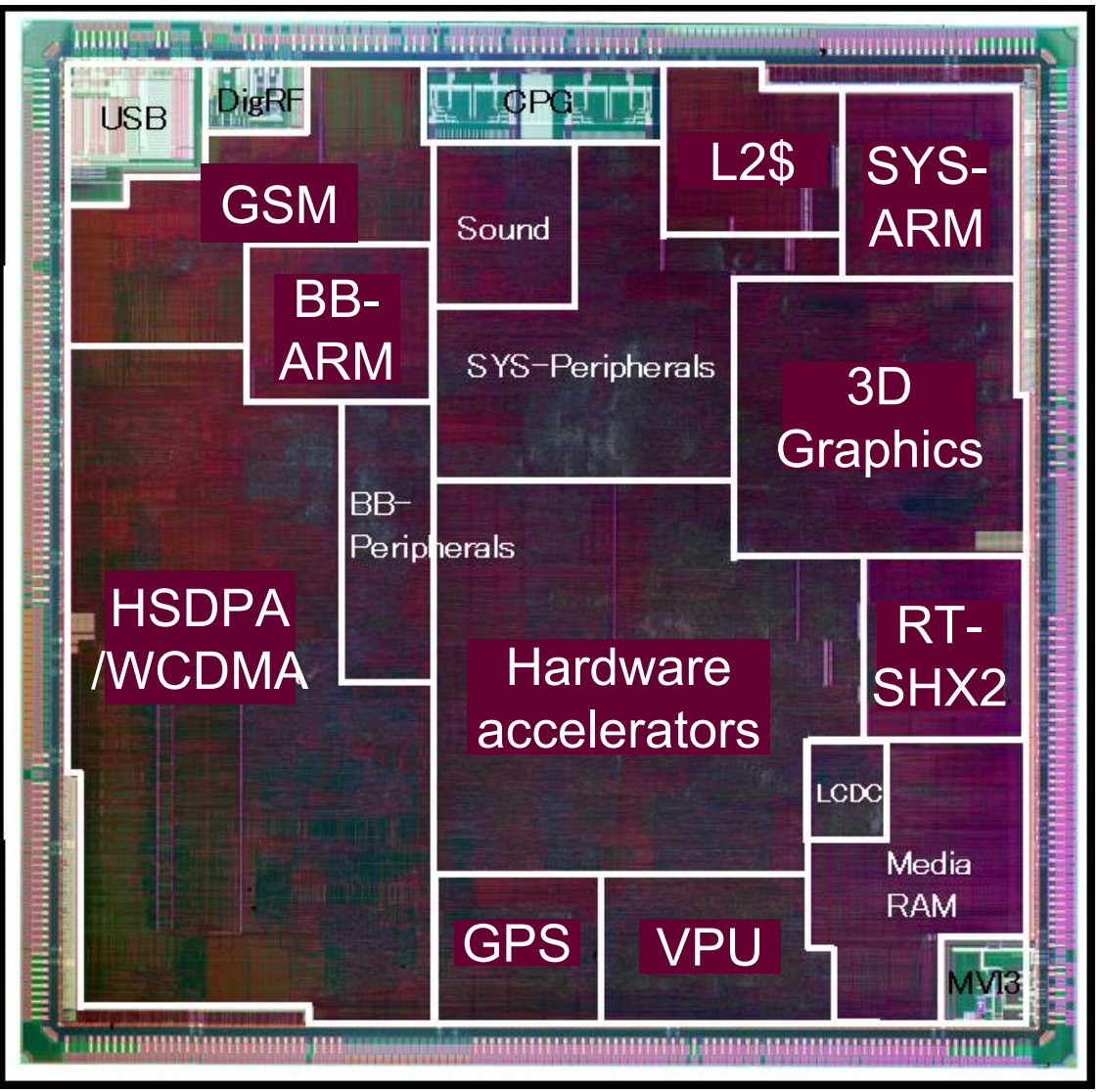
SH-Mobile G3 Chip Specifications

CPU	ARM926EJ-S, 166MHz [baseband] ARM1176JZF-S, 500MHz [application] SH-X2, 500MHz [multimedia]
3G/2G modem	W-CDMA/HSDPA Cat. 8 (up to 7.2 Mbps), GSM/GPRS/EDGE
Multimedia hardware engines	Video Processing Unit(VPU) (MPEG4/H.264/VC-1 D1 size), Sound Processing Unit(SPU), 3D/2D Graphics, GPS, LCDC, Camera interface (up to 12M pixels), 512KBytes MediaRAM(MERAM)
I/O	617 pins

Block Diagram (Bus Architecture)



Die micrograph



Die size	9.3mmx9.3mm
Process	65nm LP 8M(7Cu+1Al) 3Vth CMOS
Supply voltage	1.2V(internal), 1.8/2.5/3.3V (I/O)
# of TRs, gate, memory	307M TRs (28.2M Gates, 30.7Mb RAM, 6.4Mb ROM)

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Power Management

Both Static and Dynamic Power are very important for mobile application!

- Static Power Consumption (Leakage)

  Objective: Standby time

  Technique: Hierarchical Power Domain (HPD)

- Dynamic Power Consumption

  Objective: Operational time

  Technique: Partial Clock Activation (PCA)

Static Power Management

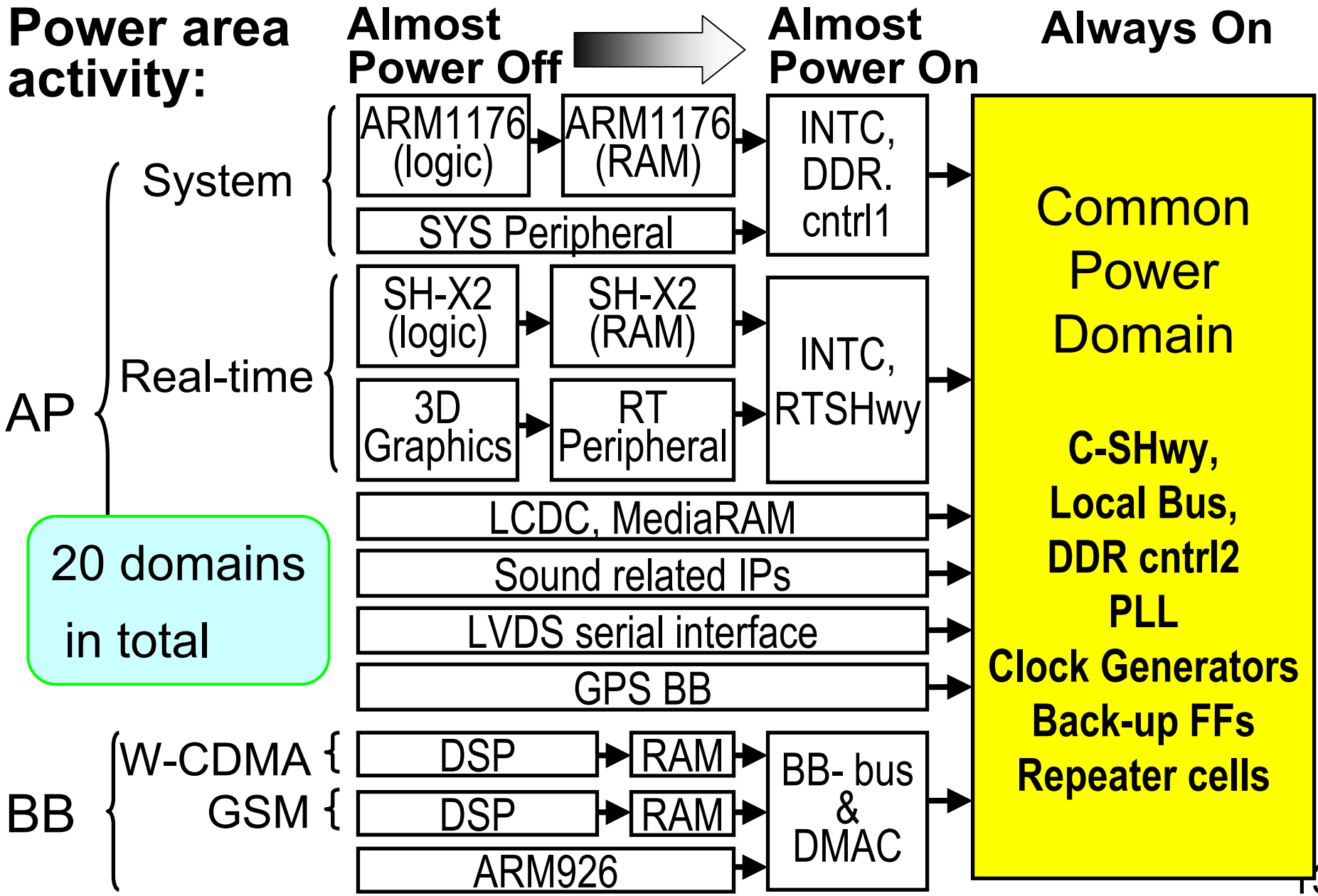
Tr. Vth	Leakage	Frequency
HVth	Good (Low)	Poor (Low)
MVth	Moderate	Moderate
LVth	Poor (High)	Good (High)

- Triple Vth technology
- Power Domain Separation (Partial Power-Off)

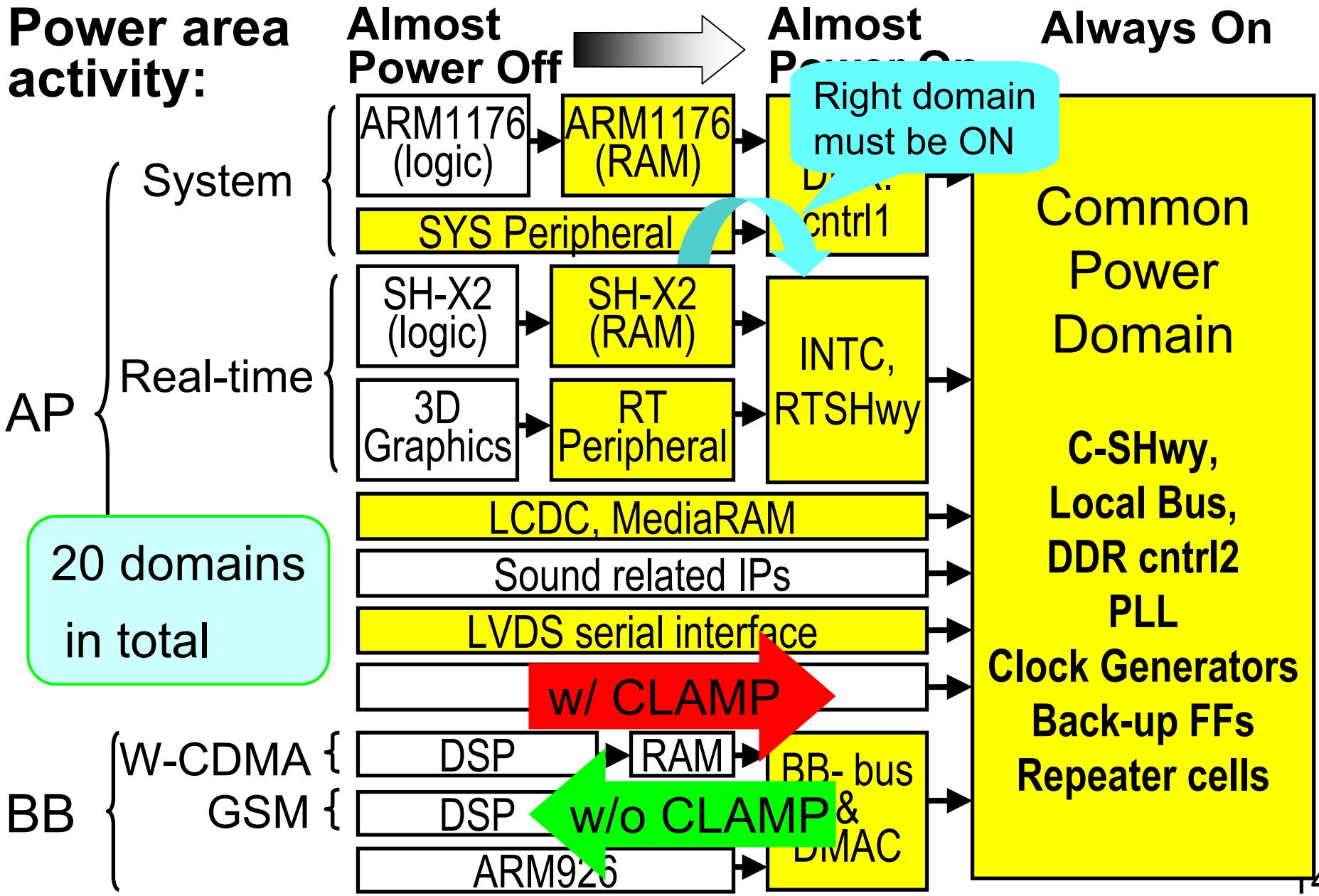
# of domains	Pros	Cons
Few	Easy to control	Limited Leakage reduction
Many	Optimal Leakage reduction	**Difficult to control**

Hierarchical Power Domain (HPD)

Hierarchical Power Domain



Hierarchical Power Domain



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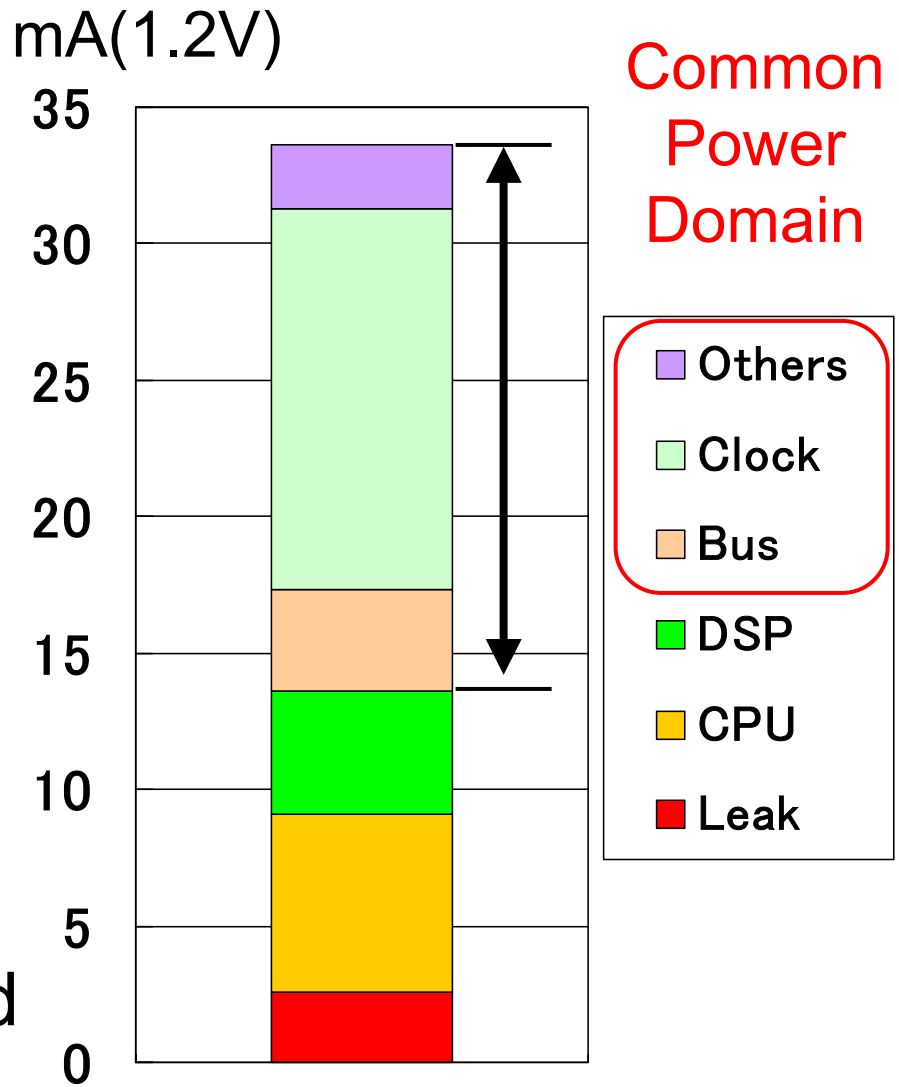
Dynamic Power Management

- At low power scenario (music replay etc.), estimated power would go over the budget.
- all un-used domains already in power-off
- Clock gating already applied deeply
- In this case, Common Power Domain consumed large percentage of whole chip power (60%).

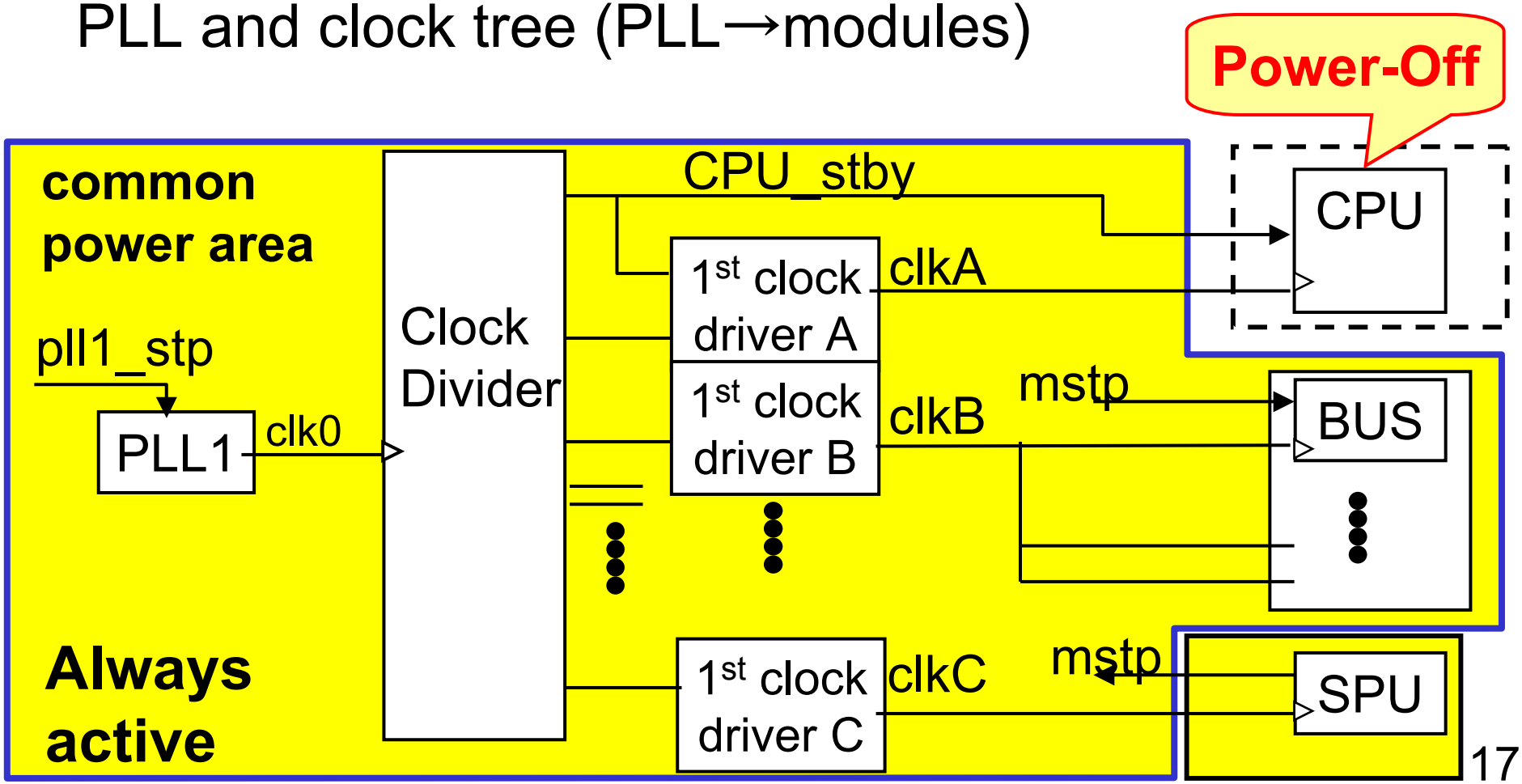


scene: long time music replay

Partial Clock Activation: Motivation

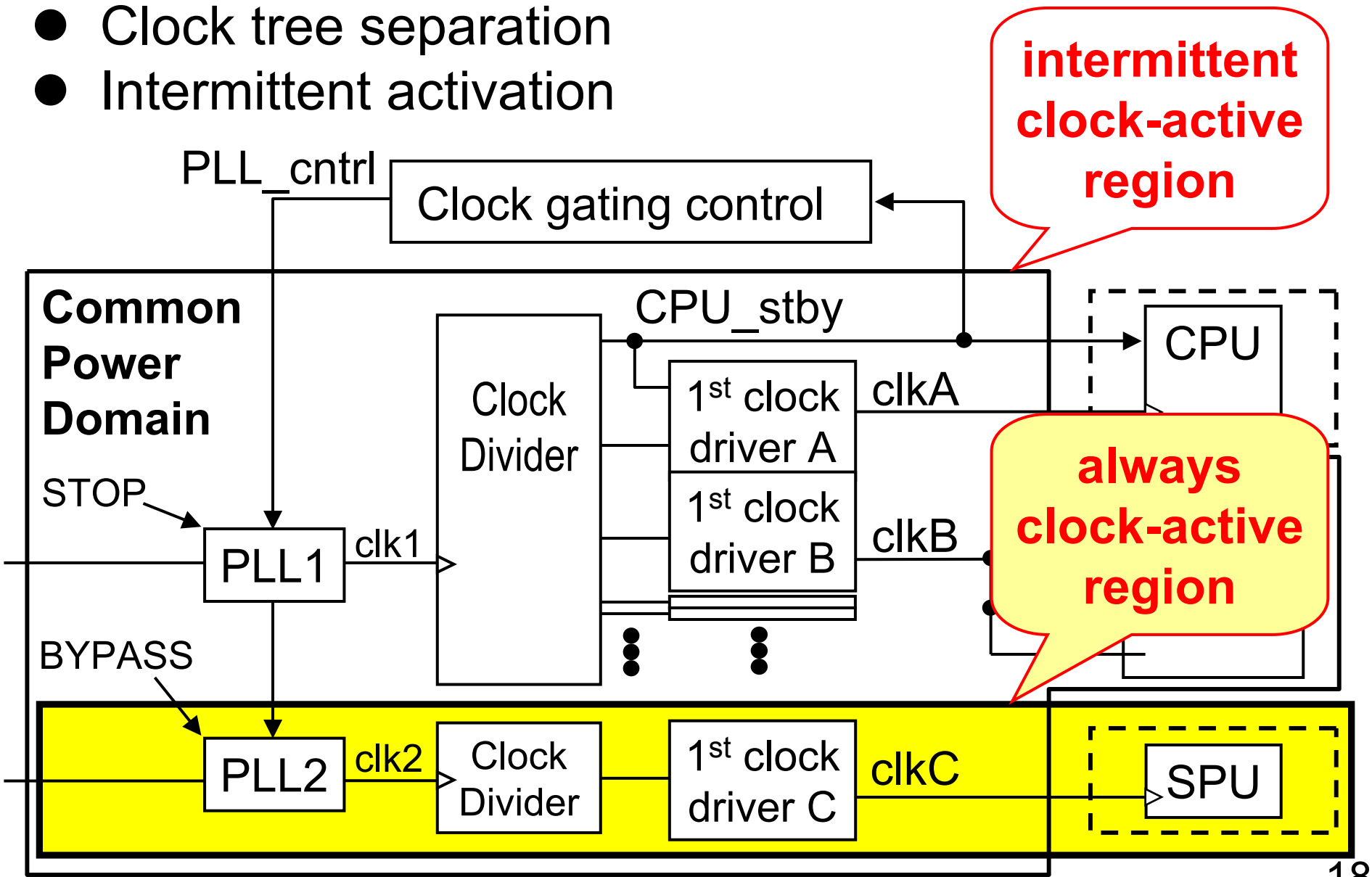
[Problem cause]

- Big modules have already been in power-off.
- But accumulated “small” power is not negligible.
  PLL and clock tree (PLL→modules)



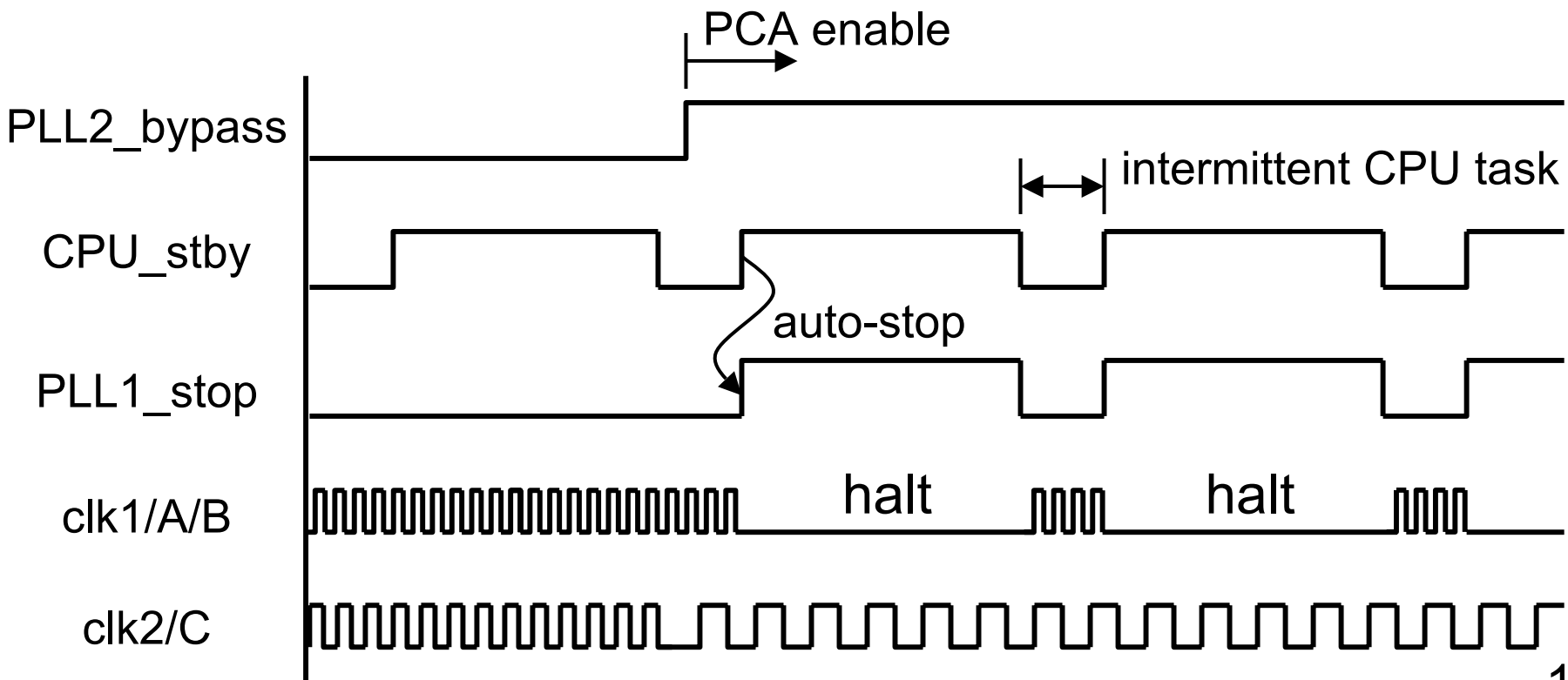
Partial Clock Activation: Diagram

- Clock tree separation
- Intermittent activation



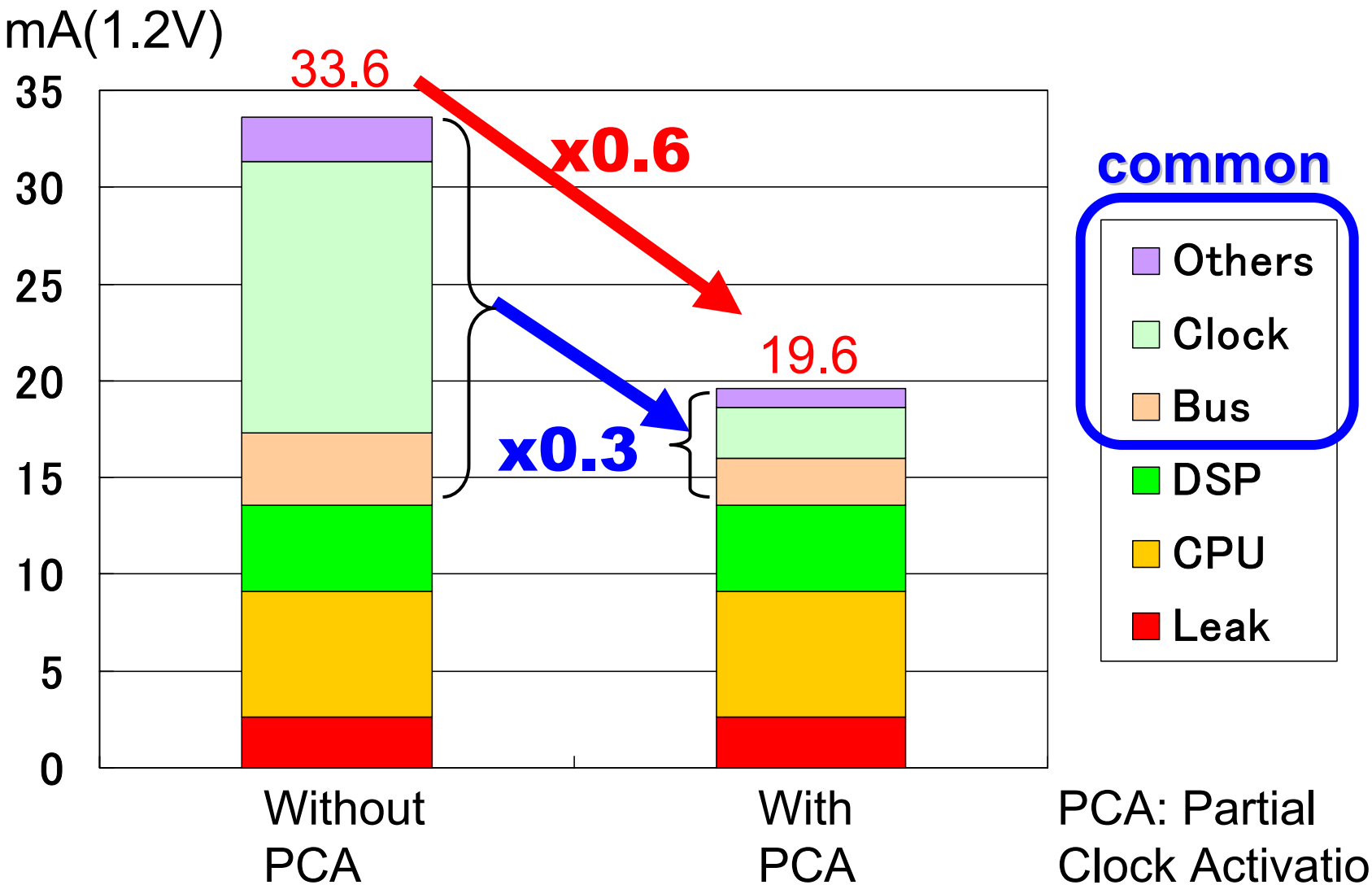
Partial Clock Activation: Control

- Clock for SPU and serial IO is slowed down (PLL2 is bypassed.)
- PLL1 and clock tree is stopped in synchronization with CPU stand-by. They are reactivated in intermittent manner for housekeeping operation. (data copy from SD-card to SPU)



Partial Clock Activation: Result

Scene: Long time music replay



PCA: Partial Clock Activation

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Memory Management: Motivation

In general, efficient memory management is required for mobile phone due to limited memory capacity.

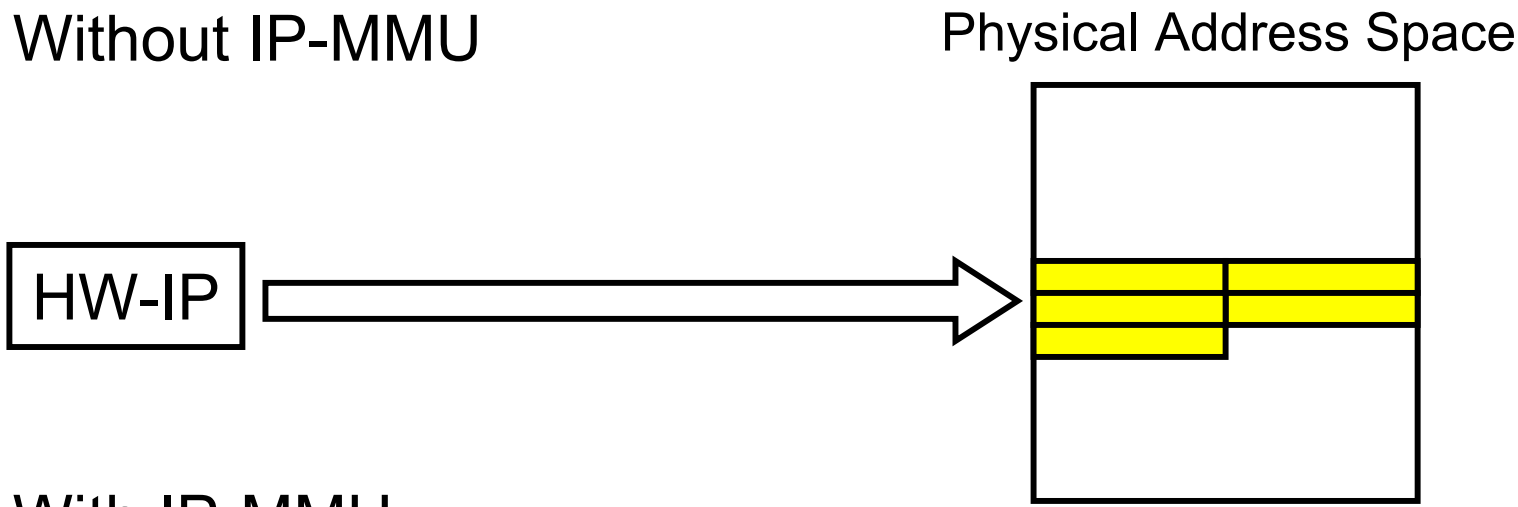
Goal: To reduce system cost by minimizing memory footprint

However,

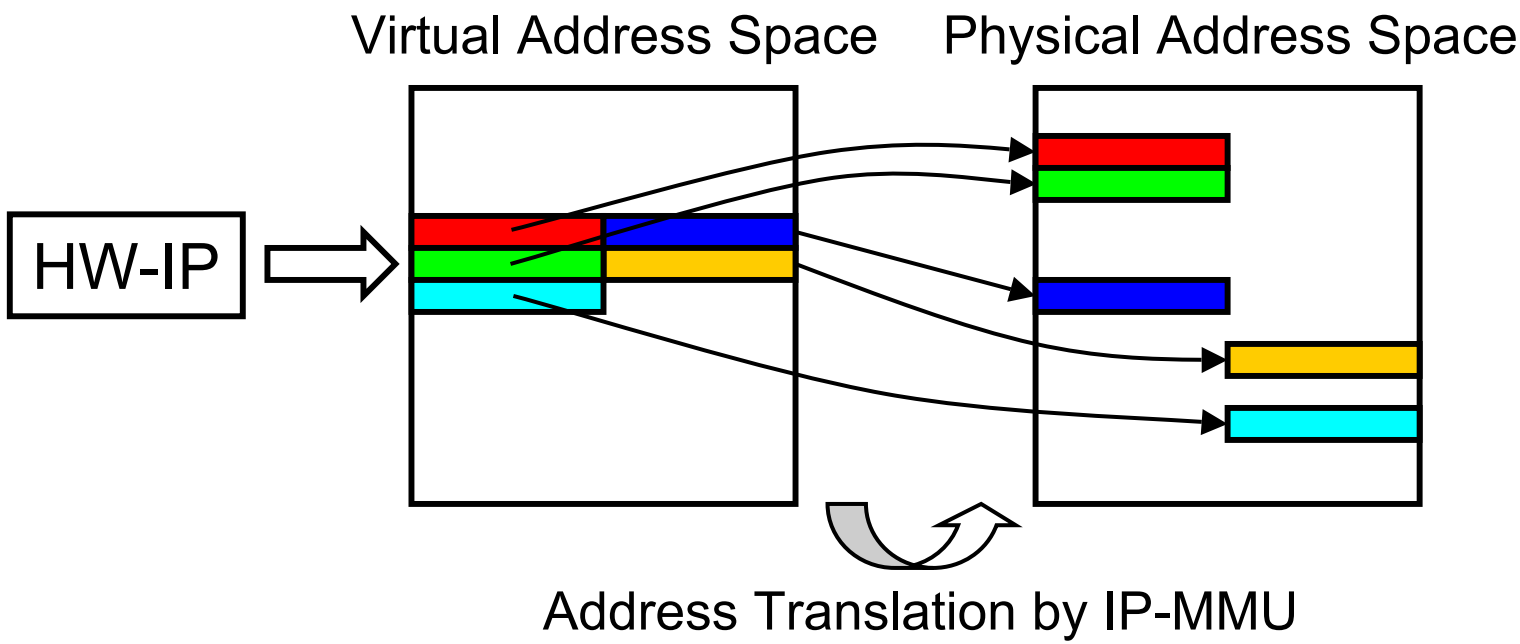
1. HW-IP (Accelerator) requires address-contiguous large memory regions.
2. Memory fragmentation proceeds with application execution. Large memory chunk may not remain after some applications have run (even after exit)!
3. To avoid this fragmentation, large memory regions have to be statically allocated at boot phase .
4. As a result, system footprint on main memory becomes very large although actual memory size in use at the same time is not so large!

IP-MMU: Concept

(a) Without IP-MMU



(b) With IP-MMU



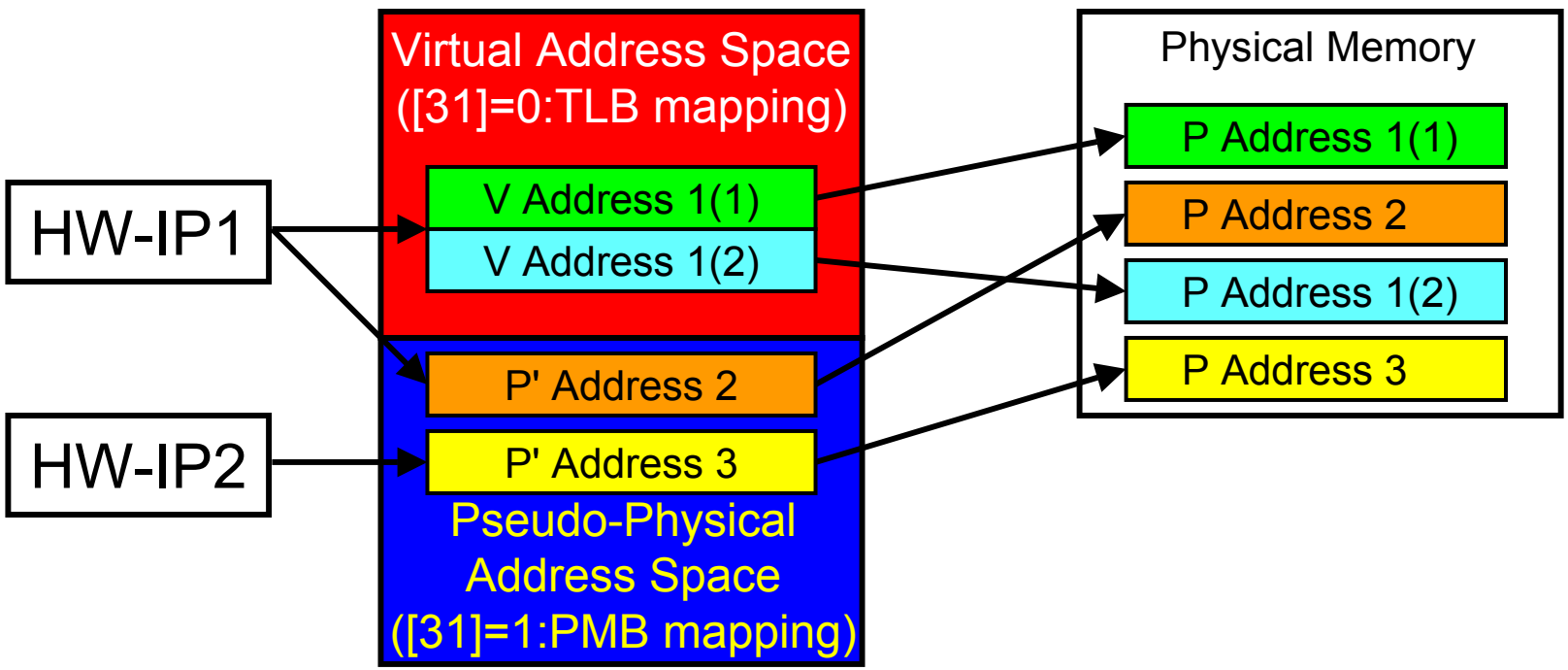
IP-MMU: Benefit

Benefit

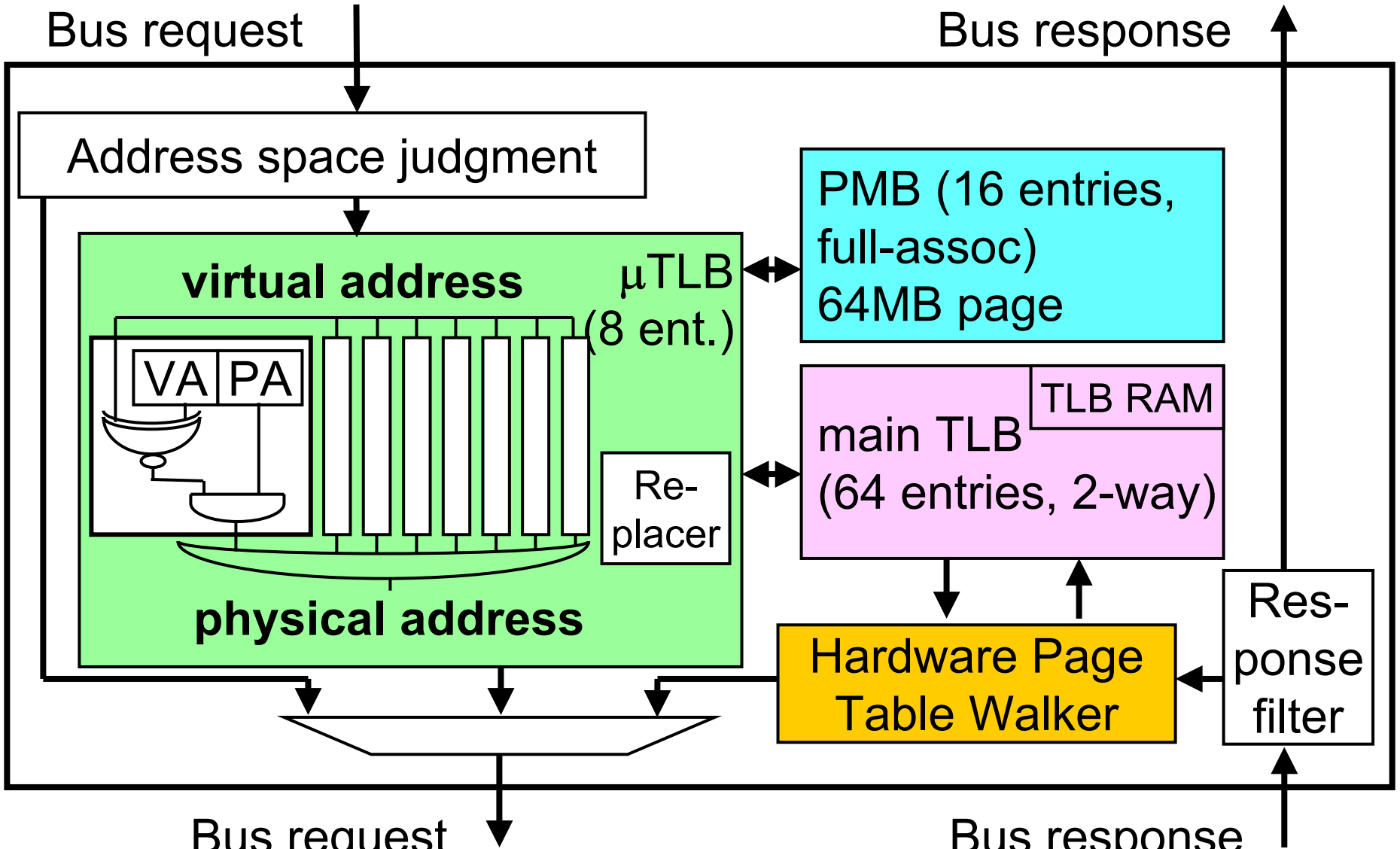
- Large address-contiguous memory regions can be composed of physically fragmented memory chunks.
  Memory regions can be freed after applications terminated and they can be allocated on demand.
  Reduction of system footprint
- HW-IP can see Virtual Address Space like CPU.
  CPU and HW-IPs can directly share the "pointer" to the memory.
  Easy development of applications utilizing HW-IPs

IP-MMU : Address Space View

- First half (2GB): TLB (Translation Look-aside Buffer)
  - Dynamically allocated by OS (4KB granularity)
  - Shared with a software process on OS
- Second half (2GB): PMB (Physical-address Mapping Buffer)
  - Statically allocated at boot time (always alive) (e.g. LCDC frame buffer)
  - Access window to arbitrary physical address



IP-MMU: Implementation (Basic)



IP-MMU: Problem

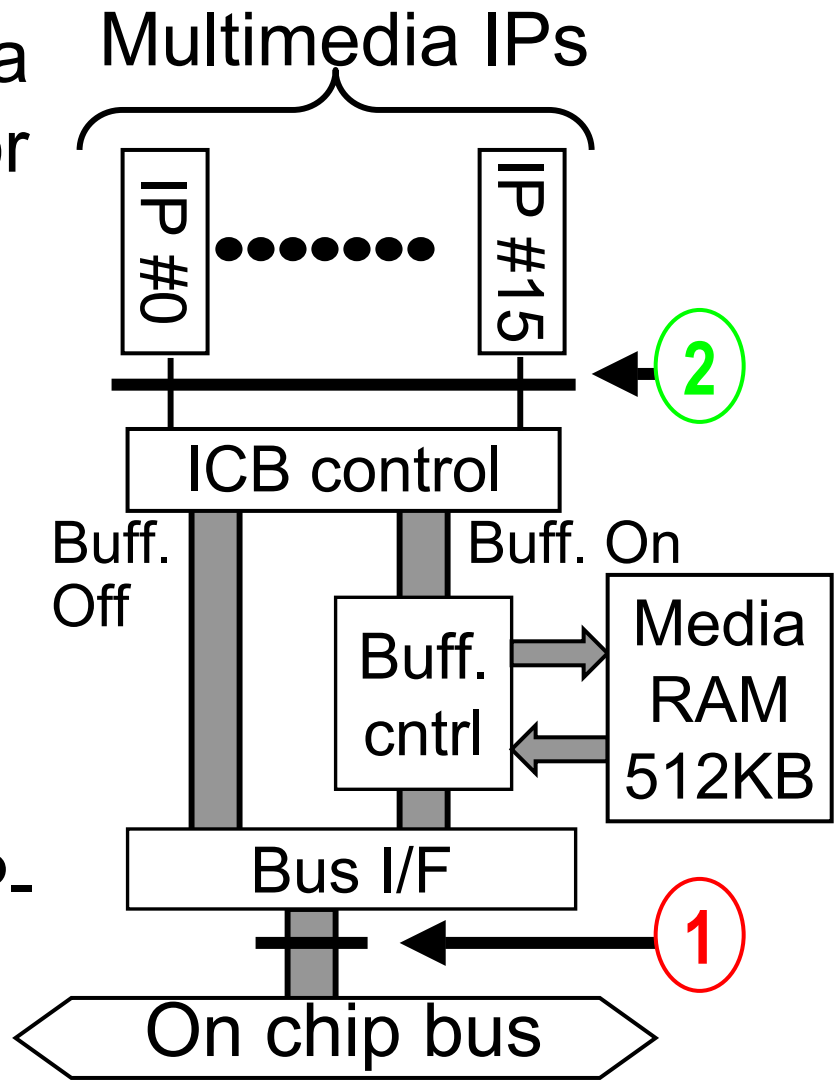
Inter-Connect Buffer (ICB) is the bus bridge that buffers data with 512 KBytes MediaRAM for inter-IP communication.

[Problem1]

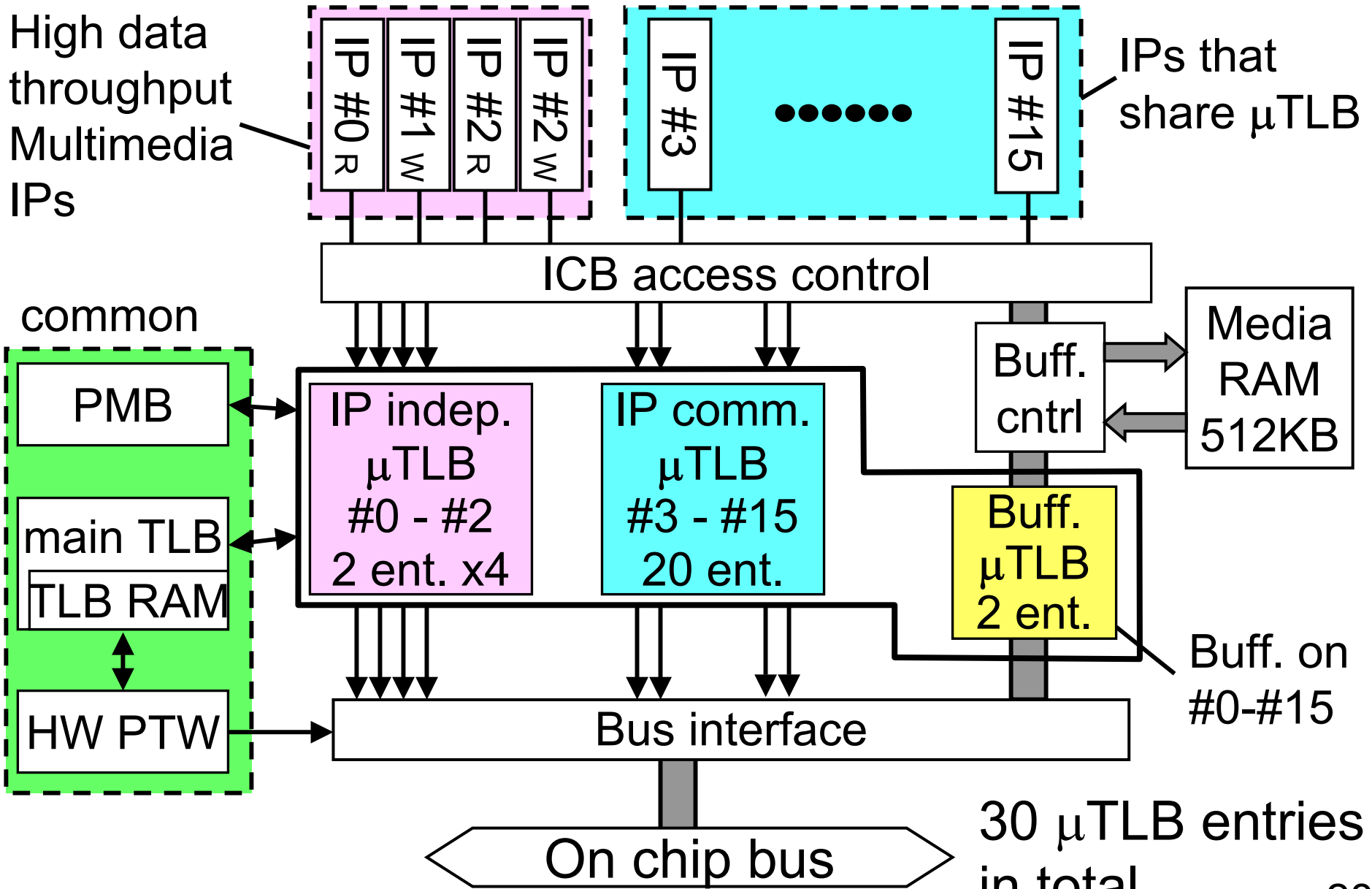
Inserting IP-MMU at bus I/F(1) may degrade performance.

[Problem2]

Inserting IP-MMU to each IP side(2) is costly because 16 IP-MMUs are needed for ICB.

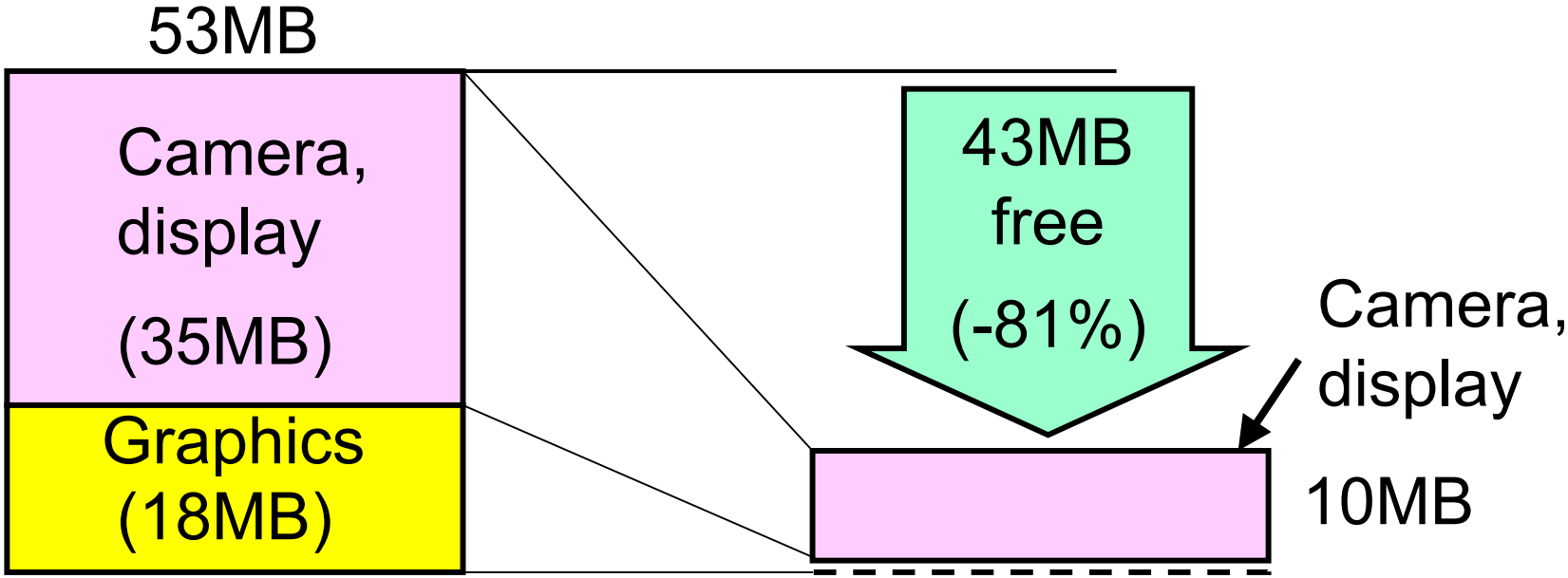


IP-MMU : Solution



IP-MMU: Evaluation results

- Statically allocated memory size



Note: All IP are used with IP-MMU.

- Performance evaluation
  Degradation is negligible.
  Video camcorder application performance:
  30 fps @D1(720x520) for MPEG4/AVC format on G3

Summary

- The SH-Mobile G3 integrates a dual-mode (3G/2G) baseband processor, an application processor, and a multimedia processor with 65nm LP for mobile phone.
- Hierarchical Power Domain architecture separates the chip into 20 power domains and reduces leakage in many use cases.
- Partial Clock Activation reduces power even in low power scenario. It achieved more than 40% reduction of chip power in long time music replay scene.
- IP-MMU enables HW-IPs to use physically fragmented memory. By using this, more than 80% of statically allocated memory can be freed in the actual system without performance degradation.