Test Infrastructure Design for Core-Based System-on-Chip Under Cycle-Accurate Thermal Constraints

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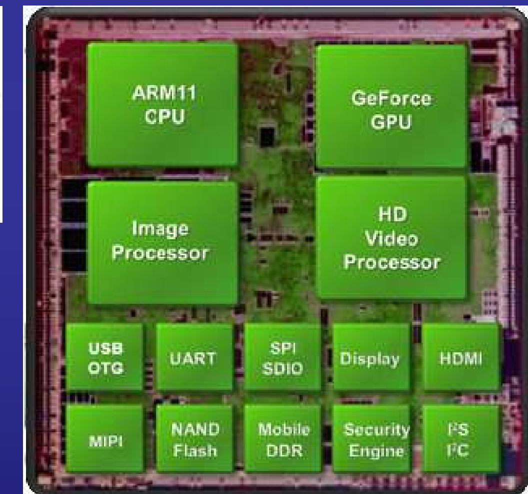
Outline

- Background
  - Core-based testing
  - Power / Heat-related problems during test
  - Limits of power-constrained SoC testing
- Related Works
- Objectives
- Proposed Method:
  - Fixed-TAM architecture
  - Scheduling techniques
  - Thermal model & cost function
- Experimental Results
- Summary

Core-Based System-on-Chip

- SoC (System-on-Chip):
  - One-chip system
  - Use pre-designed functional blocks called IP cores
  - Reduced design and manufacturing cost
    - IP design and test re-use

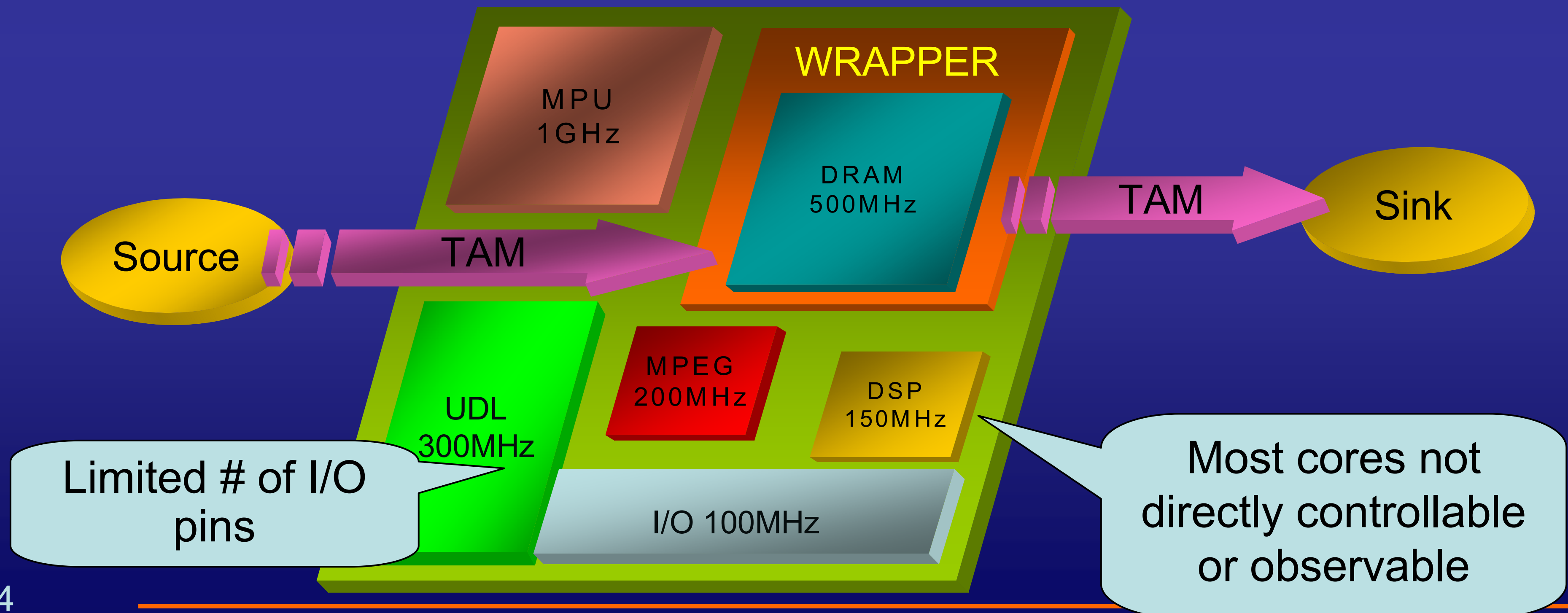


Courtesy of WindowsForDevices.com

- Test challenges
  - High test data volume
  - Limited access to internal circuitry
  - Long test application time (TAT)
  - High test power and temperature

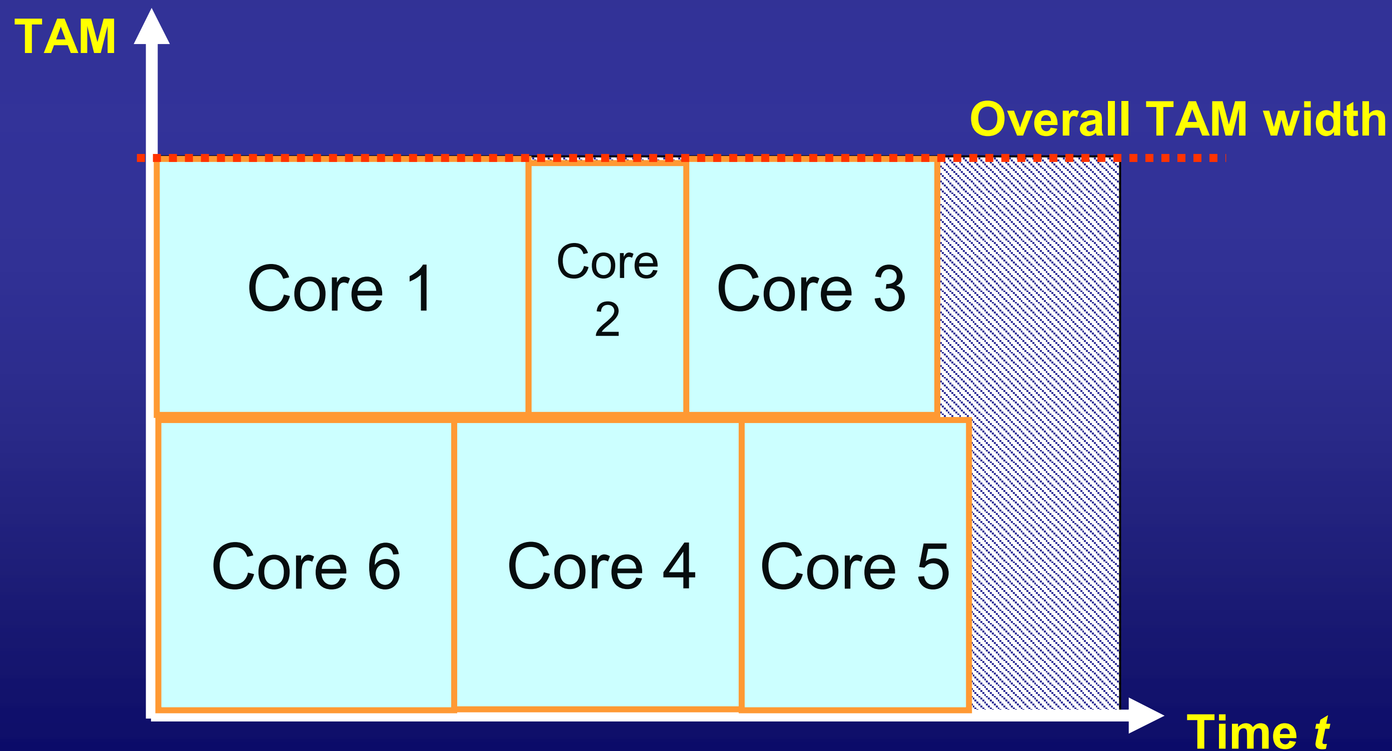
Design for Test (DFT) for SoCs

- TAM (Test Access Mechanism)
  - Dedicated test bus connecting test source/sink and core-under-test (CUT)
- Wrapper
  - Isolates CUT from other cores during test
  - Interfaces TAM & core
  - Enables test reuse



Test Scheduling

- Determine test sequence for each core
- Minimize test time under certain constraints
  - Power, TAM width, temperature, etc.
  - Parallel testing results in high test power and temperature

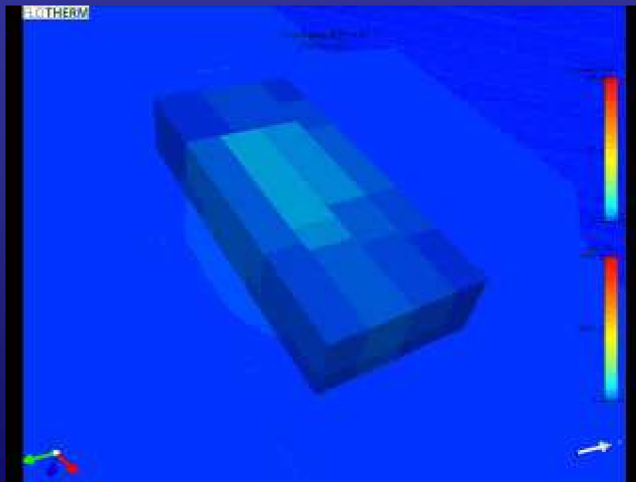


Power & Heat-related Issues During Test

- High test power dissipation
  - can cause chip damage or random errors
  - result in yield loss
- High power dissipation can cause overheating
  - every 20°C rise in temperature = approx. 5-6% timing delay
  - chip packaging are designed for worst case *typical* application

Limits of Power-constrained SoC Testing

- Ignore non-uniform spatial power distribution across chip
  - layout, core proximity affects temperature
  - can't ensure thermal-safety
- Ignore effect of time on temperature



Testing 5 cores in parallel

1 P=100	2 P=100	3 P=100
4 P=100	5 P=100	6 P=100
7 P=100	8 P=100	9 P=100

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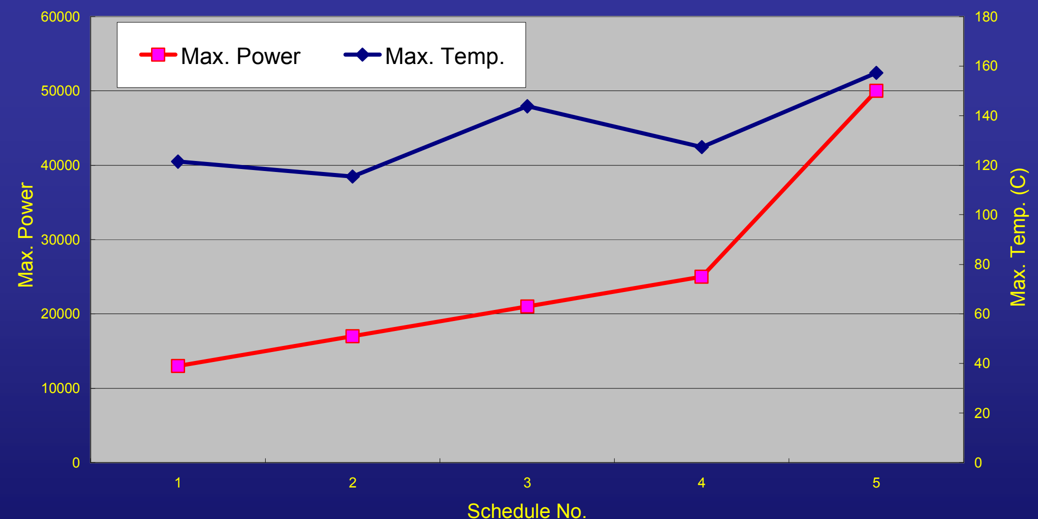
Max. Power and Temp. for p93791 SoC



*Results using HotSpot temp. simulator (Skadron et al., ISCA'03)

Objectives

- Given an SoC, test data and maximum allowable temperature,

  Propose a thermal-safe test architecture design and test scheduling methodology
  - the given thermal constraint is satisfied at any time during test
  - the test application time is minimized

Related Works

- Thermal-safe test scheduling (*Rosinger et al., DATE'05*)
  - group cores with fixed wrappers into test sessions
  - minimize temperature per session
- Uniform heat distribution (*Liu et al., DFT'05*)
  - use layout information to determine wrapper configuration and test schedule
- Test set partitioning and interleaving (*He et al., DFT'06*)
  - partition test set when temperature constraint is exceeded
  - interleave test partitions sequentially, allow other cores to cool down

Characteristics of Related Works

- Use constant power per core
- Ignore effects of active cores on non-active cores
- Do not optimize both the TAM and Wrapper configuration

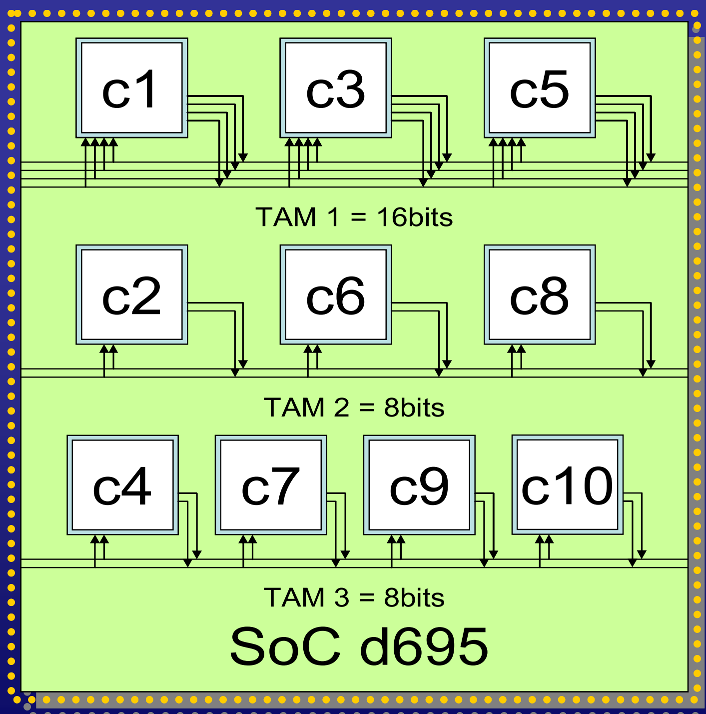
- Thermal-safe TAM / Wrapper Co-optimization (*Yu et al., ATS'07*)
  - use cycle-accurate power profiles per core wrapper configuration
  - consider heat exchange across all cores and test sequence via heat dissipation paths
  - first work to optimize TAM and Wrapper under a thermal constraint

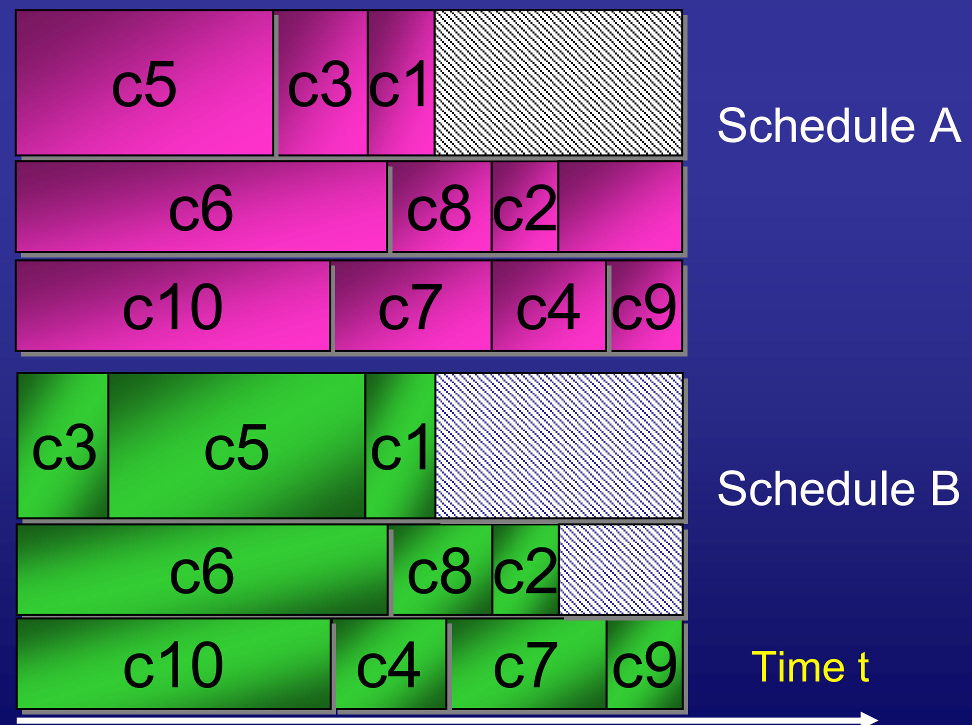
Research Contributions

- Improvements over work done for ATS`07
  - Allow schedule reshaping
  - Allow dynamic test partitioning and interleaving
  - Allow insertion of bandwidth matching circuitry
  - Find solutions under much tighter temperature constraints
- Preserve advantages of ATS`07 work
  - Cycle-accurate power and temperature profiles
  - Consider inter-core temperature effects
  - Optimize TAM & Wrapper architecture

Target Test Architecture

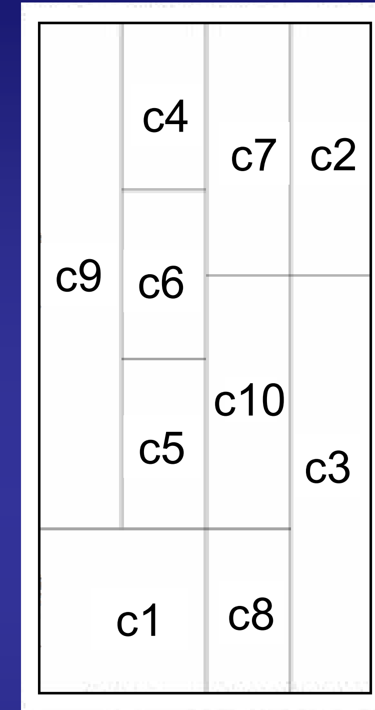
- Characteristics:
  1. TAM has fixed partitioning
  2. Cores are assigned to only one TAM partition
  3. Cores in the same TAM scheduled sequentially, order is variable
  4. Cores in different TAMs can be scheduled in parallel

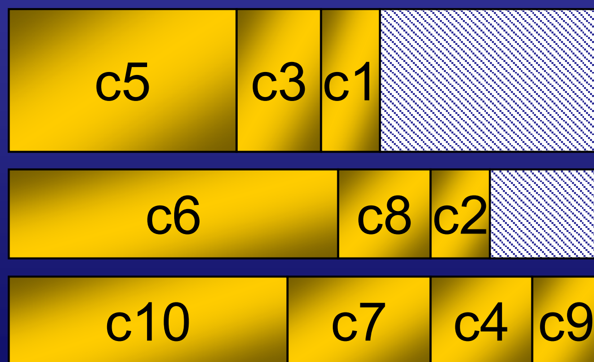




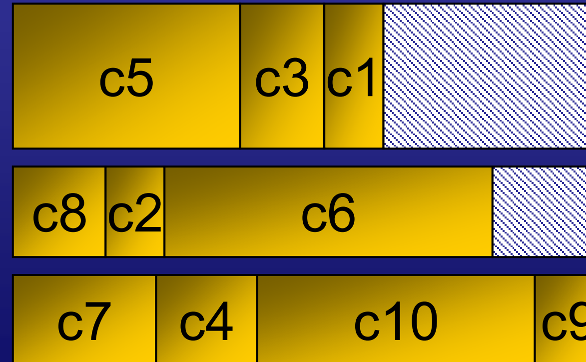
Test Schedule Reshaping, Partitioning & Interleaving

- Test schedule reshaping
  - Reconfigure schedule to minimize temperature of target core
  - Ex. Avoid testing hot cores in parallel and in sequence
- Test partitioning and interleaving
  - Partition test before temperature exceeds constraint

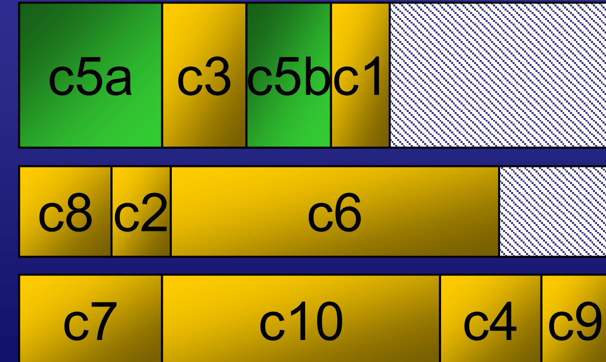




Max. Temp = 110°C



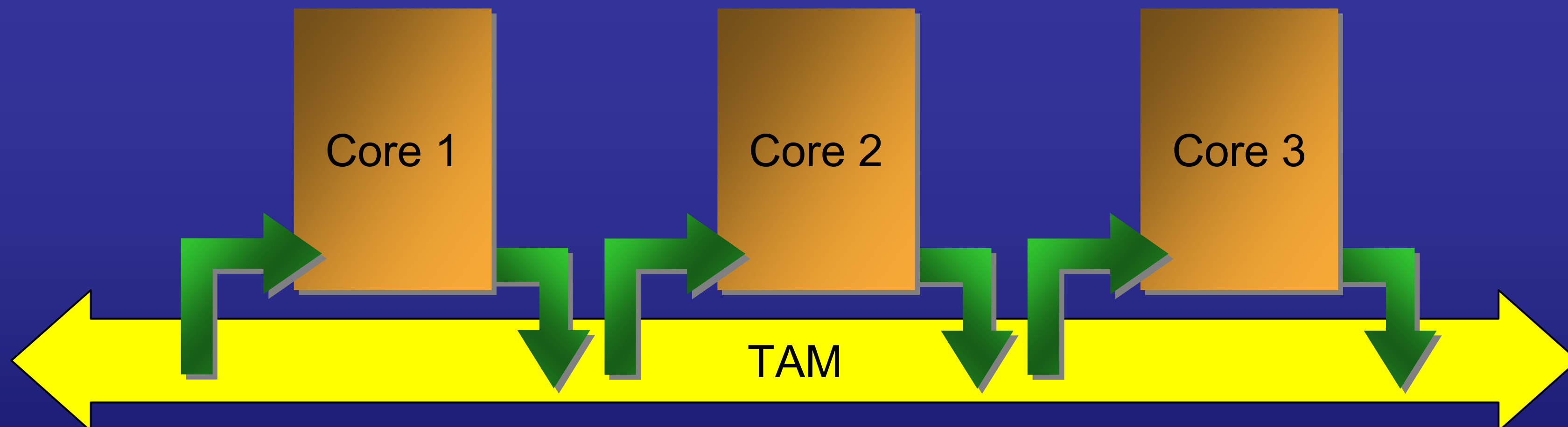
Max. Temp = 100°C



Max. Temp = 95°C

Bandwidth Matching

- Frequency throttling
  - lower scan frequency => lower power
- Add bandwidth matching circuitry to TAM partition
  - 2*TAM width, ½ freq. => temperature reduction ideally w/o TAT increase



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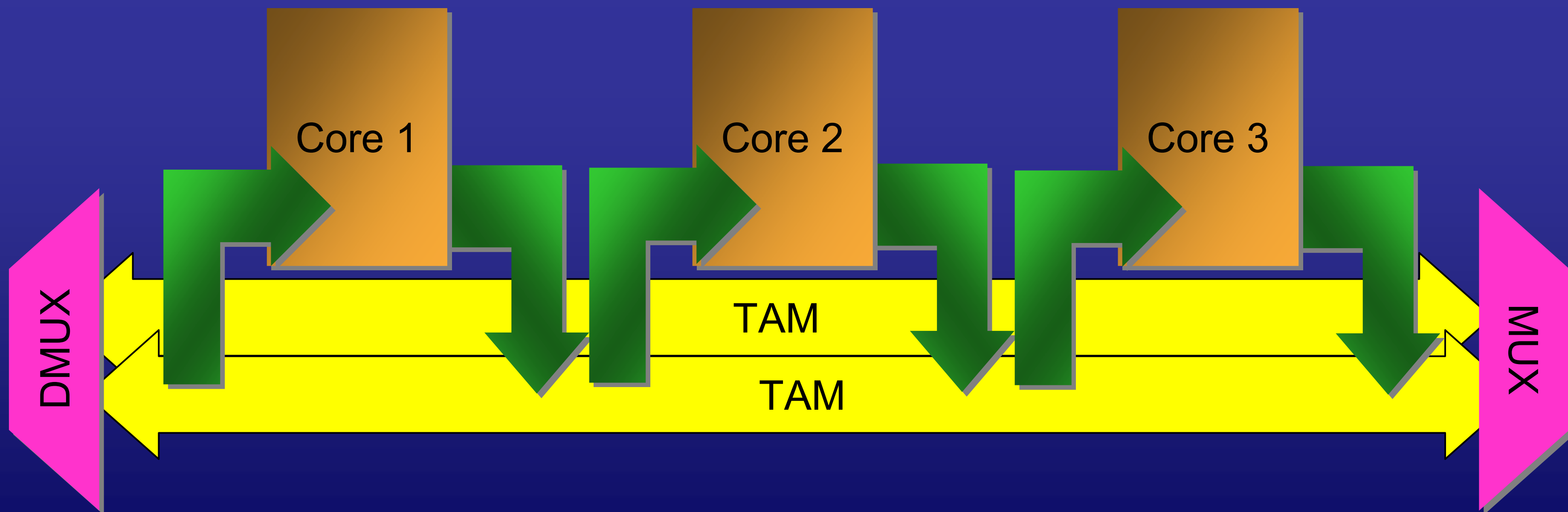
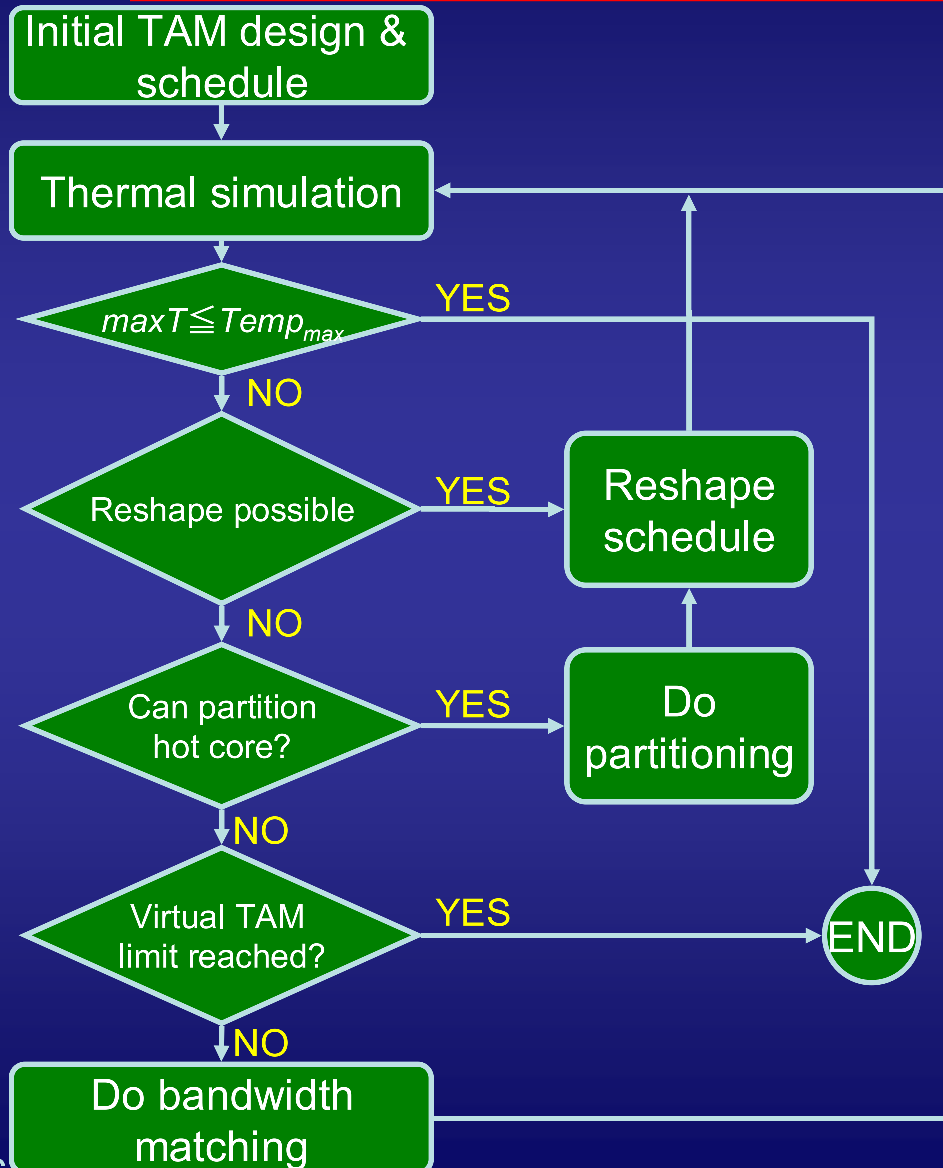


Proposed Method Flow

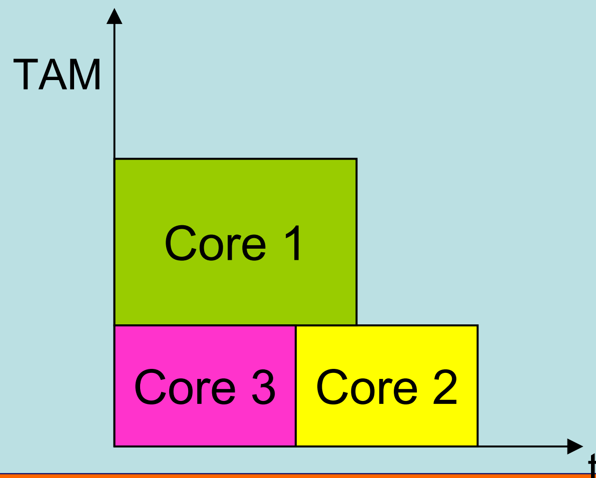


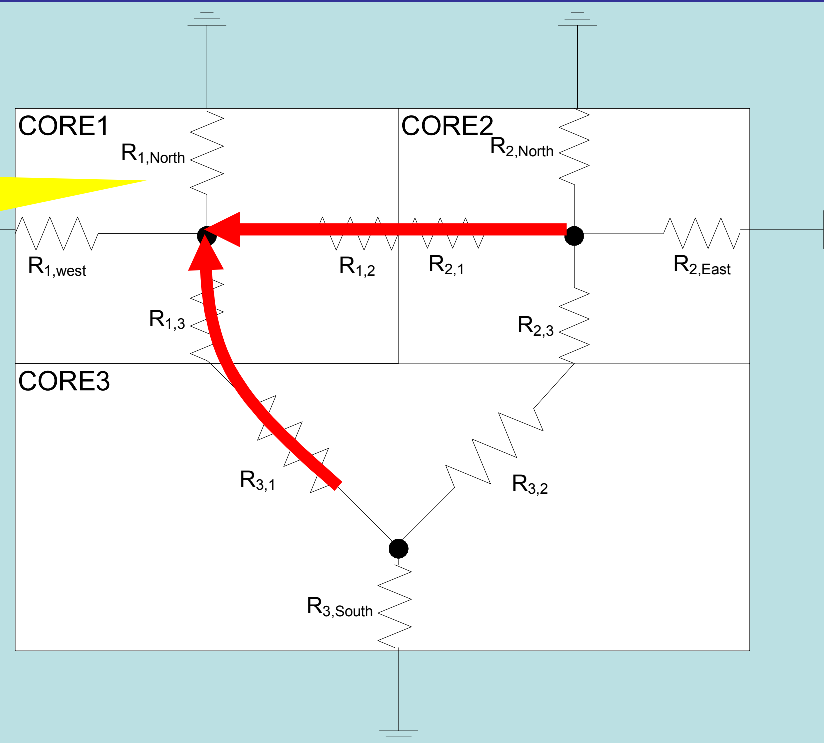
- Scheduling is NP-Hard
  - need heuristic scheduling algorithm
- Thermal simulation is time consuming
  - need simplified thermal model
  - need simple thermal cost function

Thermal Model

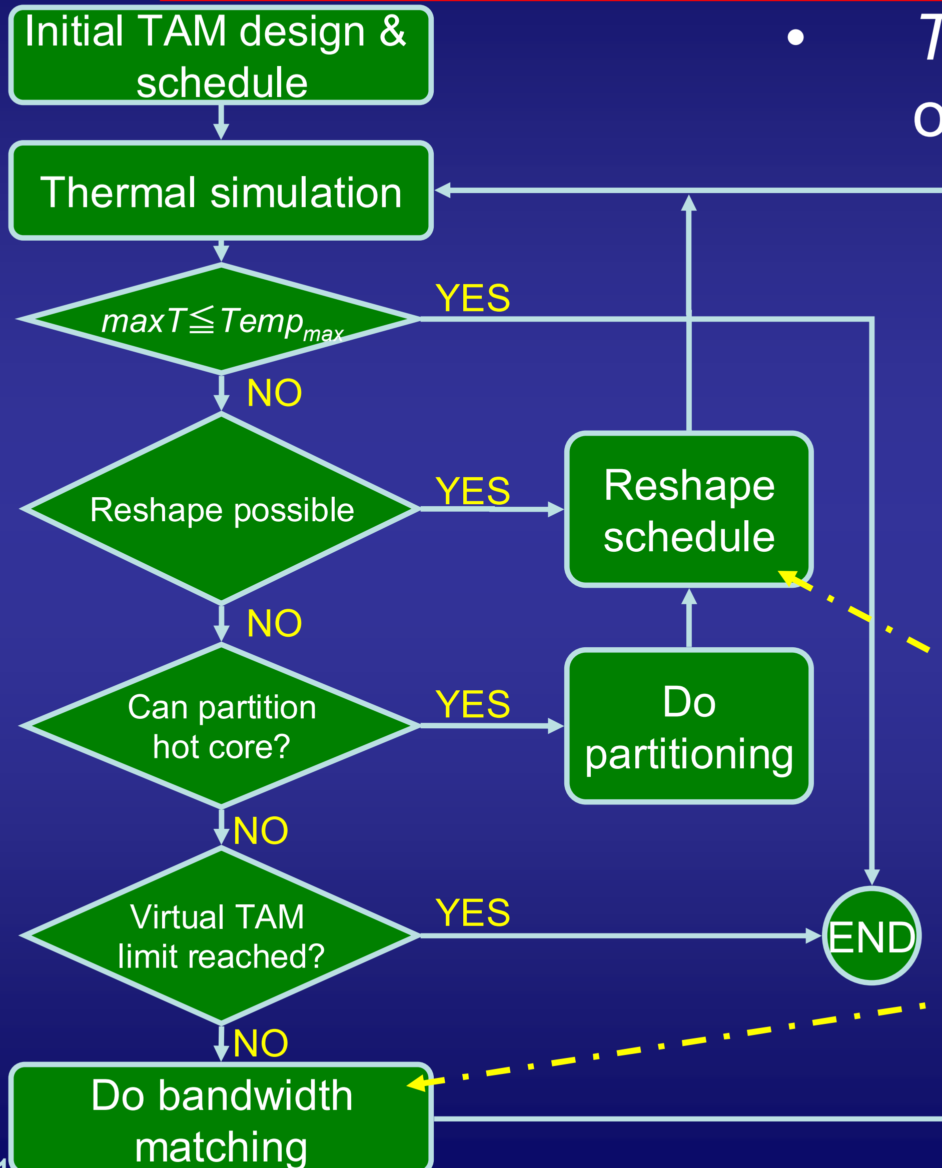
- Model SoC as a network of thermal resistances
  - first proposed by P. Rosinger, K. Chakrabarty, et.al (*DATE'05*)
  - takes advantage of thermal and electrical duality
  - only consider lateral thermal resistances

•Models lateral heat flow
•More heat flow from cores
= higher temperature





Thermal Cost Function



- *$Tcont_j(c_i)$:* thermal contribution of Core *j* to Core *i*

$$Tcont_j(c_i) = \frac{R_{ji}}{R_{TOT,j}} \times Pavg_j \times \frac{Trel_{ji}}{TAT_i}$$

where : R_{ji} : Lateral thermal resistance from core c_j to c_i, ($R_{ii} = 0$)

$R_{TOT,j}$: Total lateral resitance of core c_j

$Pavg_j$: Average power dissipation of c_j

$Trel_{ji}$: Relative test time of c_j and c_i

Minimize thermal contribution to hotspot core

Reset cost values and revert to initial schedule

Experimental Setup

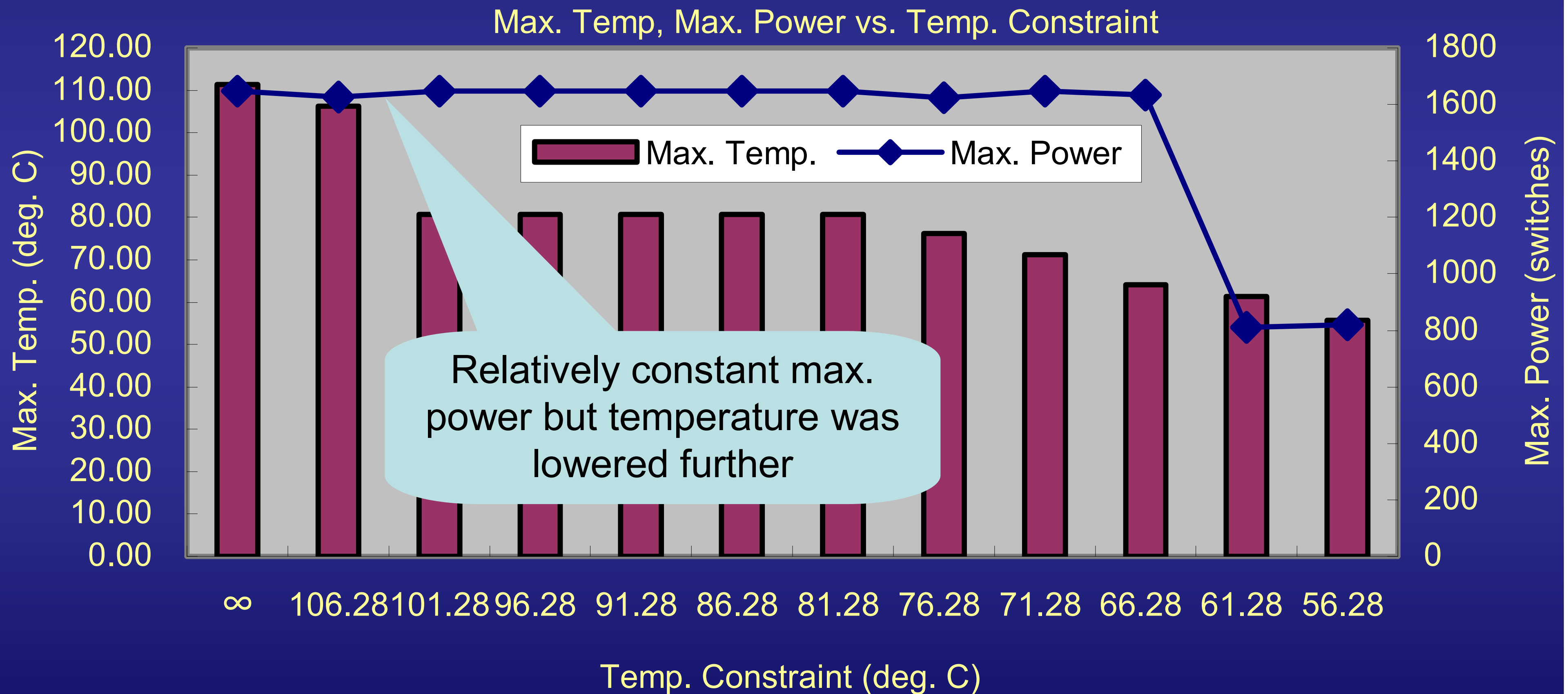
- Benchmark *ITC'02* SoCs
  - d695, p22810 with hand-crafted layouts
  - cycle-accurate power profiles from Samii et al.

  ("Cycle- Accurate Test Power Modeling and its Application to SoC Test Scheduling," *Proc. of IEEE International Test Conference (ITC)*, pp. 1-10, 2006)

- Scheduling parameters
  - *TAM* = 16, 24, 32, 64
  - *Tmpmax* : initially set to max temperature of schedule under no power & thermal constraint
    - decreased by 5°C intervals

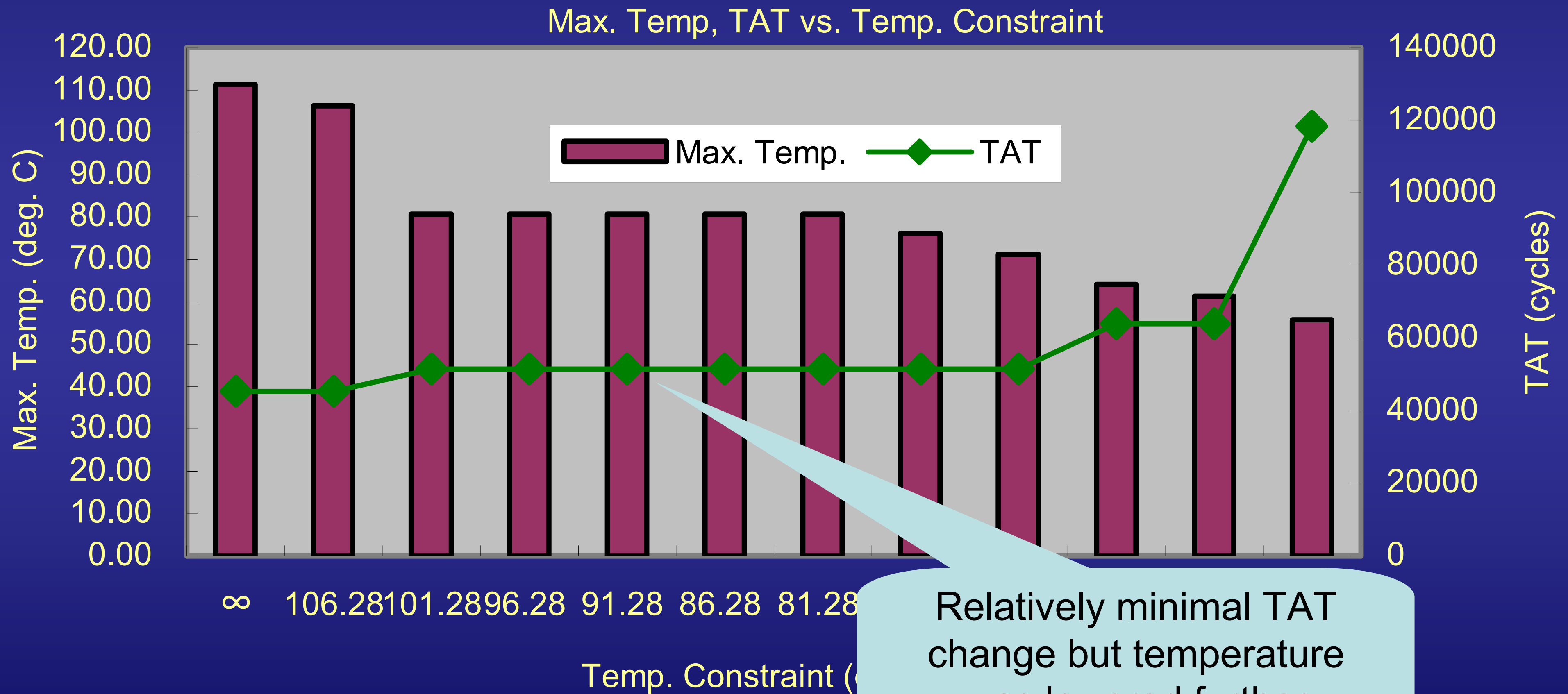
Max. Temperature & Power vs. Temp. Constraint

- d695 with TAM = 16bits



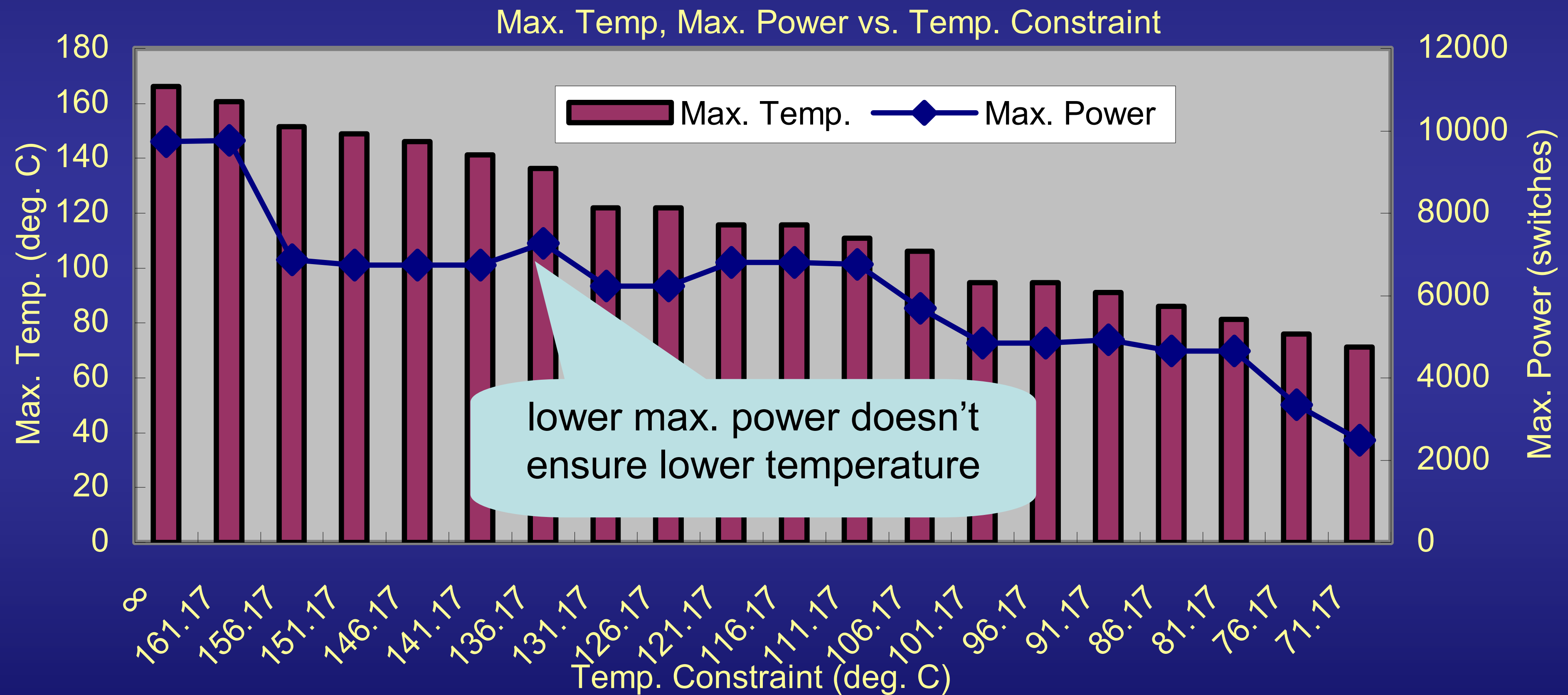
Max. Temperature & TAT vs. Temp. Constraint

- d695 with TAM = 16bits



Max. Temperature & Power vs. Temp. Constraint

- p22810 with TAM = 32bits



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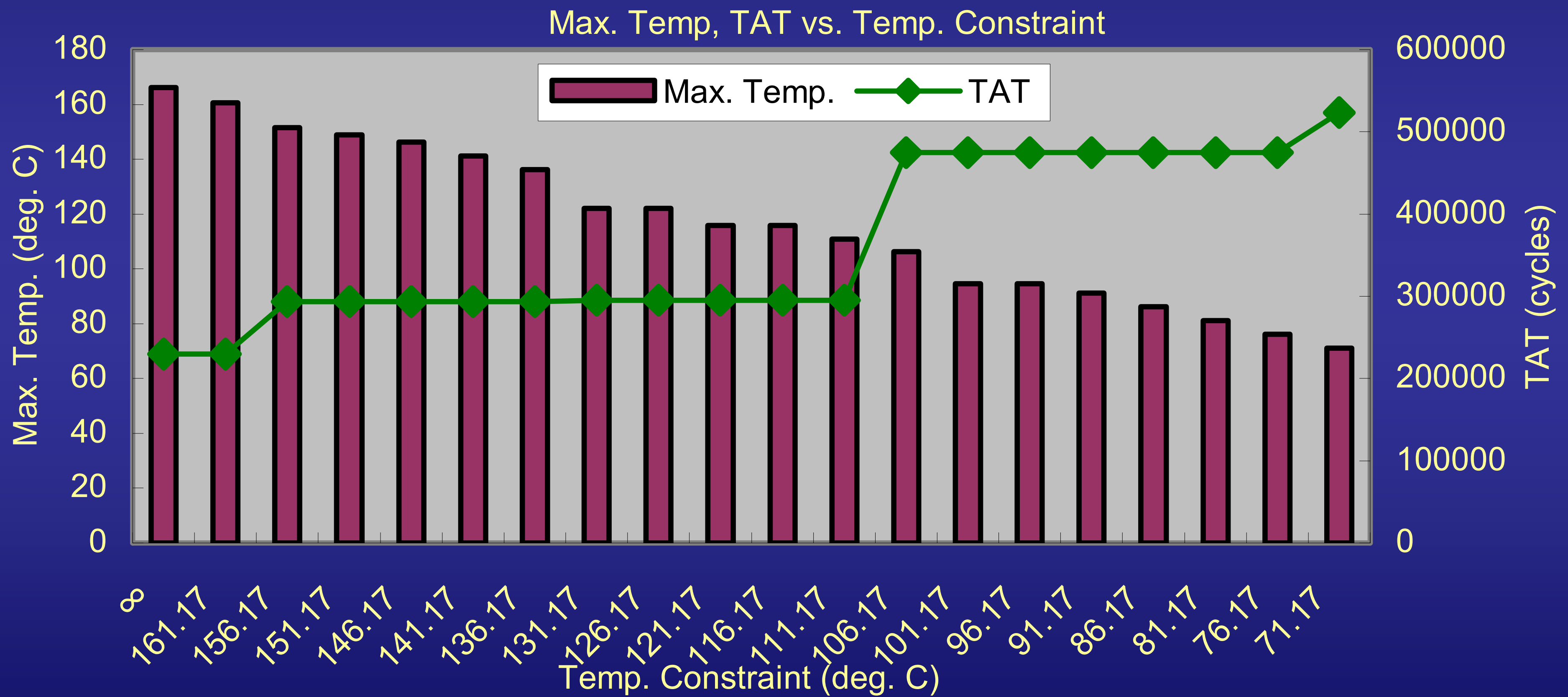

Minimum Temperature Comparison

Max. 40% reduction in minimum temperature

	TAM=16			TAM=24		
SoC	*ATS'07*	*Proposed*	*dTAT(%)*	*ATS'07*	*Proposed*	*dTAT(%)*
d695	92.79C	55.8C	-152	91.49C	58.46C	-46
p22810	133.02C	77.71C	-53	110.1C	102.29C	7

	TAM=32			TAM=64		
SoC	*ATS'07*	*Proposed*	*dTAT(%)*	*ATS'07*	*Proposed*	*dTAT(%)*
d695	77.15C	69.91C	16	84.71C	80.59C	26
p22810	109.36C	71.17C	-98	107.25C	92.79C	-20

Summary

- Studied the impact of test-set partitioning, bandwidth matching on thermal-aware TAM / Wrapper optimization and test scheduling
- Algorithm based on computationally tractable thermal-cost model makes thermal simulation more useable; ensures thermal safety
- The results show that:
  - method allows more flexibility to trade-off temperature and TAT while minimizing TAT increase
  - method provides solutions even under tight temperature constraints, including situations where previous work fails to find a solution