TOSHIBA
Leading Innovation

Challenges to EDA System from the View Point of Processor Design and Technology Drivers

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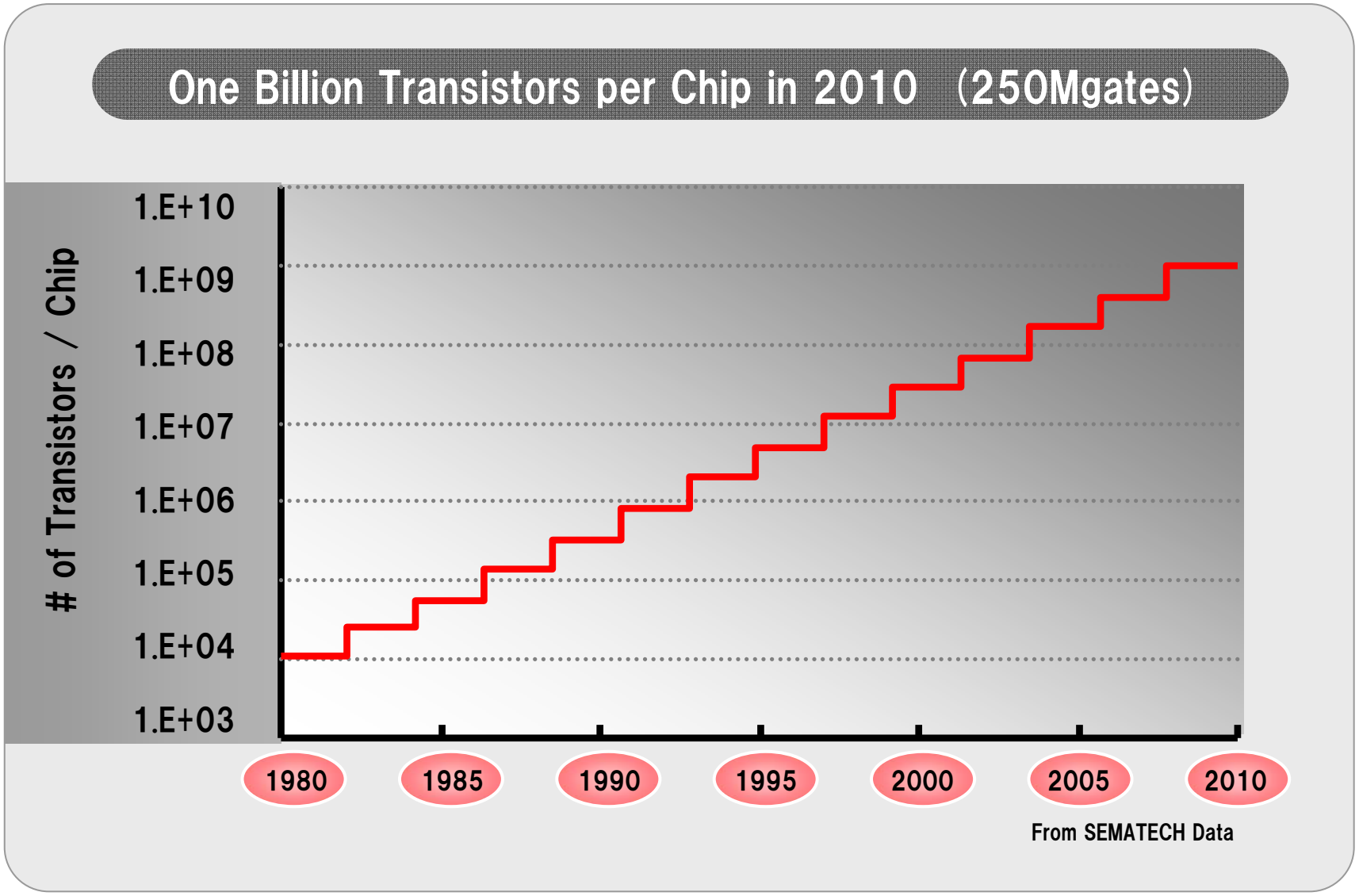
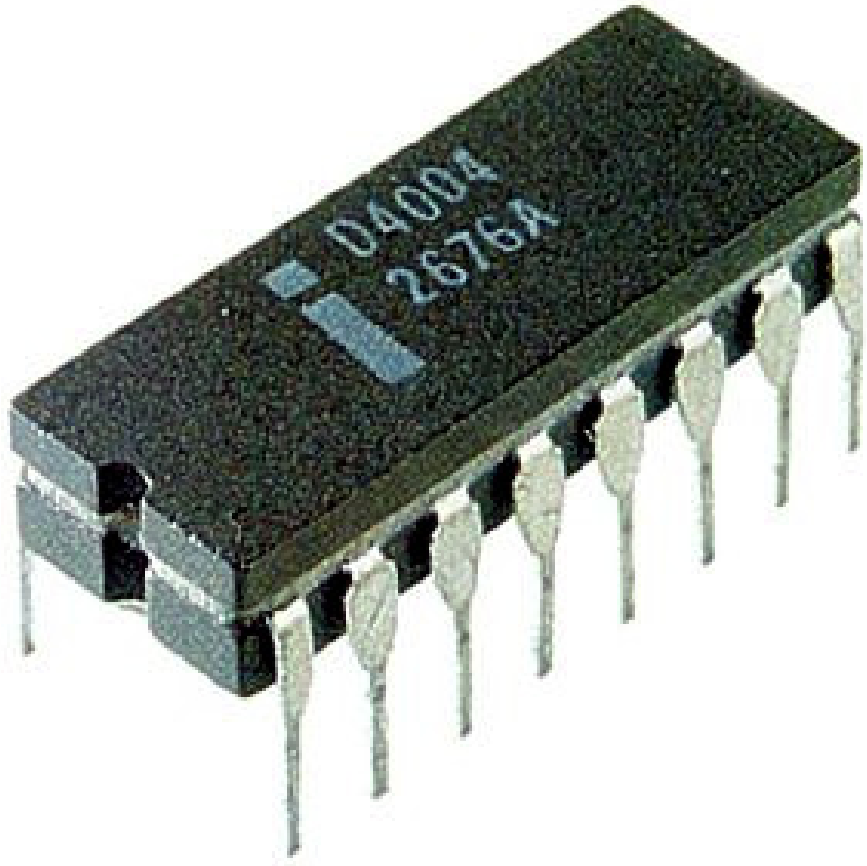
Contents

Still Semiconductor Roadmap is Working : Moore's Law



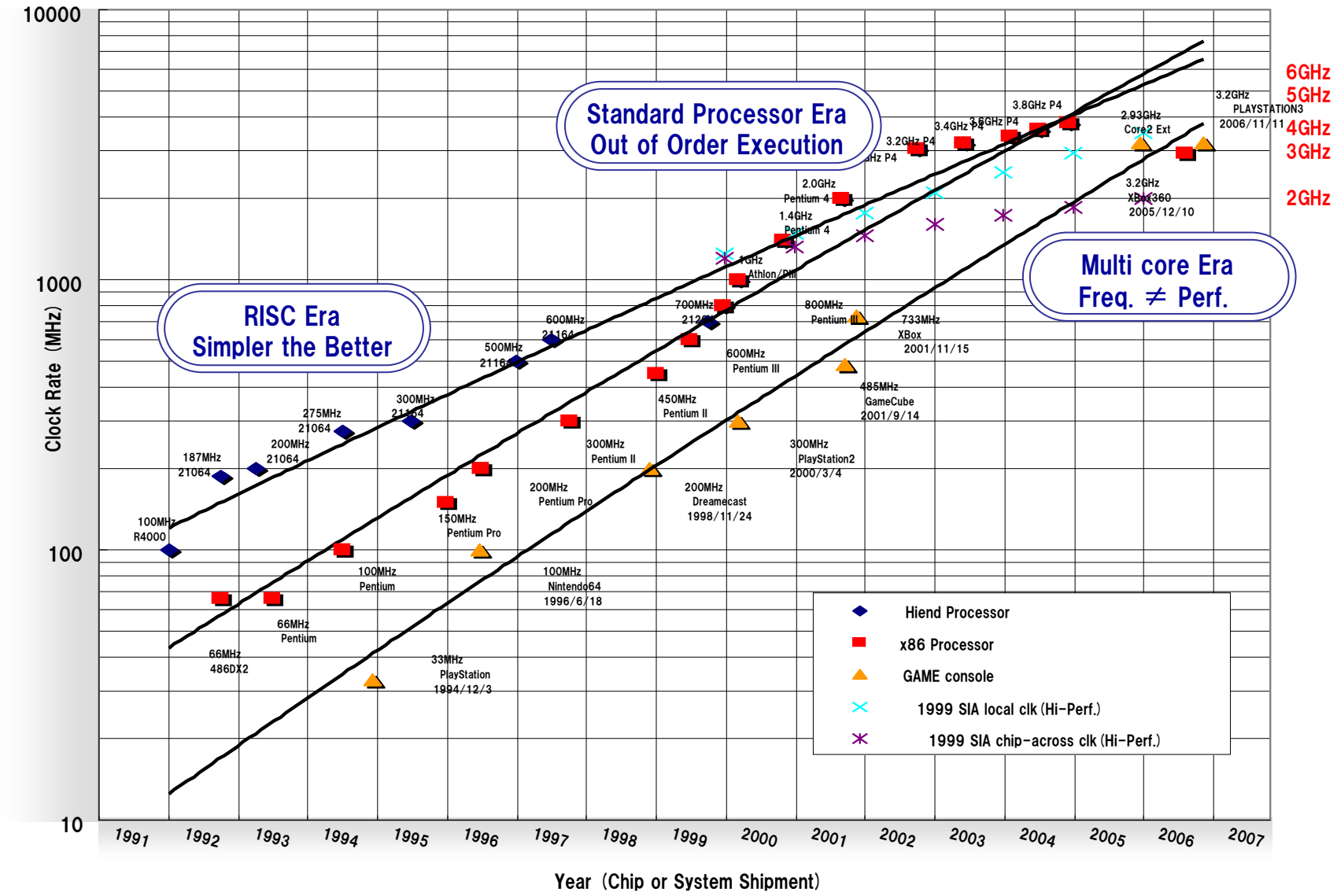
First Micro Processor was born in 1971

- **Intel 4004**
- **DIP16P, Address bus 12 bit, Data bus 4 bit**
- **Clock 741KHz**
- **P-MOS 10um**
- **Tr. 2300**
- **11/15/1971**

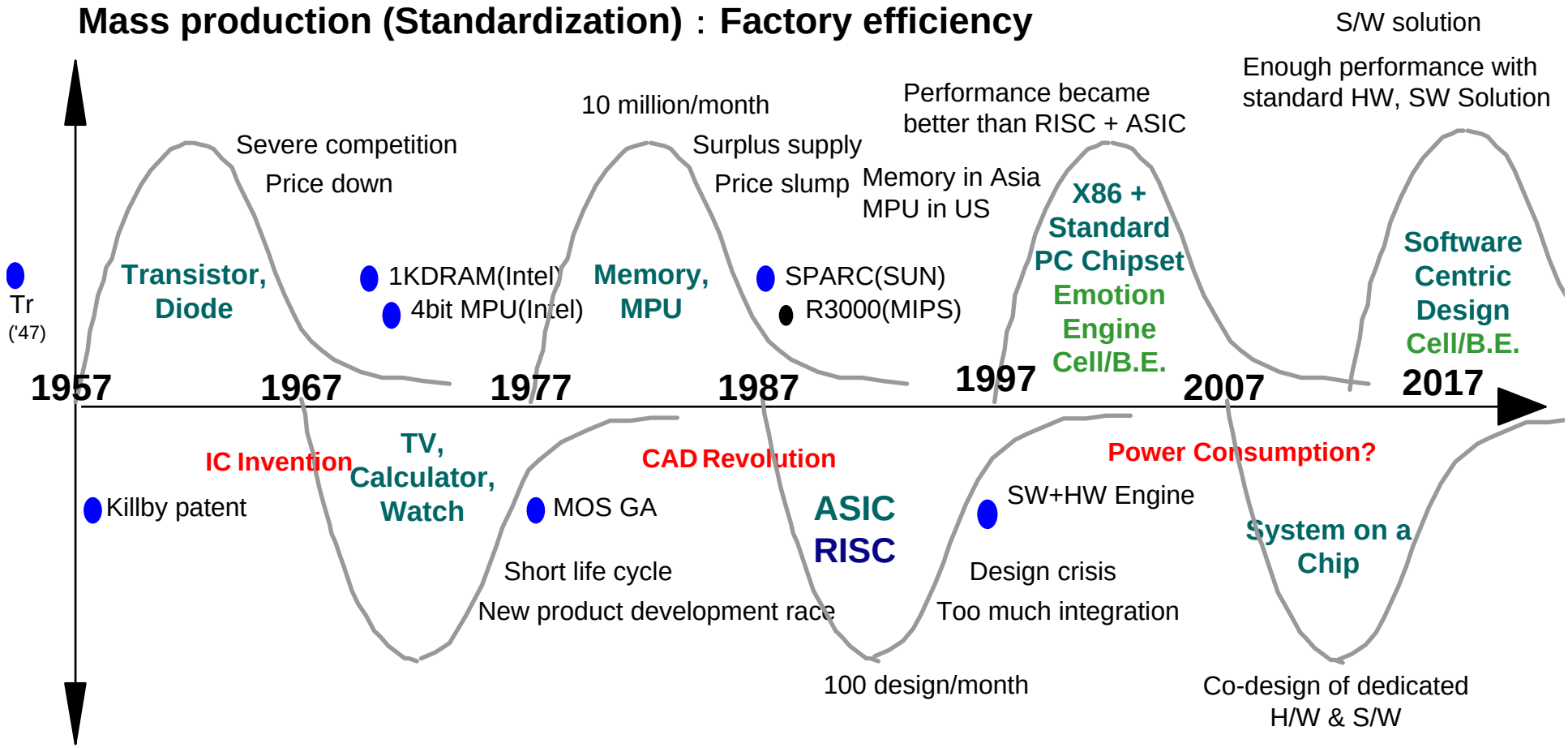


From : Wikipedia

Processor Clock Rate per Year



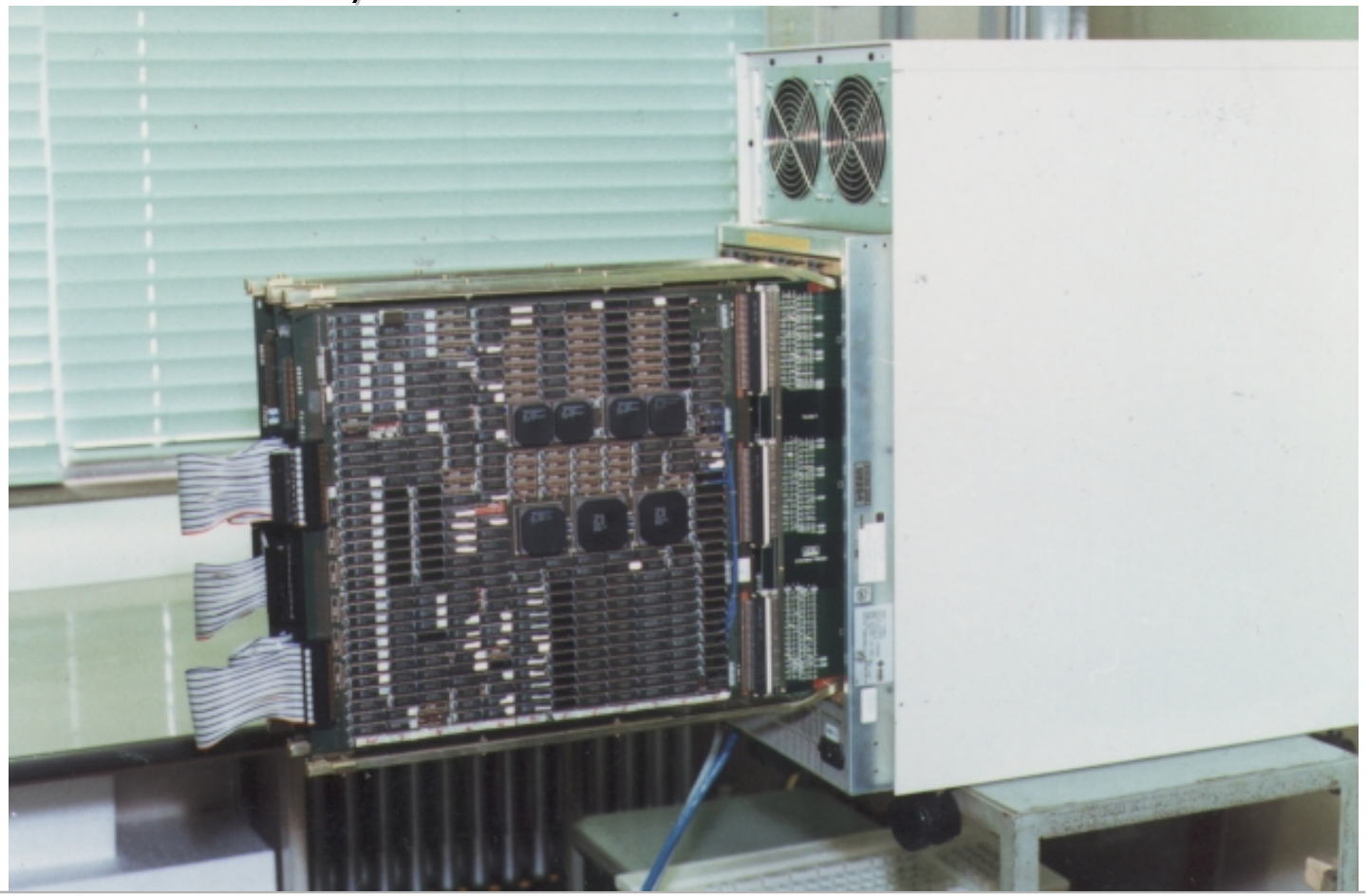
Waves to Standardization and Customization



Source : Makimoto's Wave

AI Workstation (1986)

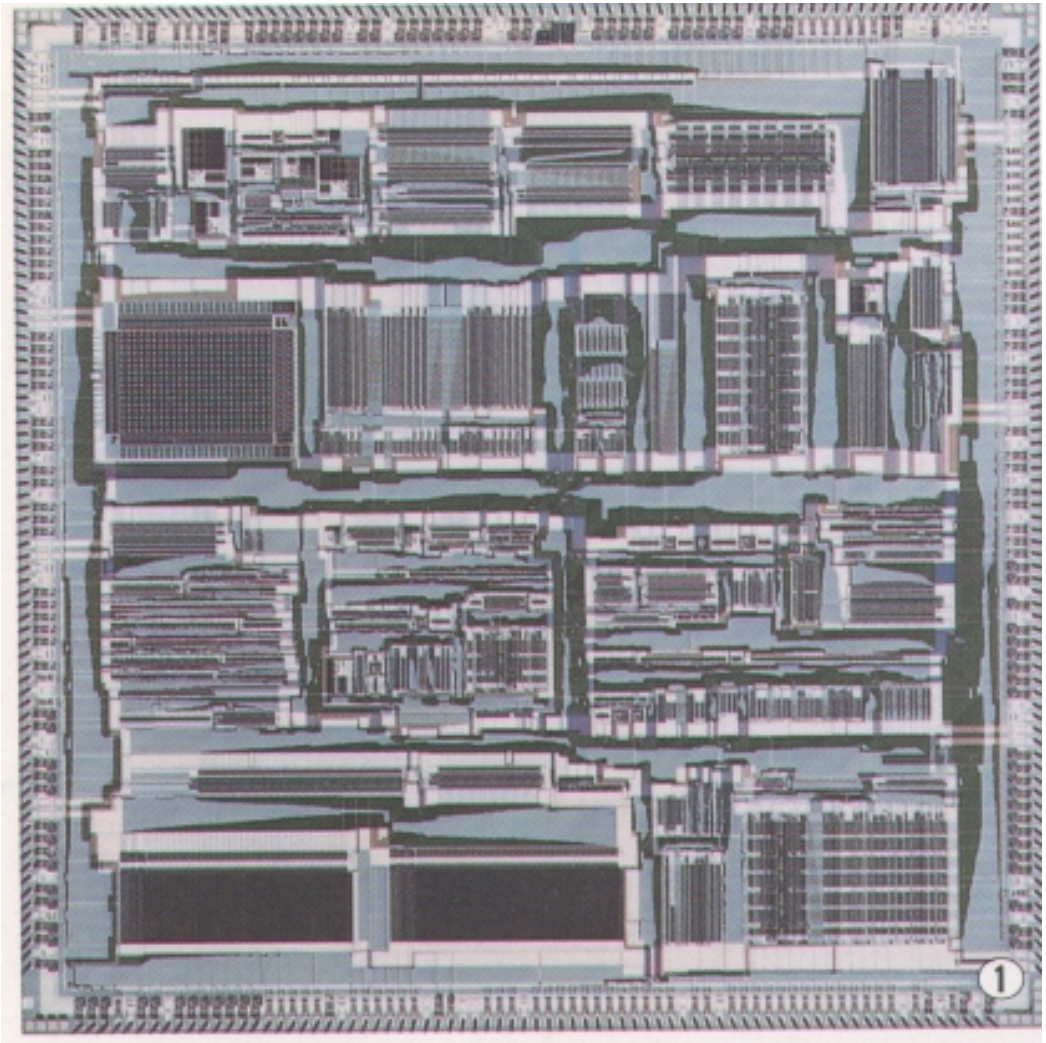
- Maybe the last paper and pencil based Design!
- Processor was a board based
- About 100 sets were sold, and reasonable revenue



AI Processor Chip (1988)

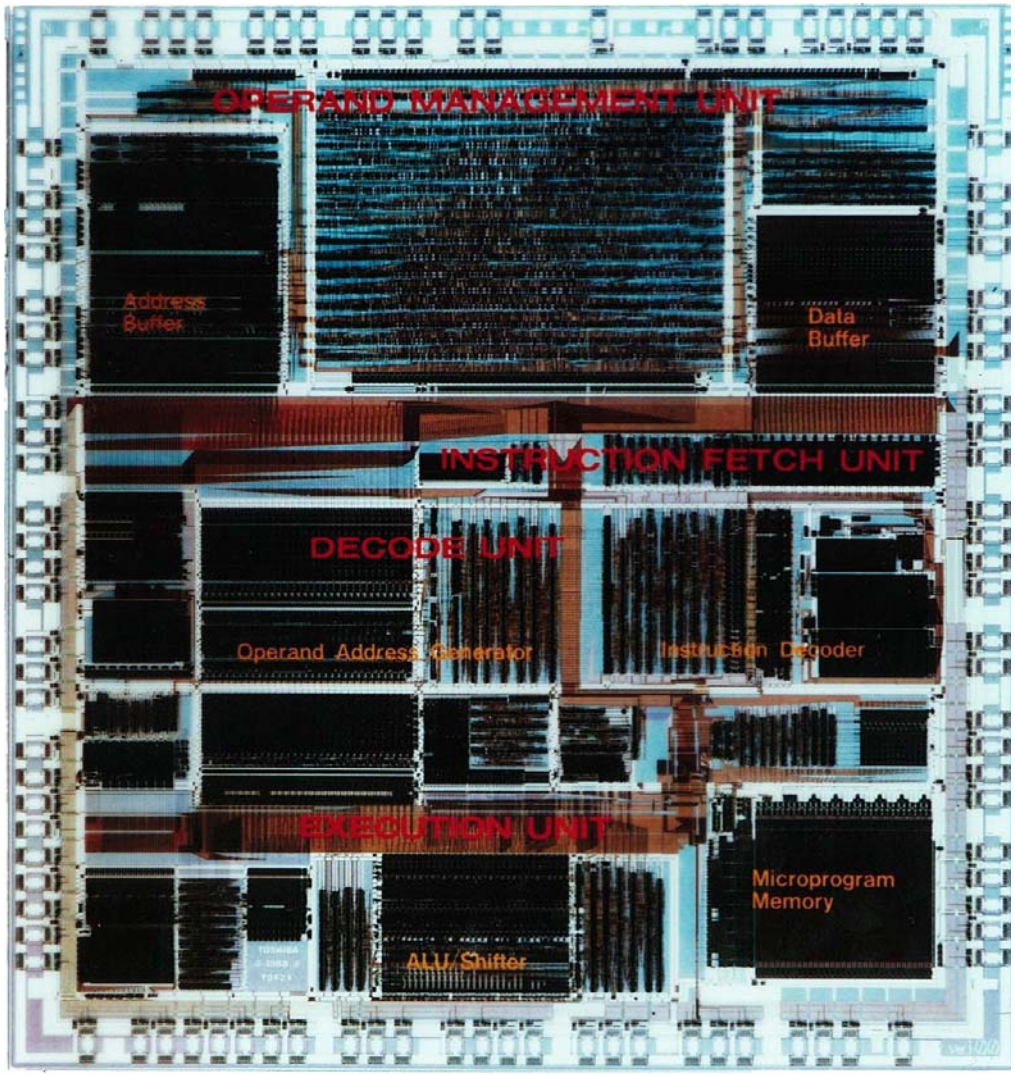
•Silicon Compiler “Genesil” was Used

Performance	12 MIPS @Dhrystone
Registers	32bit × 32
Buses	32bit × 2
Bus Cycle	1 Clock min
Clock Freq.	16MHz Max
Process	1.2um 2 Layer Metal CMOS
Tr.Cnt	113K
Package	299pin PGA



First TRON Processor TX1 (1988)

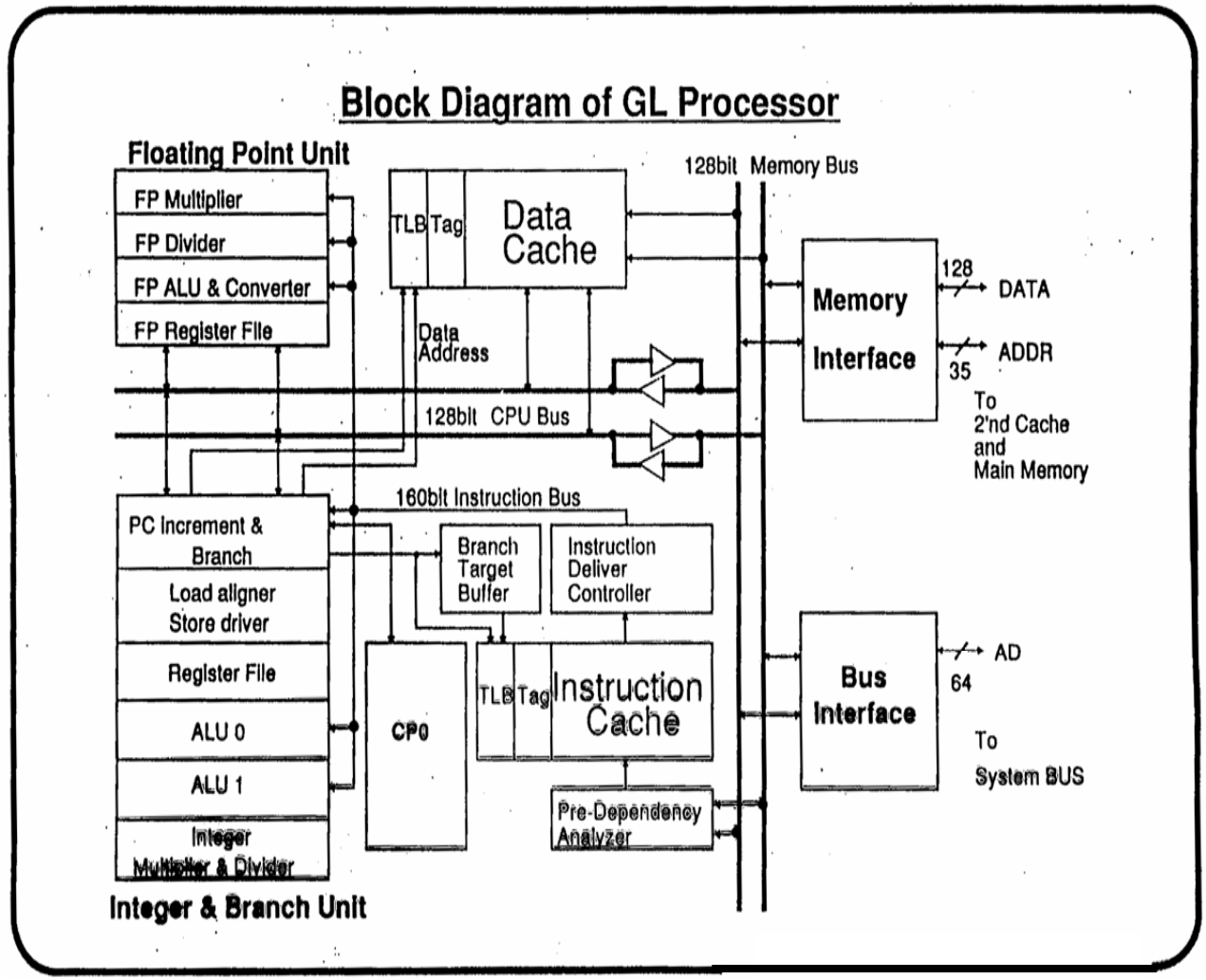
- **Proprietary HDL (H^2DL) was used**



Performance	5 MIPS
Registers	32bit × 16
Buses	32bit × 2
Bus Cycle	2 Clock min
Clock Freq.	25MHz Max
Process	1.0um 2 Layer Metal CMOS
Package	155-pin PGA

Incomplete GL Processor (1990)

- **Proprietary HDL (H^2DL) was used**

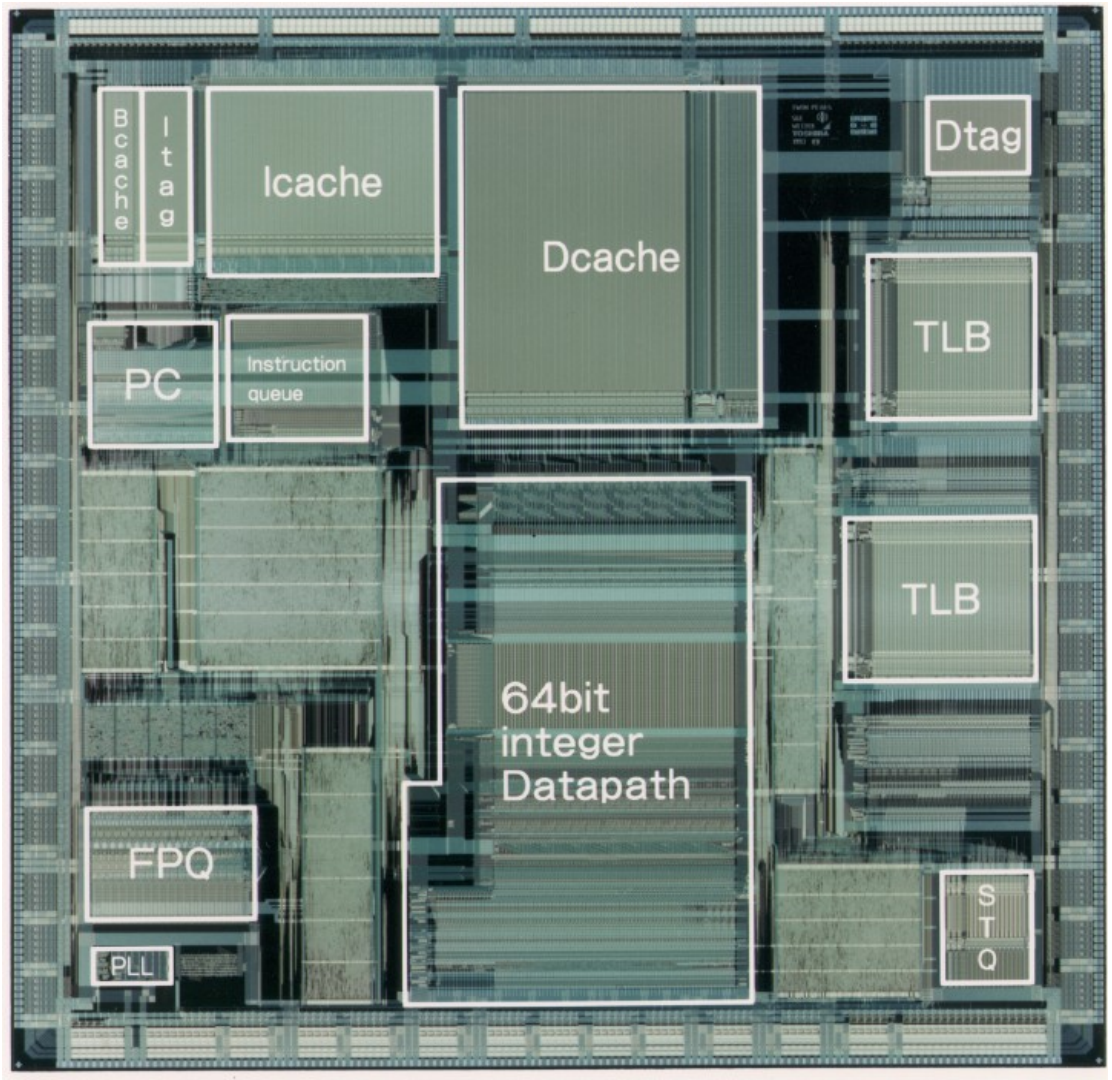


Freq.	65MHz
Inst.	4 Way SuperScalar
Dhry.	100MIPS
Linpack	66MFlops(Single) 35MFlops(Double)
Power	3.3V/5~6W
Process	0.5 μ mCMOS
Package	448pin PGA
Tr.cnt	2.5M

RISC Processor R8000 (1993)

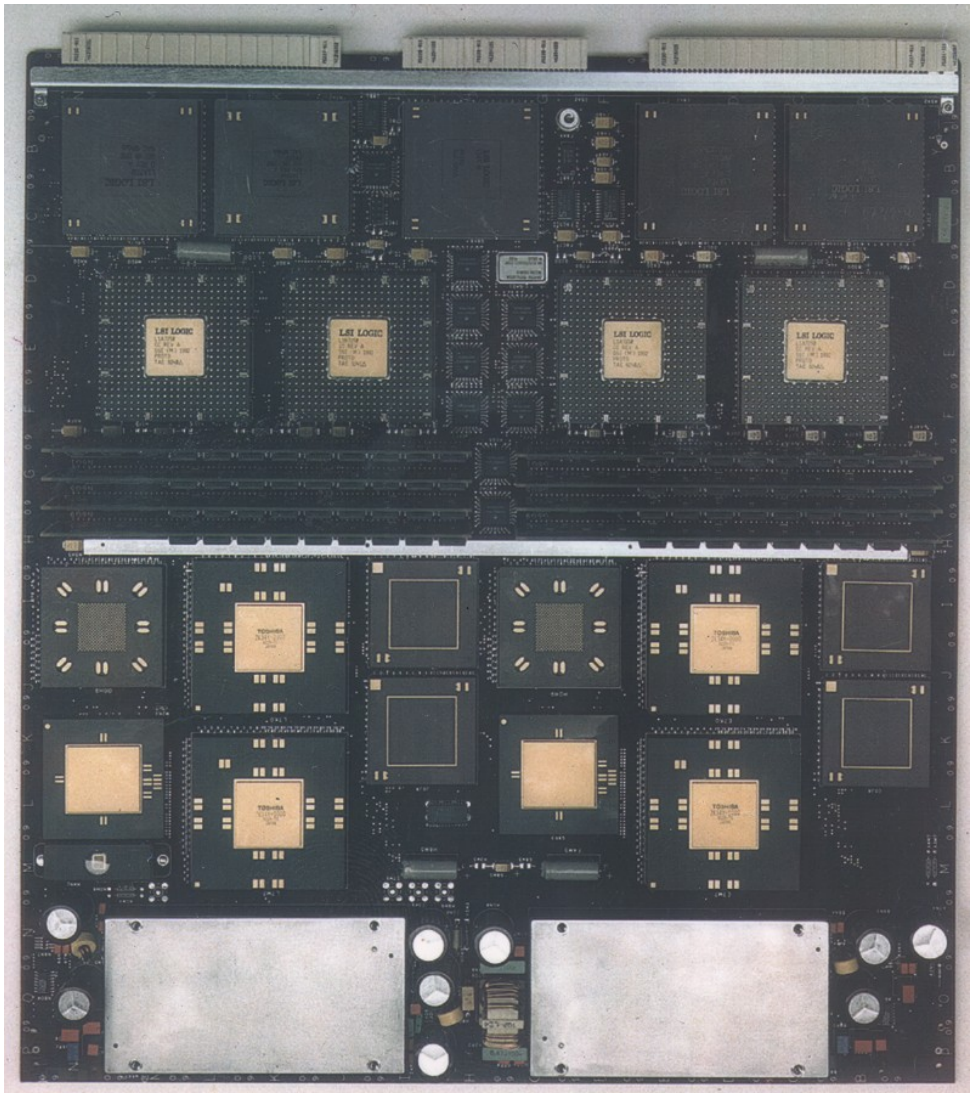
- **Verilog was used**

Jointly developed with Silicon Graphics Inc.



R8000 Based Computer Board

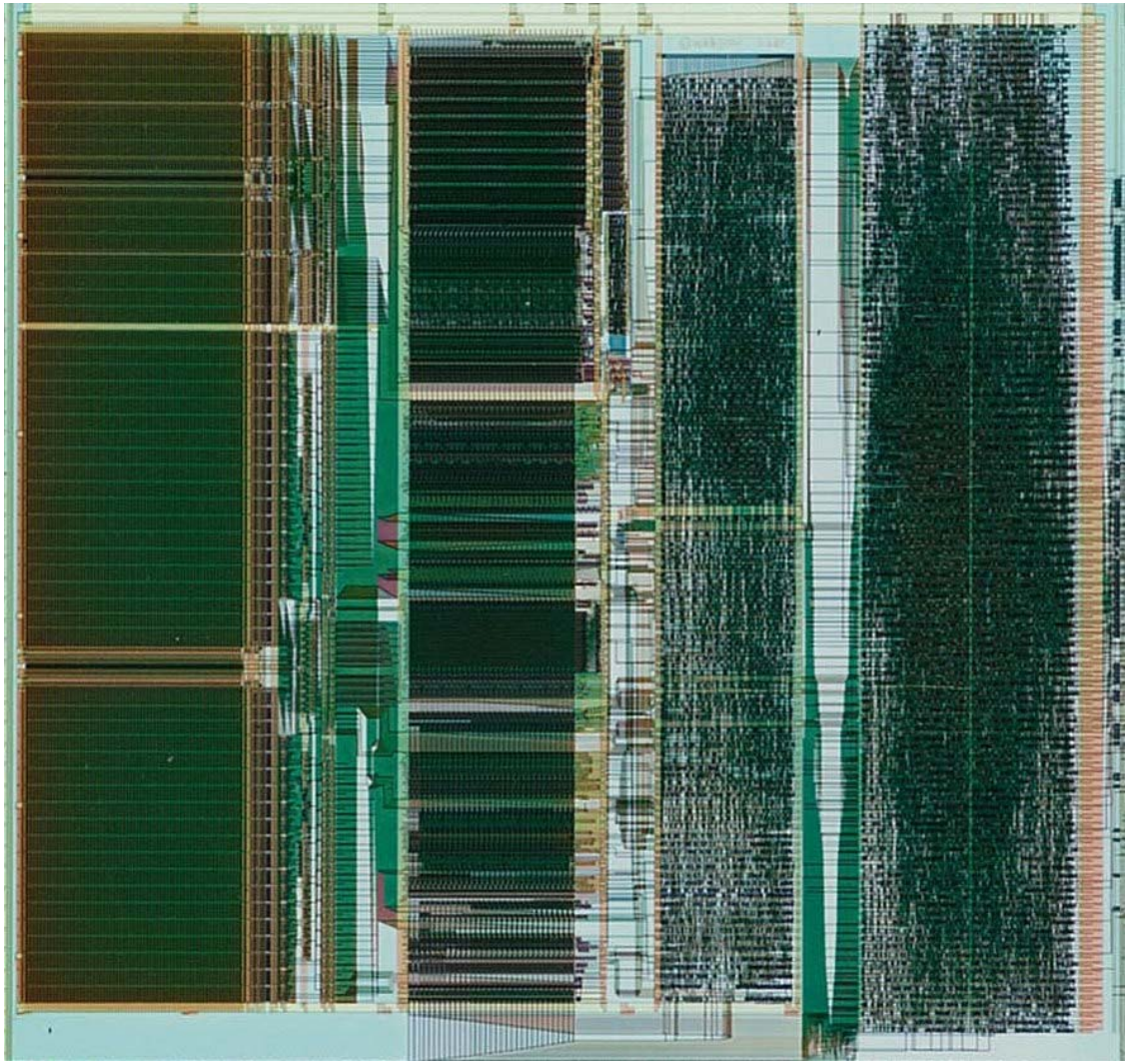
Designed by Silicon Graphics Inc.



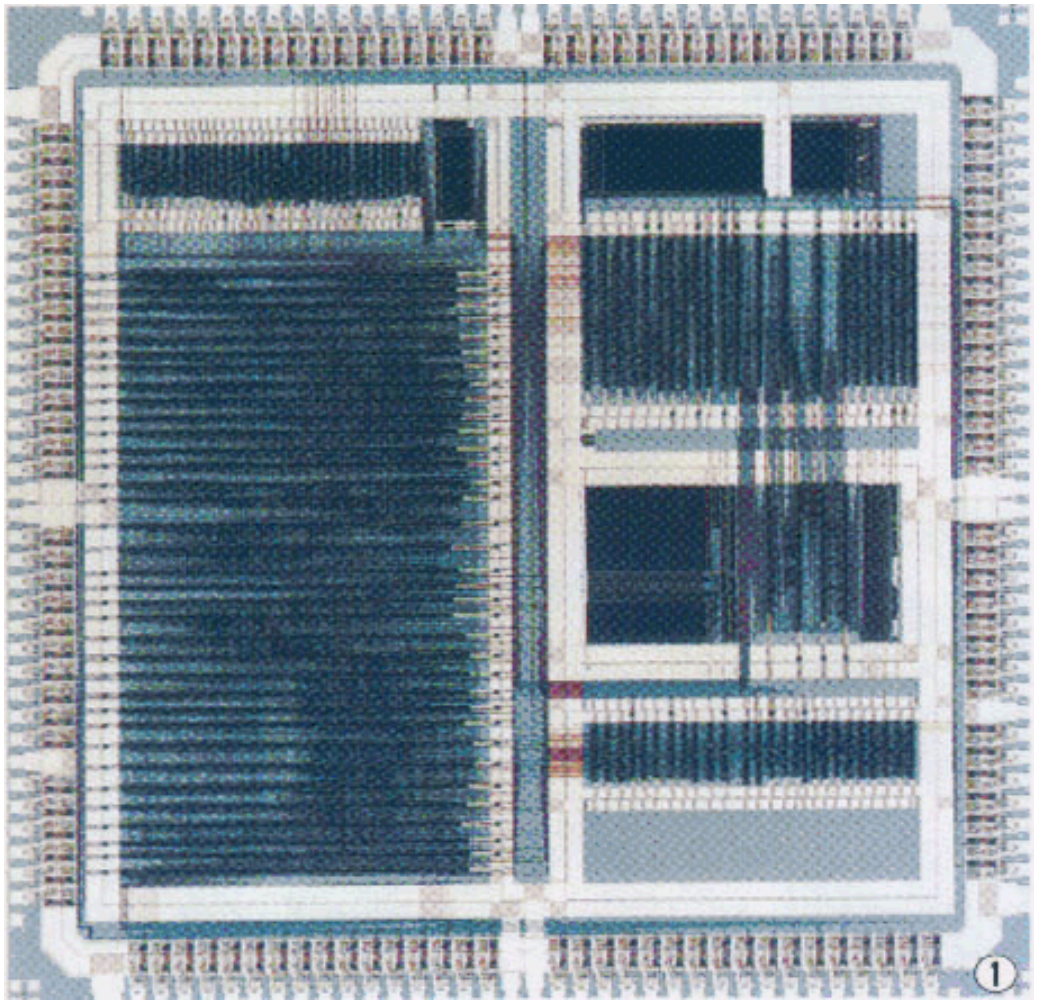
Embedded RISC Processor TX39(1995)

- **Verilog was used**

- First Embedded RISC
- 32bit MIPS Architecture
- 40MHz/43MIPS
- 500mw
- 4KB I cache / 1KB D cache
- 4K page MMU (32 entry)

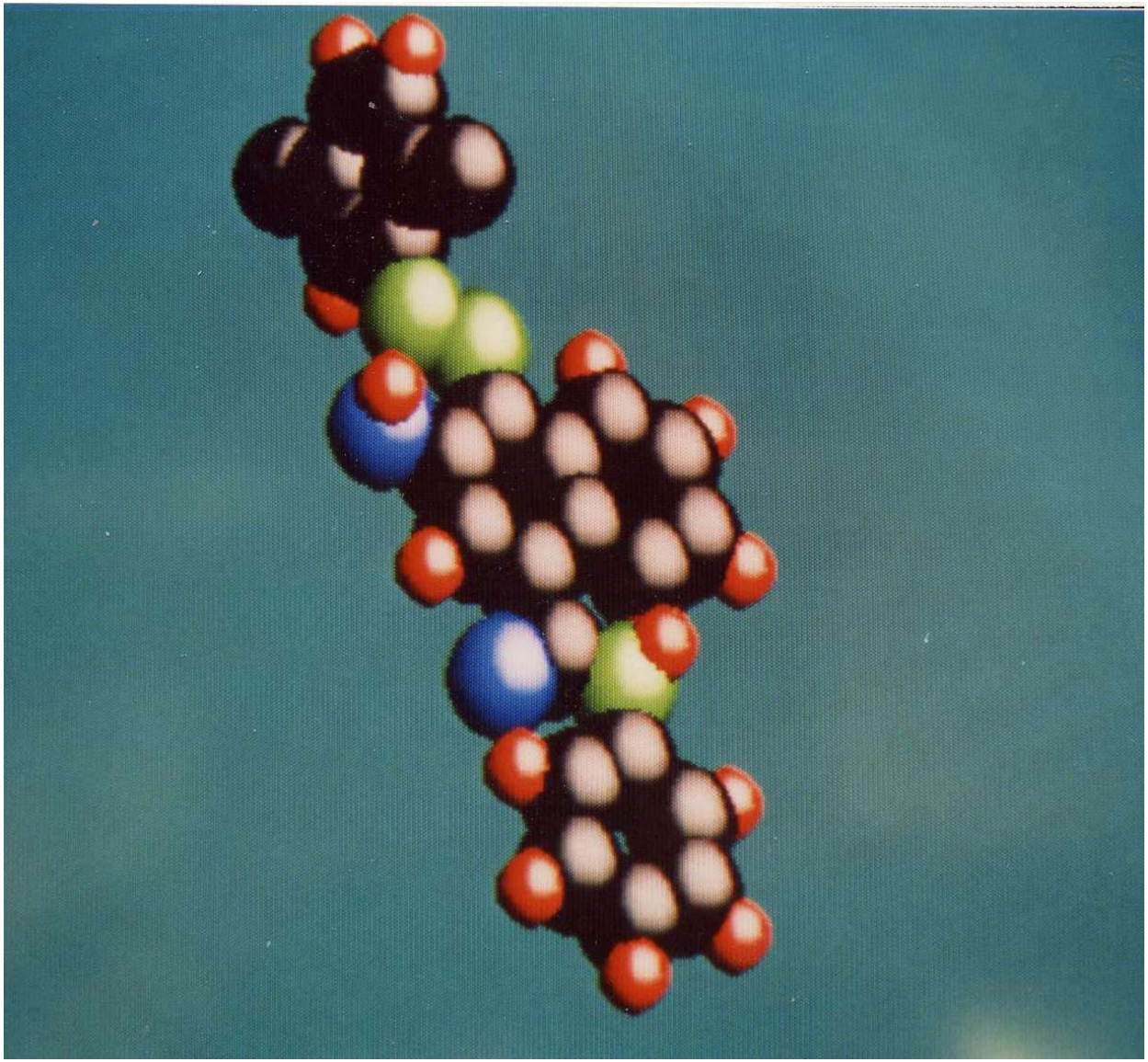


“GSP” in 1988



- Gouraud Shading
  - 10M Pixel/sec
  - 30K Polygons/sec
- Flat Shading
  - 160M Pixel/sec
- Lines
  - 1M Lines/sec
- Clock
  - 20MHz
- Technology
  - 1.2 μ mCMOS
- Transistor Count
  - 130K Transistors
- Chip size
  - 11.5 × 11.3mm
- Package
  - 144pin Flat Package

Molecular model image by GSP



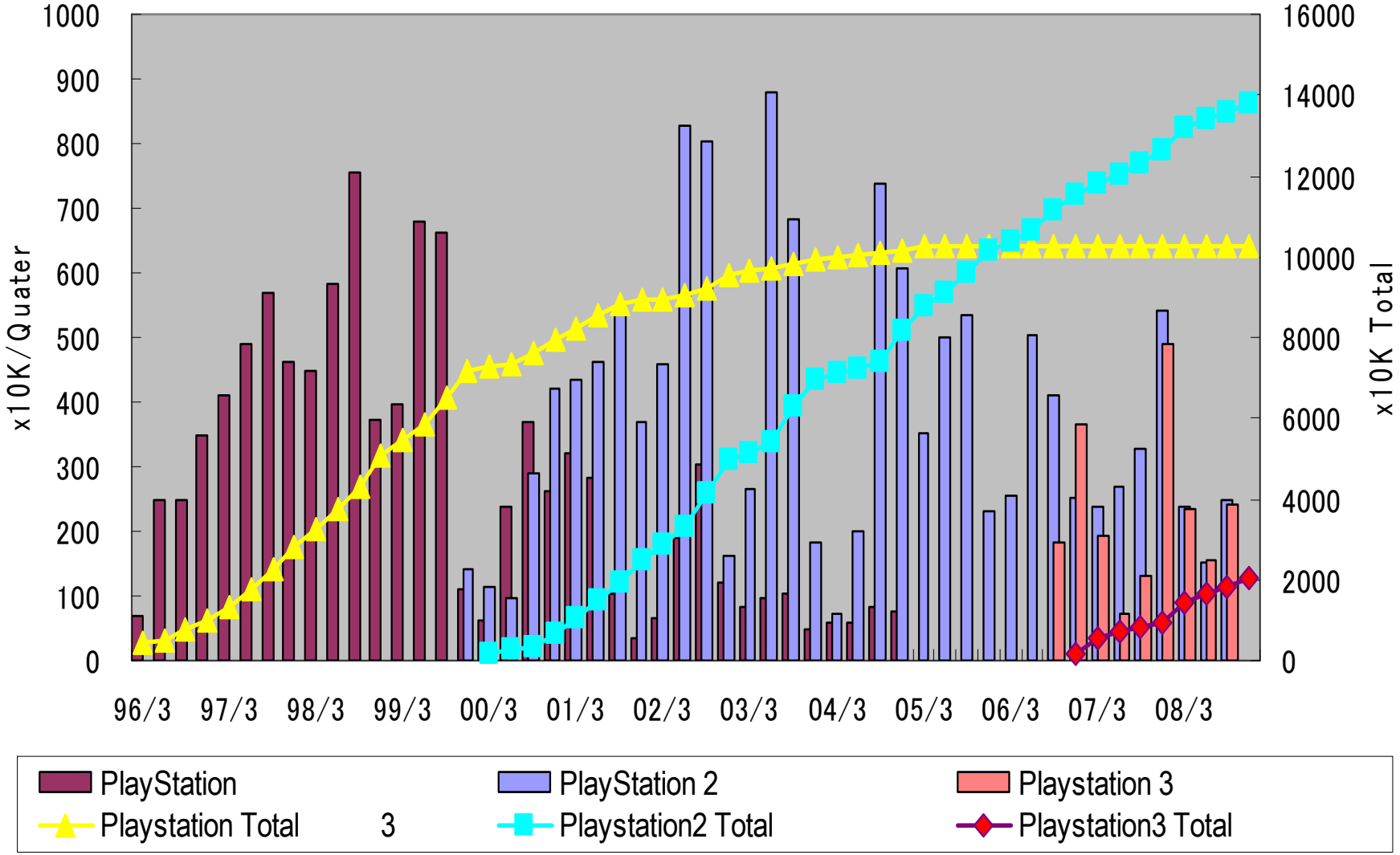
- 5160 Polygons
- 6.4 frames/Sec
- 8 bit/pixel
- 16bit Z Buffer

First Generation Playstation

Source : Wikipedia

Playstation Shipment History

From: http://www.scei.co.jp/corporate/data/

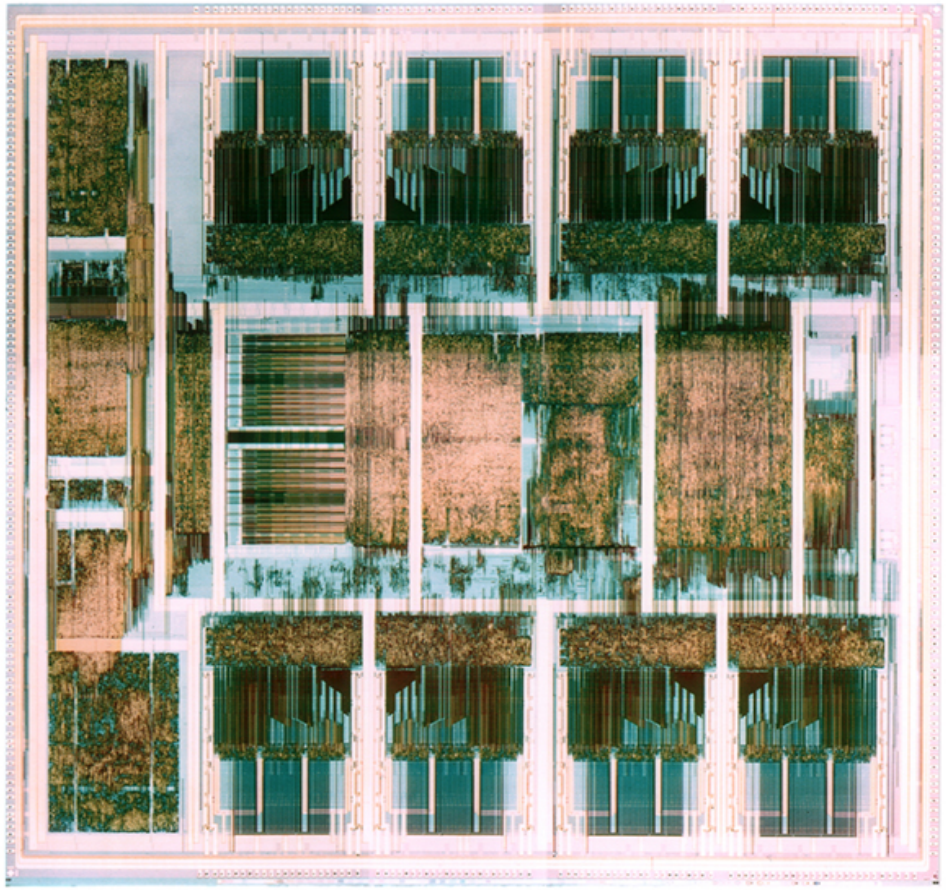


Playstation was very successful, though

- **Original business model was not making money from Hardware but Software license. In reality, could make money even from hardware, mainly because of semiconductor cost down.**
- **3D graphics could get very good reputation. But It's performance was not good enough yet. Emotion of the characters couldn't be presented!**
- **By considering game console life cycle, hardware performance should be competitive at least for a few years**
- **An epoch-making graphic chip was the key for the next generation**
- **Embedded DRAM technology based graphics was employed**
- **Main processor had to have enough performance correspond to very high performance graphics. Special processor had to be developed**

“Graphics Synthesizer ”(GS)

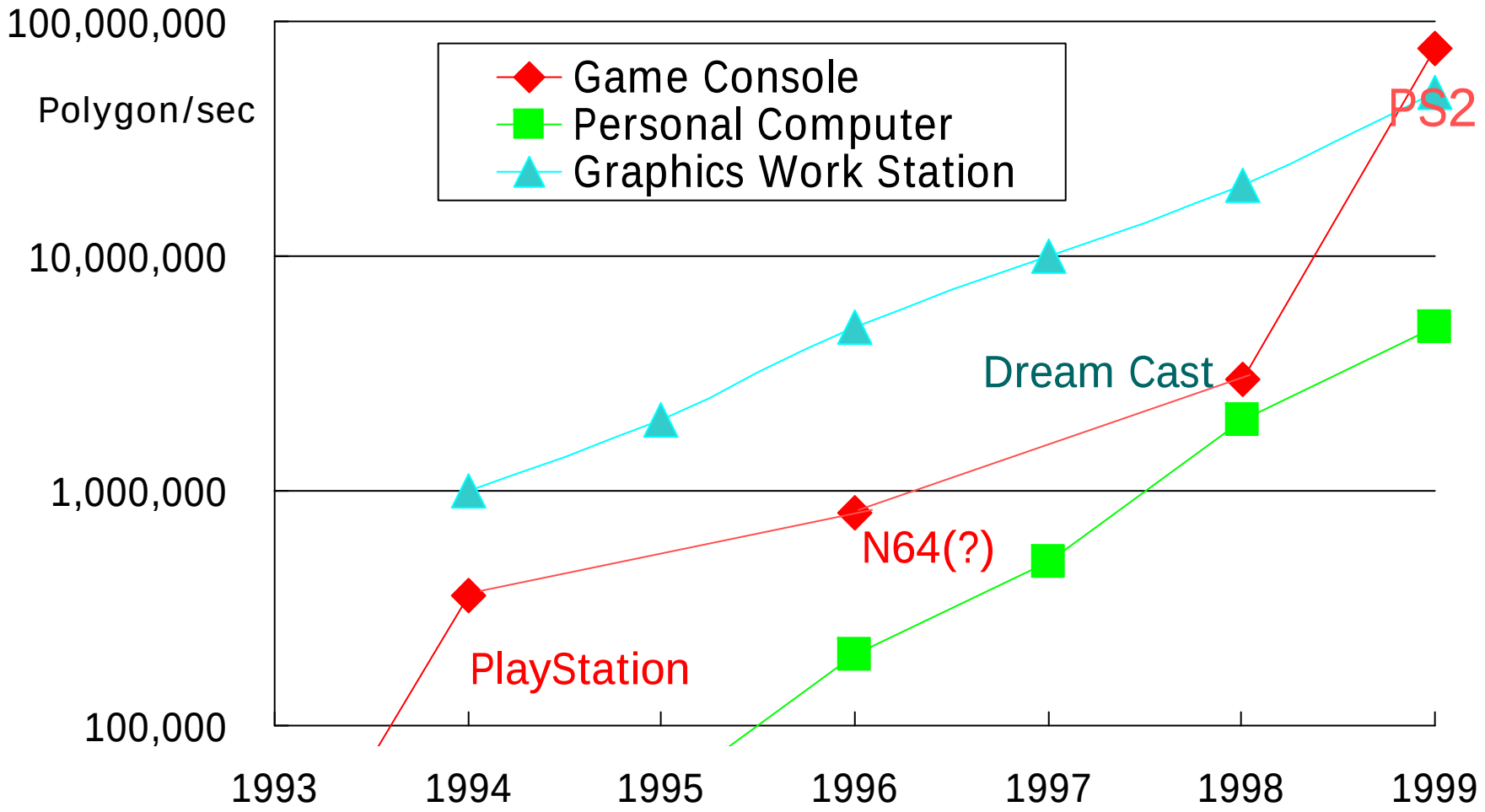
- 16.6mm × 16.8mm
- 32Mbit Embedded DRAM
- 0.25 μ m
- 47.7 M transistors
- Designed by SONY, SCE and Toshiba
- Fabricated by SONY



GRAPHICS SYNTHESIZER

16.6mm x 16.8mm (279mm²)
42.7M transistors
0.25μm

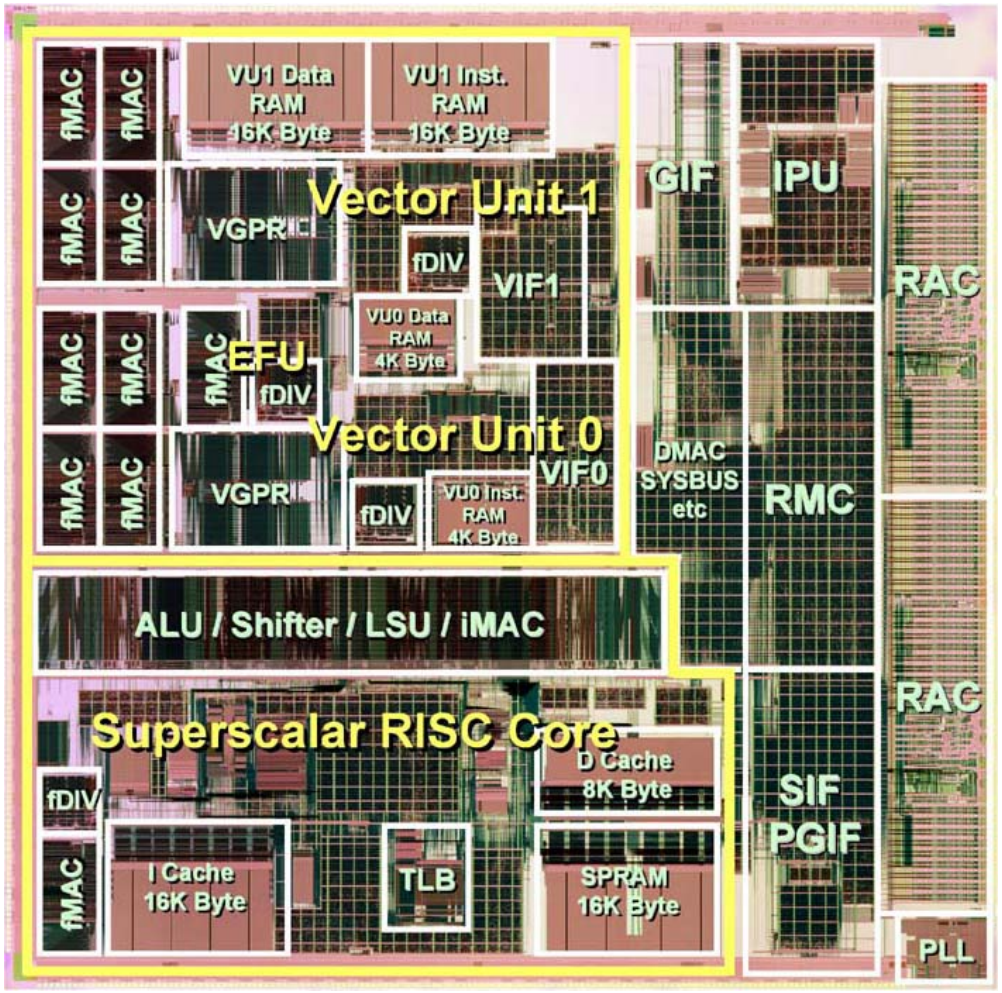
Rendering performance Trend



How Emotion Engine was born?

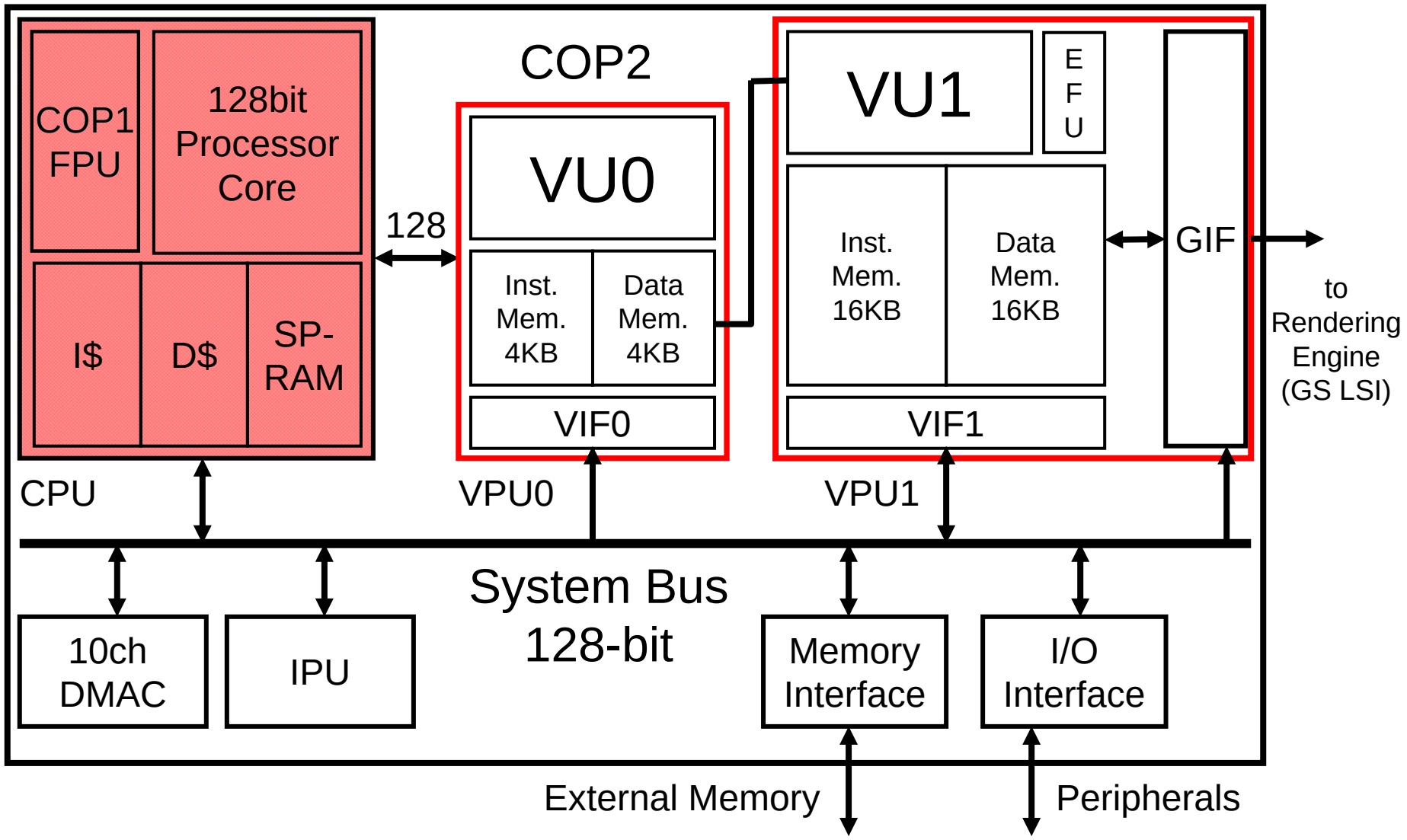
- **Toshiba could develop and provide the graphics chip for the first generation Playstaion. However, processor chip was provided by US company.**
- **Some engineers in Toshiba semiconductor division, began to consider to propose not only graphics but main processor for next generation Playstation, and it was called “Emotion Engine” afterwards.**
- **Started to approach to SCEI a few month after first generation Playstation was launched (12/3/1994).**
- **SCEI was interested in proposed Geometry Engine architecture, and started a joint technical investigation**
- **After main concept of Emotion Engine was accomplished, Toshiba team has started to develop the processor portion at the Silicon Valley office in 1996, before an agreement was done.**

Emotion Engine Die Photo

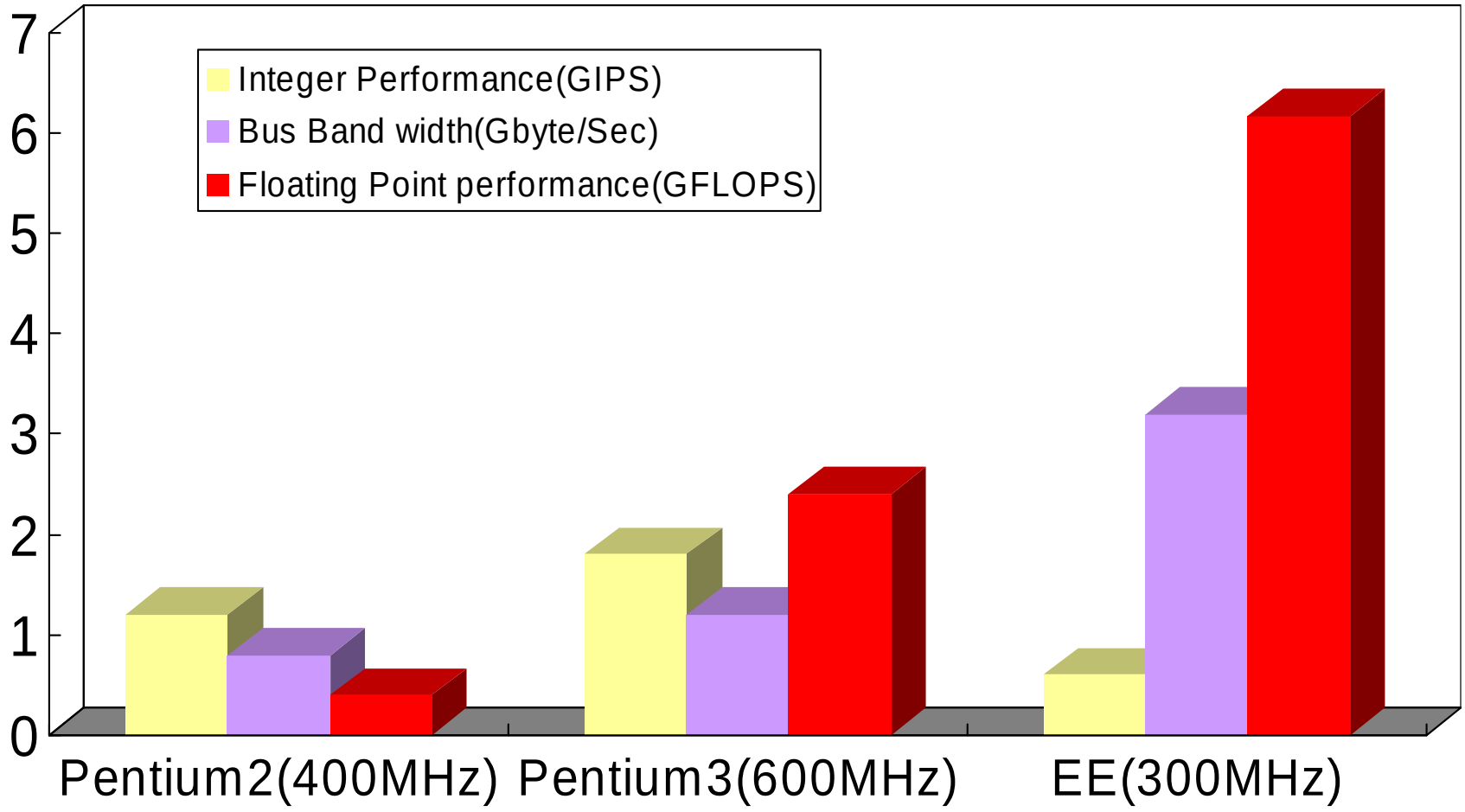


15.02mm x 15.04mm
Frequency : 300MHz
Transistors : 13.5M
Power : 18Watts
Design Rule : 0.25um
Gate Length : 0.18um
Designed by SCE and Toshiba
Fabricated by Toshiba

Emotion Engine Block Diagram



Emotion Engine Peak Performance



Emotion Engine Development History

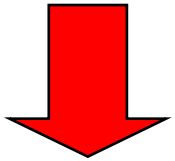
- Spring 1997：Joint Development Agreement was done (Schedule was defined)
- Spring 1998 ：Design Completion has been delayed because of many Bugs of CPU and not enough speed
  - Had to report Six month delay from the original schedule
- Spring 1998 ：Reorganize and enhance development team (82 engineers from Toshiba Japan), and Reset the Target date and specification
  - #1 Design Completion 7/1998
  - Chip size=17x14.1mm2
- Aug. 1998 ： EE#1 Design completion (8 month Delay)
  - Relaxation of the target frequency（300MHz=>200MHz)
  - Agreed to Relax voltage and temperature constraint
- Oct. 1998 ： Shipped the first sample and SCE started the system evaluation
- Dec. 31 1998 ： Shipped the software developable revised samples
- Feb. 1999 ： Presented at the conference（ISSCC）, fair reputation
- Mar. 1999 ： Next generation Playstation technical overview was presented at PlayStation Meeting 1999, and big impact on all over the world!

EE#2 Design completed as scheduled and achieved 300MHz Target

EE#3 Shrunken version(0.18um) development has been started

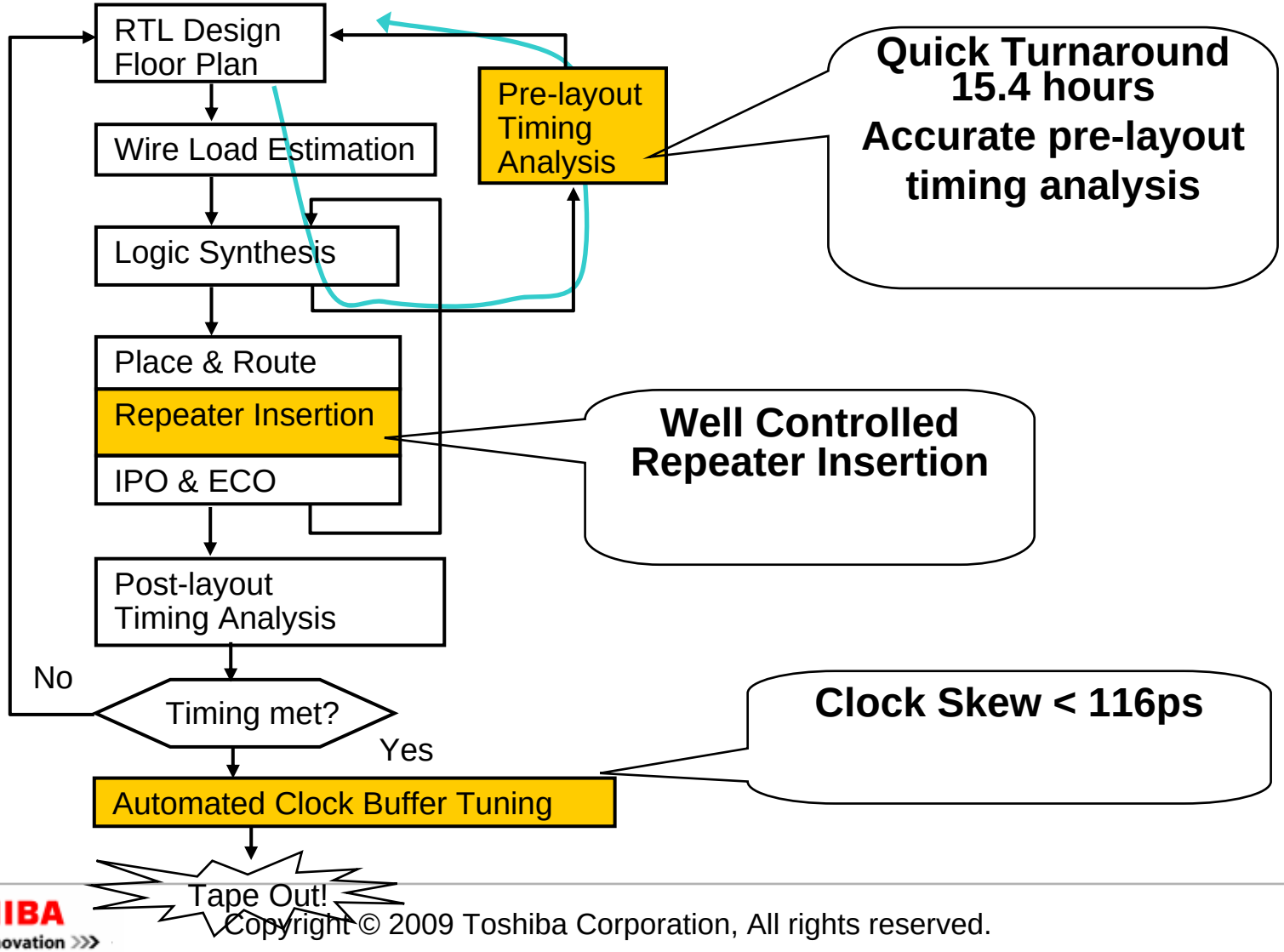
Timing Closure

- With 0.25/0.18 um design rule, controlling interconnect delay has become significant task in LSI design projects.

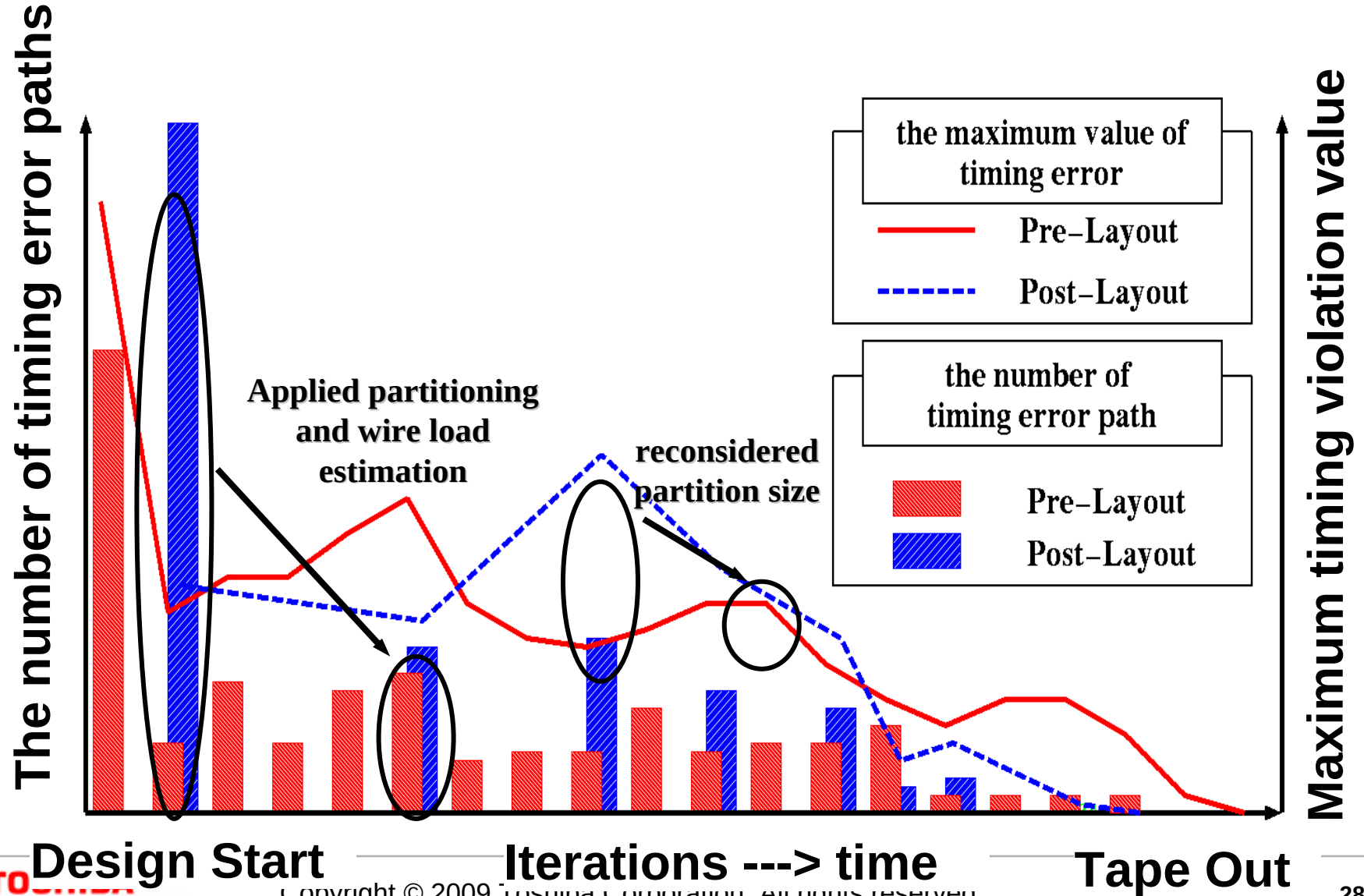


- Key is “quick timing analysis and feedback to RTL and floor plan”.
- Designer is able to do “what-if” analysis.

Timing Design Flow



Timing Closure -Results-



Clock Skew Management

- Clock skew must be minimized for
  - the maximum clock rate,
  - evading a race condition.
- Automated Clock design, e.g. CTS, is established in Standard Cell rich ASIC.
- In Contrast, half of EE is occupied by custom blocks (CB's). Manual tuning is time-consuming.

➔We developed an automated clock tuning method.

Playstation2

From Wikipedia

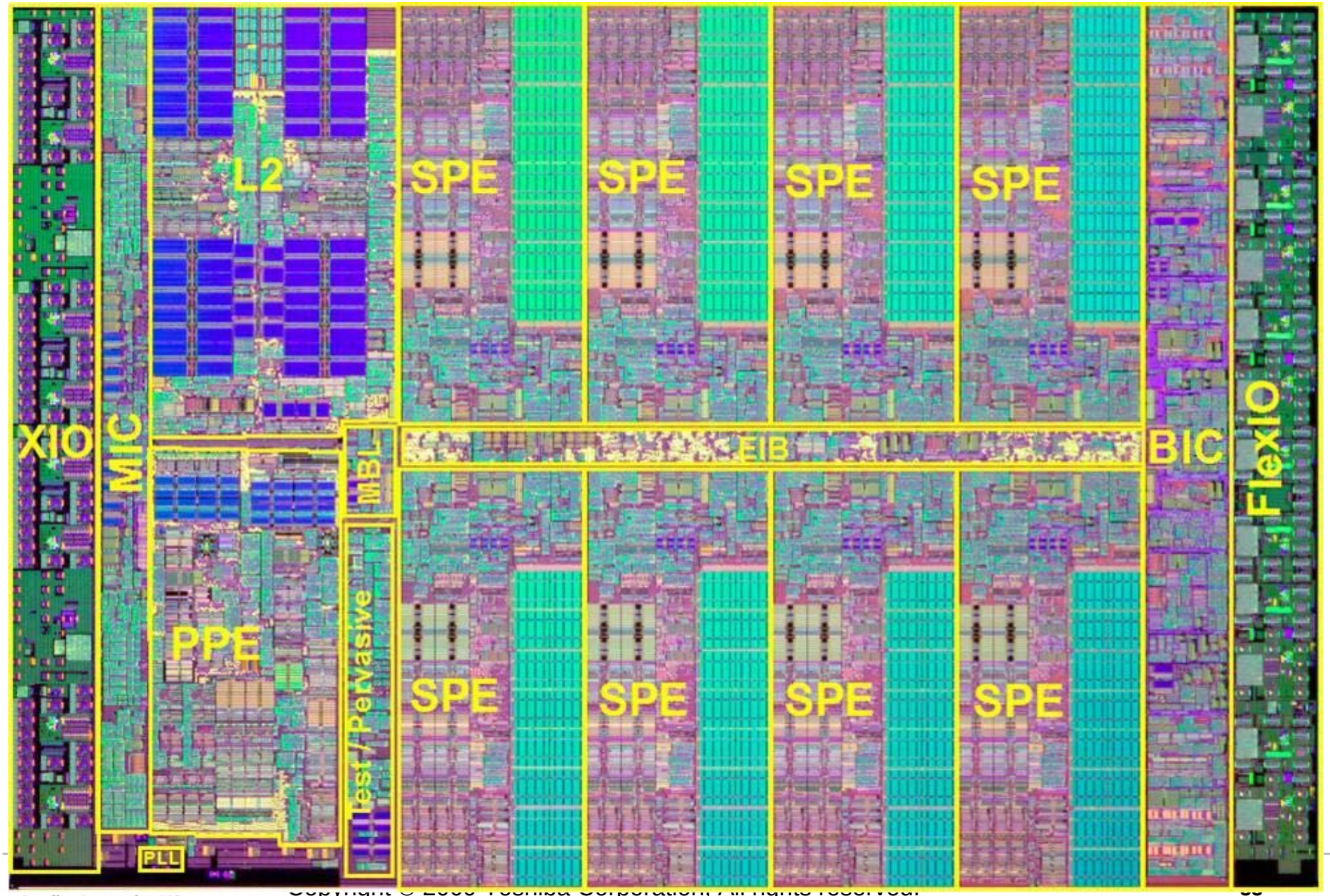
Beyond Playstation2

- **Jan. 1999 : The Investigation of the processor for the next-generation Playstation started internally in Toshiba**
  - At first, investigated the possibility to develop in Silicon Valley
  - Investigated IBM as a partner, they were not interested so much at first
- **From the experience of Playstation2**
  - We didn't have to use the existing processor architecture, because Playstation can have enough volume to be a standard by itself
  - From DVD capability experience, It will not be only a game console but the center for the entertainment in home
  - Broadband network will be popular and have very big impact
- **Basic concept of the next generation processor**
  - Not just for Game console, but should be useful in various applications
  - So, it must be scalable
  - The real-time computation will be the key for gaming and networking
  - New computer architecture should be employed for the new world
- **Development Team**
  - By talking directly from Kutaragi-san to IBM, SCEI, IBM, and Toshiba have agreed to set up the joint development team
  - We have agreed to develop next generation general purpose processor, and three company join the project, totally even share of the resource and the right

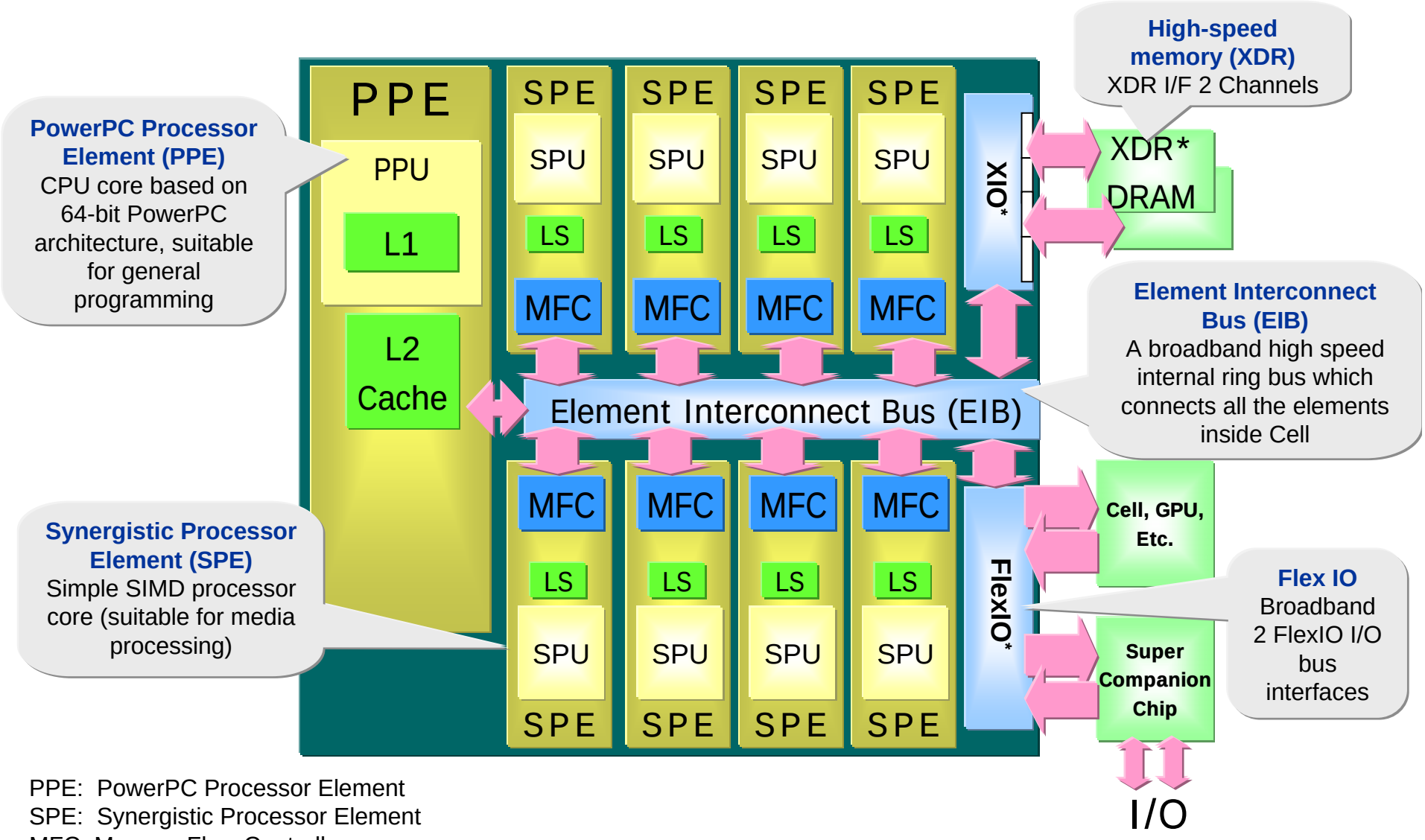
Cell BE Development Project

- **Established main campus in IBM Austin**
  - **For the quick startup**
  - **Reserve excellent engineers**
- **Multiple sites were mandatory**
  - **Overcome management difficulty by frequent tele-conference**
  - **Network infrastructure was very effective for the information sharing**
- **Joint Development team has been established**
  - **Each part was consist of mixture of three companies engineers**
  - **For the good communication to collaborate smoothly**
  - **Necessary also for the technical transfer to each company**
- **After target was clarified, development was relatively smooth**
  - **Quick termination of culture friction was achieved**
  - **Flexible resource allocation was possible**

Cell BE Die Photo



Cell Block Diagram



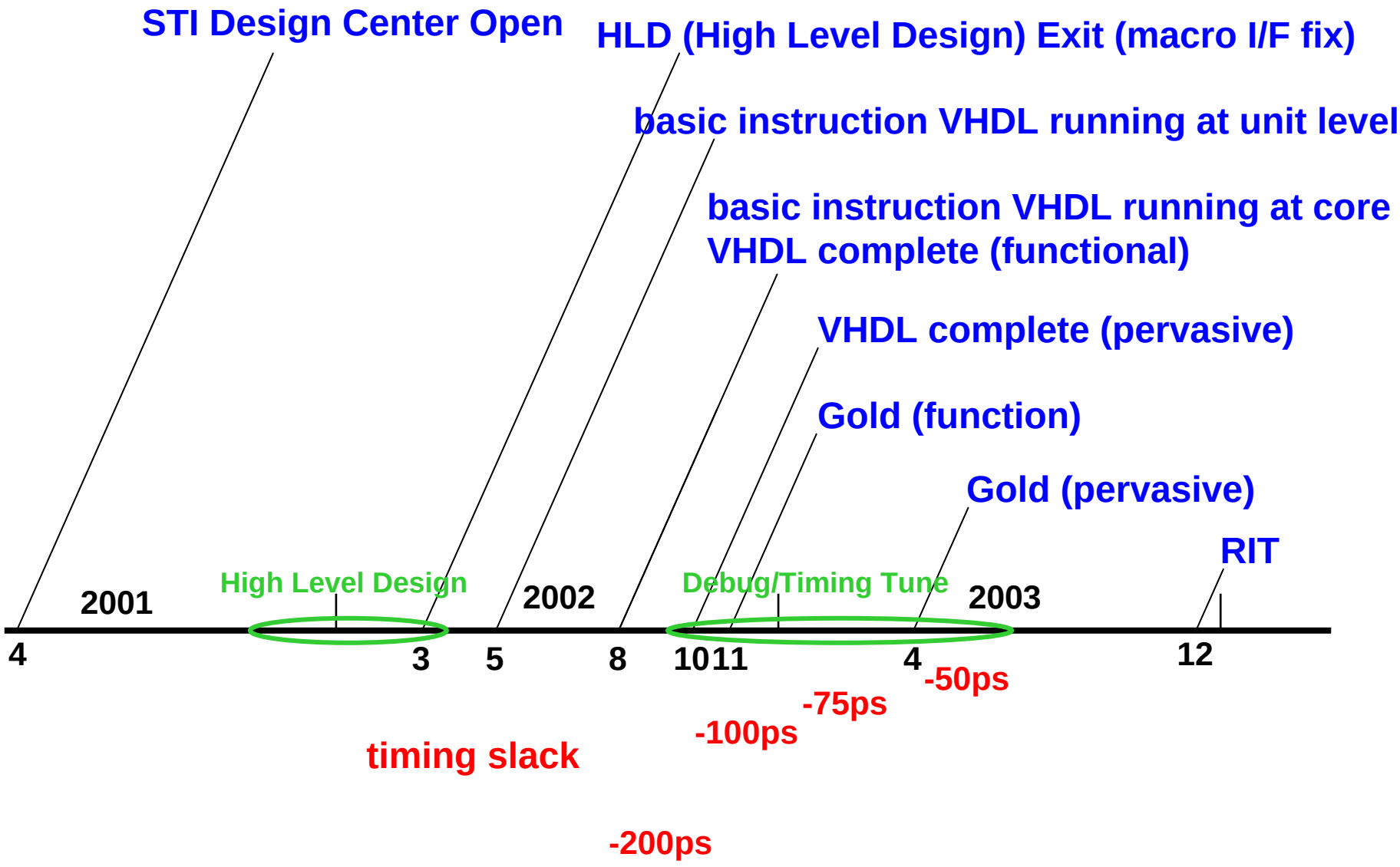
PPE: PowerPC Processor Element
SPE: Synergistic Processor Element
MFC: Memory Flow Controller
LS: Local Storage

* Trademarks of Rambus, Inc.

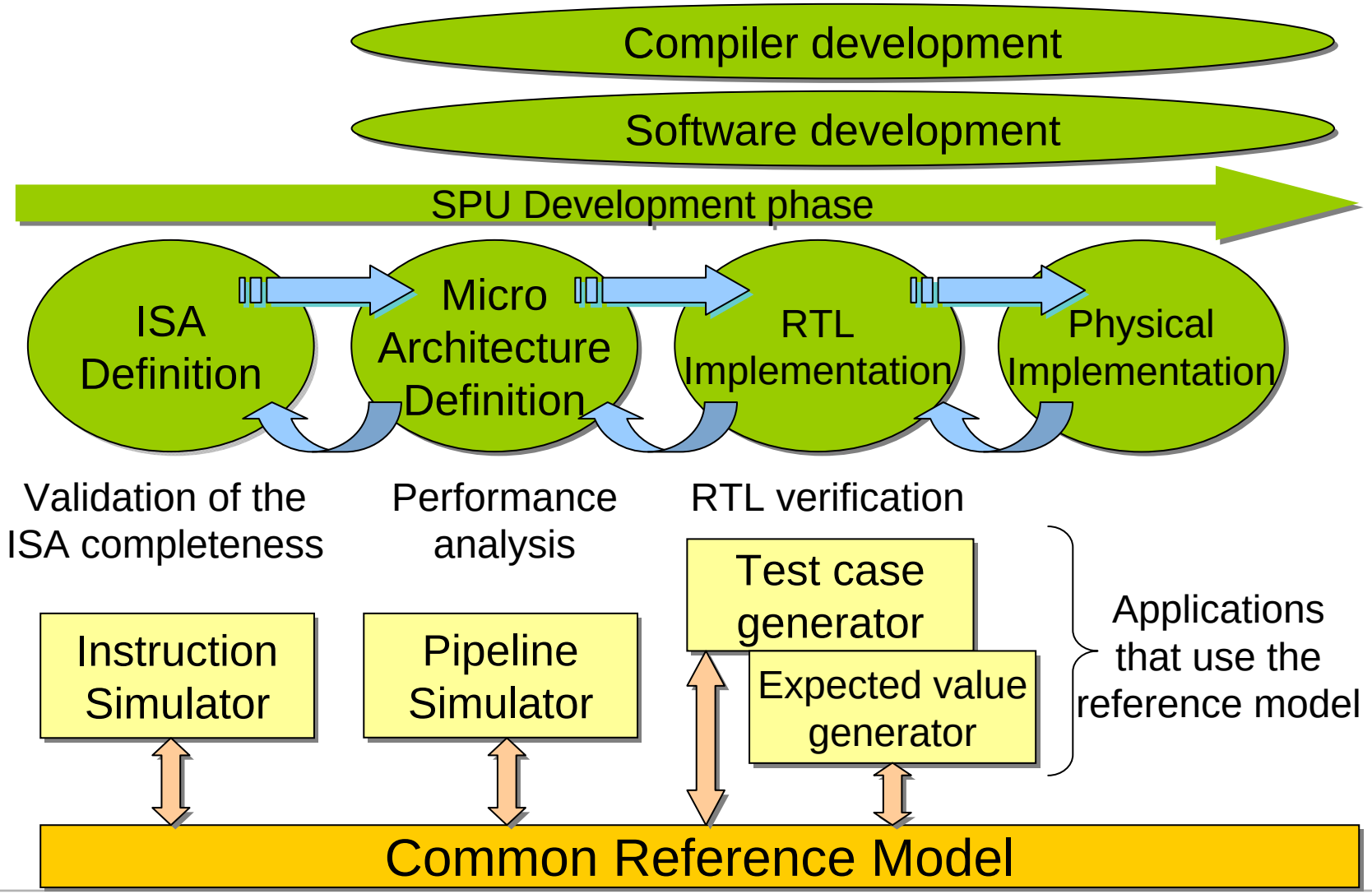
Cell BE Major Development Topic

- **Apr. 2000 : Architecture investigation has been started among three companies**
  - **Big culture gap, and lot of friction**
  - **Various candidates were investigated, and concluded almost same as present one**
- **Mar. 2001 : Public announcement of Joint development**
  - **Started project by setting the campus in Austin**
- **Sep. 2001 : Toshiba has started to investigate the function of Peripheral chip**
- **Apr. 2004 : Cell BE first sample was accomplished and worked!**
- **Feb. 2005 : First technical presentation at ISSCC conference**
  - **Big impact all over the world**
- **Aug. 2005 : Toshiba presented peripheral chip and SPE asign software idea**
- **Oct. 2005 : Toshiba demonstrated at CEATEC exhibition**
  - **One of the biggest impact demonstration**
  - **All major TV station mentioned in the news program**
- **Apr. 2006 : Toshiba started to provide Cell BE development set**
- **Sep. 2006 : IBM won a Cell BE based super computer for the national research Lab.**
- **Nov. 2006 : SCEI launched Playstation3 with Cell BE**

Cell BE（SPU) Design History



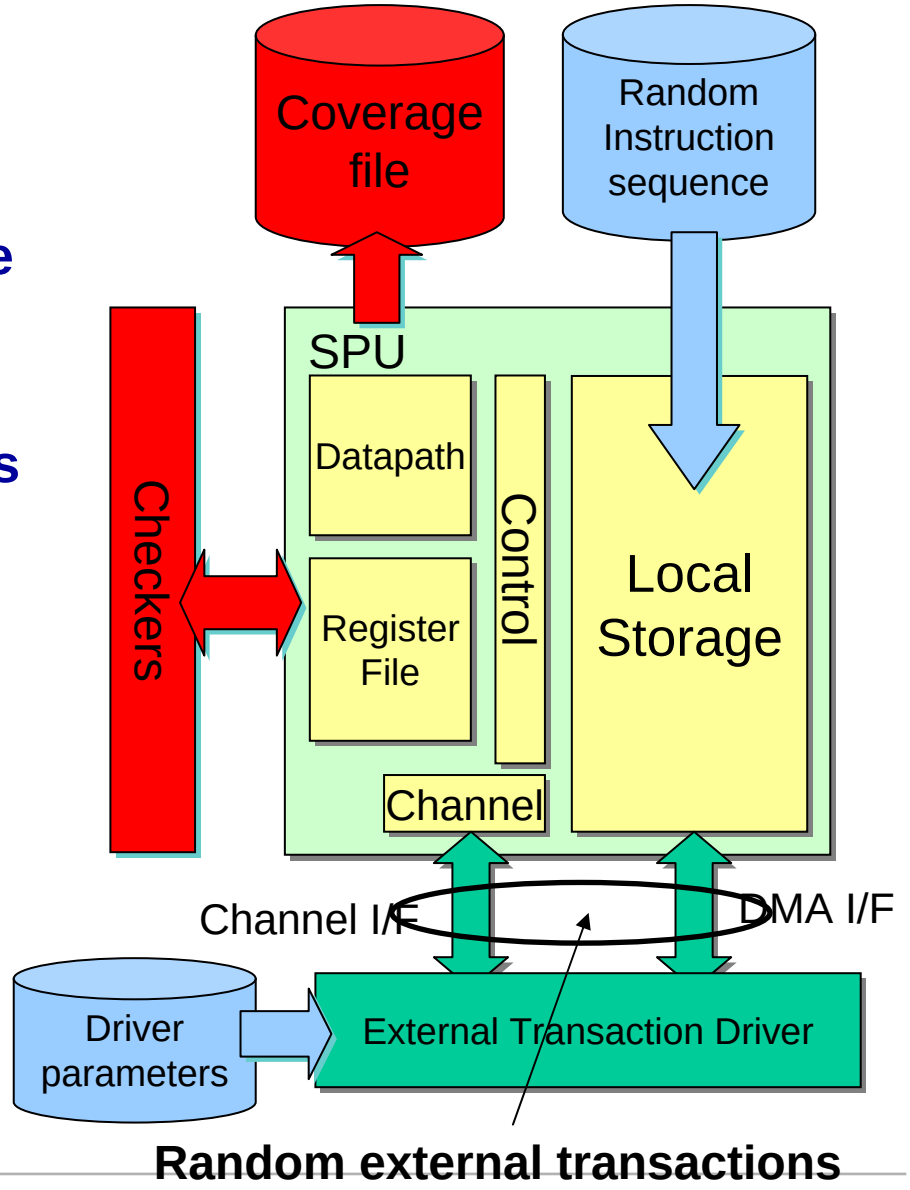
Each Reference model for SPU Development phase



SPU Verification Strategy

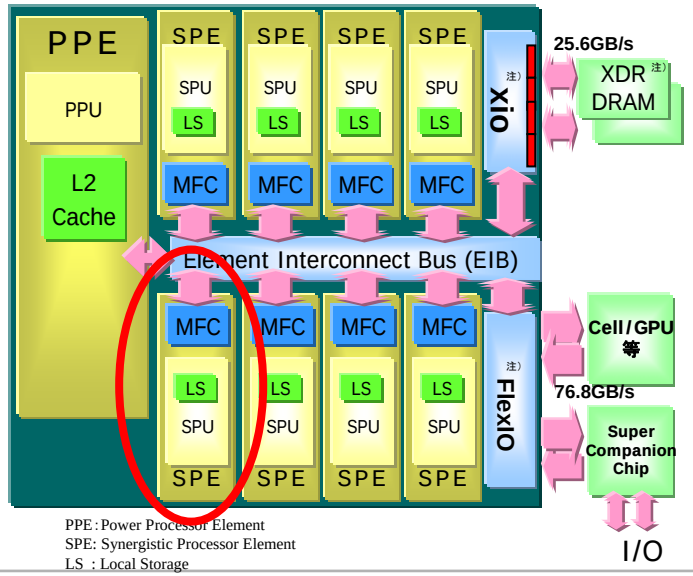
Coverage Based Verification

- **Test items are written as coverage events**
- **Executes simulation random test cases until all the coverage events are hit.**
  - Random instruction sequences
  - Random external transactions
- **The checkers check SPU logic correctness while simulation**
- **Coverage files are generated as a simulation results**

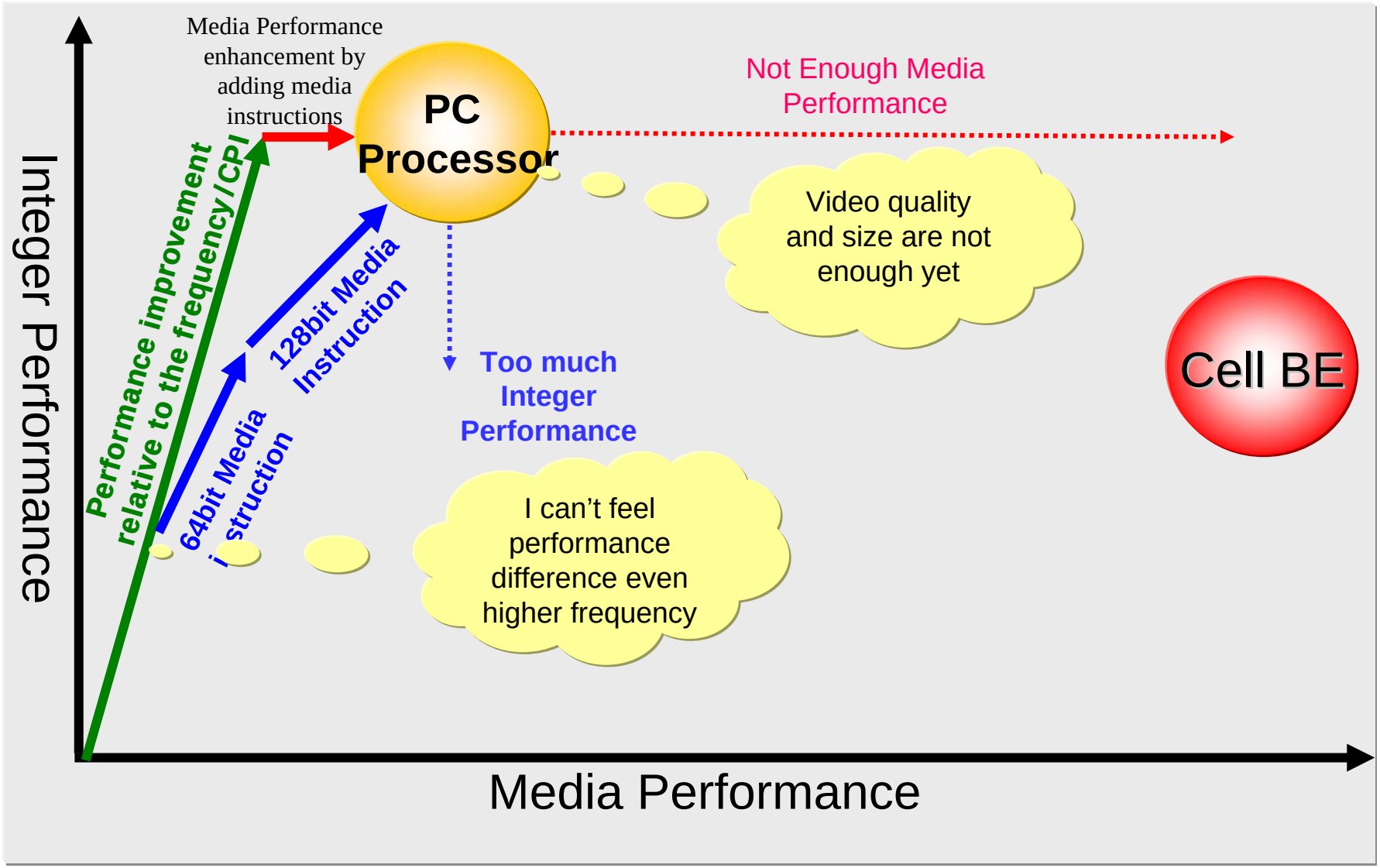


Synergistic Processor Element Feature

- **New architecture for the data processing**
  - **Media and floating point computation**
- **RISC type instruction set**
  - **High level language oriented**
- **SIMD based instruction scheme**
  - **128 bit width Parallel execution (e.g. 4x32bit)**
- **Large 128bit width 128 entry register file**
- **256KB Local store, not Cache**
- **Rich performance monitoring capability**



Cell BE positioning as a Processor

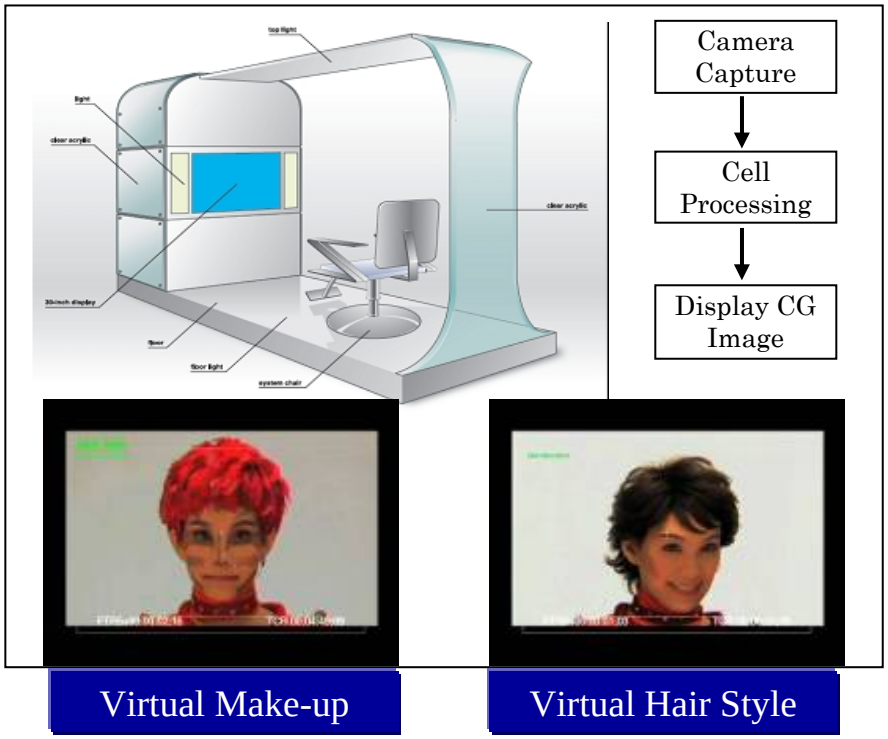


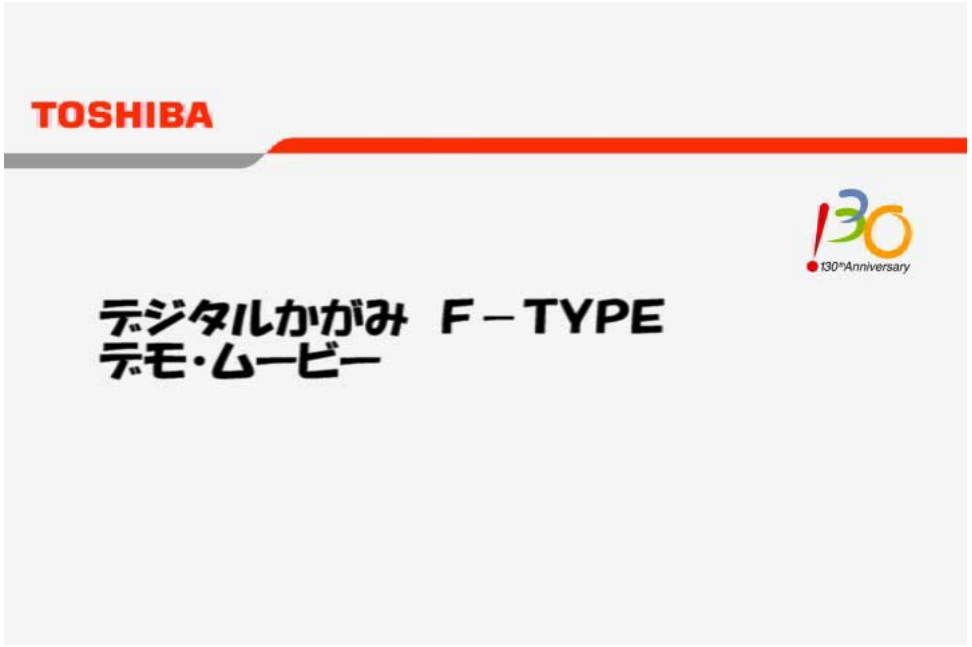
Cell BE Proposes New Computer Direction

- **New computer direction proposed by Cell BE**
  - **To show hardware feature as is to the user**
    - Program must be written by considering HW structure and memory size
    - Need knowledge about HW
  - **Instead, let user know what is going on in the computer**
    - Easier performance tuning
    - Especially for realtime system
  - **Overwhelming cost performance is achieved**
    - Very Small SPE sometimes provide twice of performance of PC processor
- **Maybe new direction since RISC is proposed**
  - **More than 20 years ago**

Real-time Face Tracking

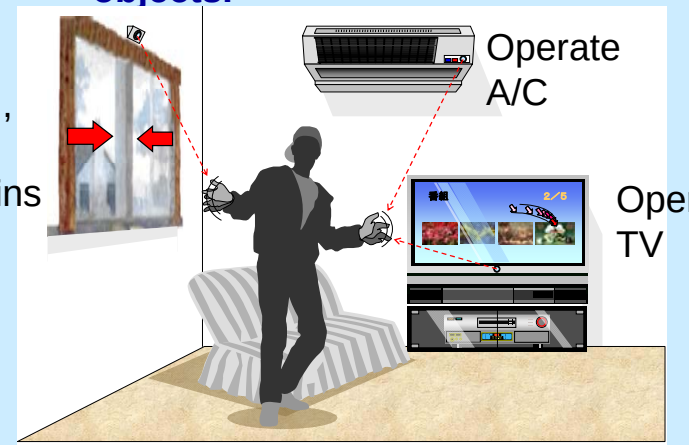
- **Camera captures the face of the person facing the “mirror”、and in real-time, the rendered image is projected in the “mirror”.**



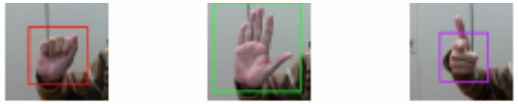


Hand Gesture User Interface

- **Operate products using hand gestures (hand position, motion)**
  - **Deviceless remote control.**
  - **Applicable for a variety of daily life objects.**

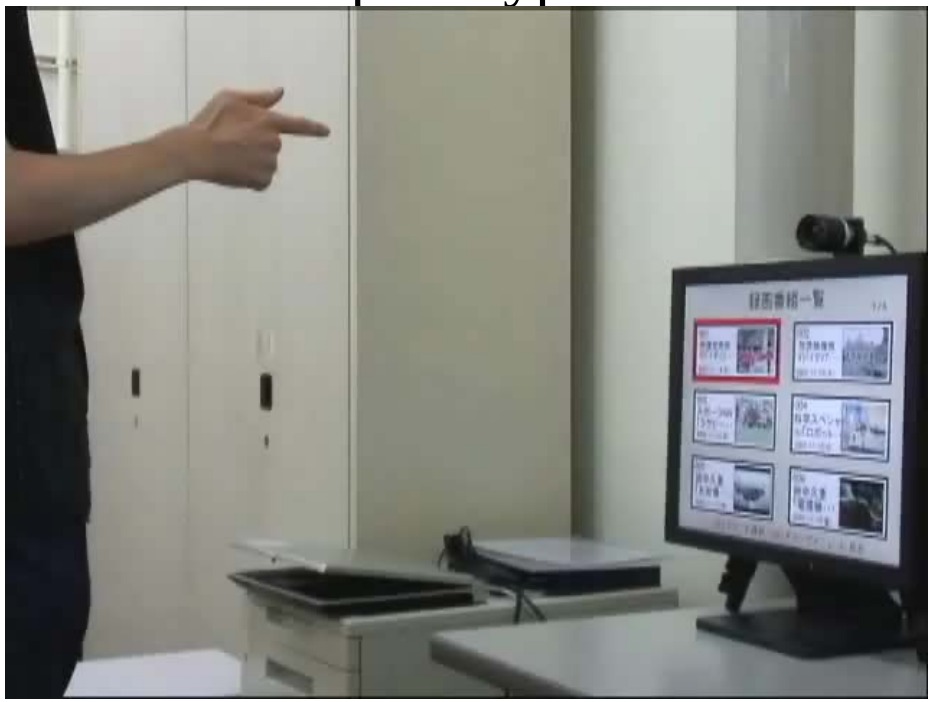


- Three hand share can be recognized

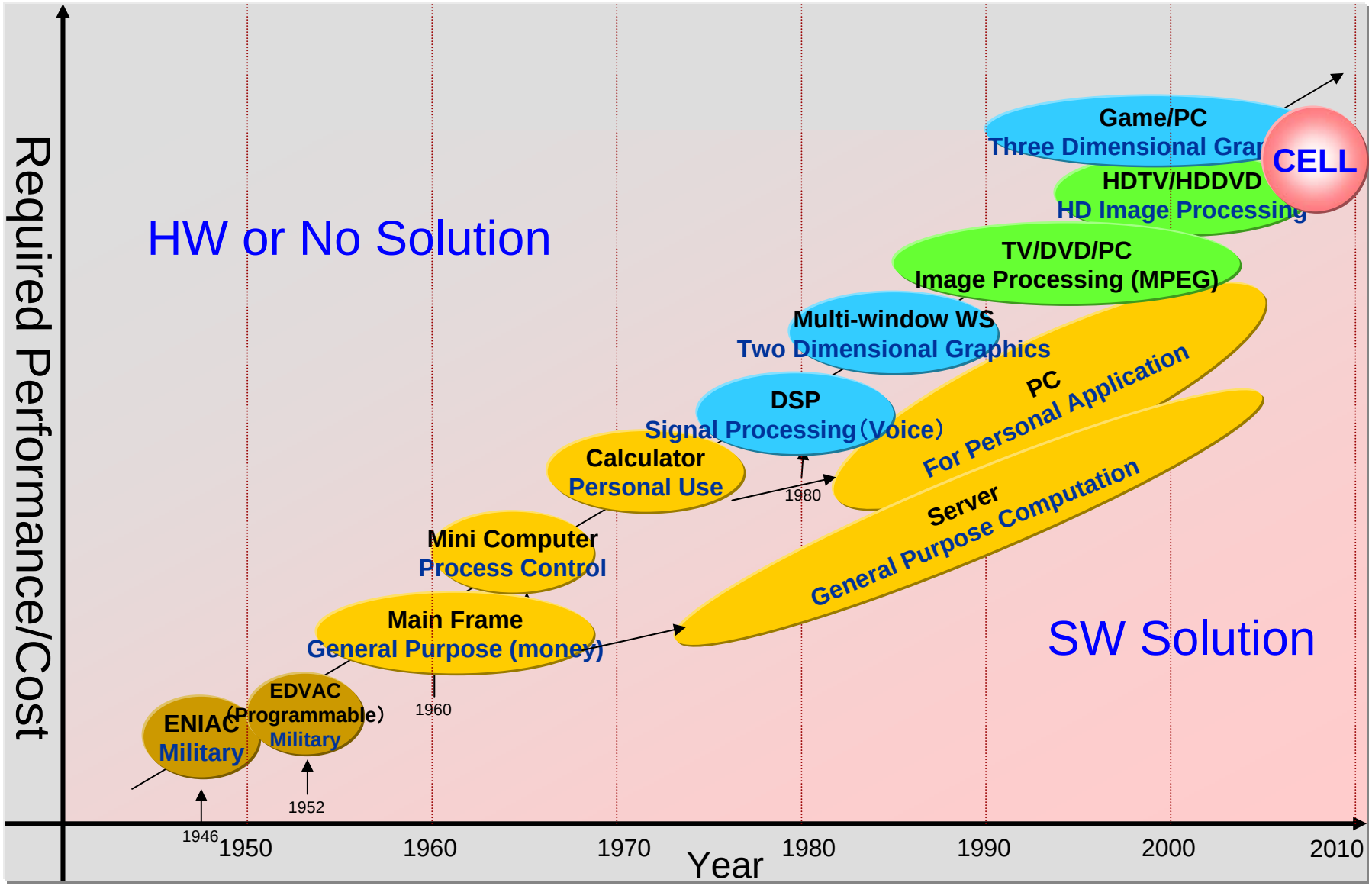


- GUI Control by recognized image

Hand gesture controlled media player equipment prototype

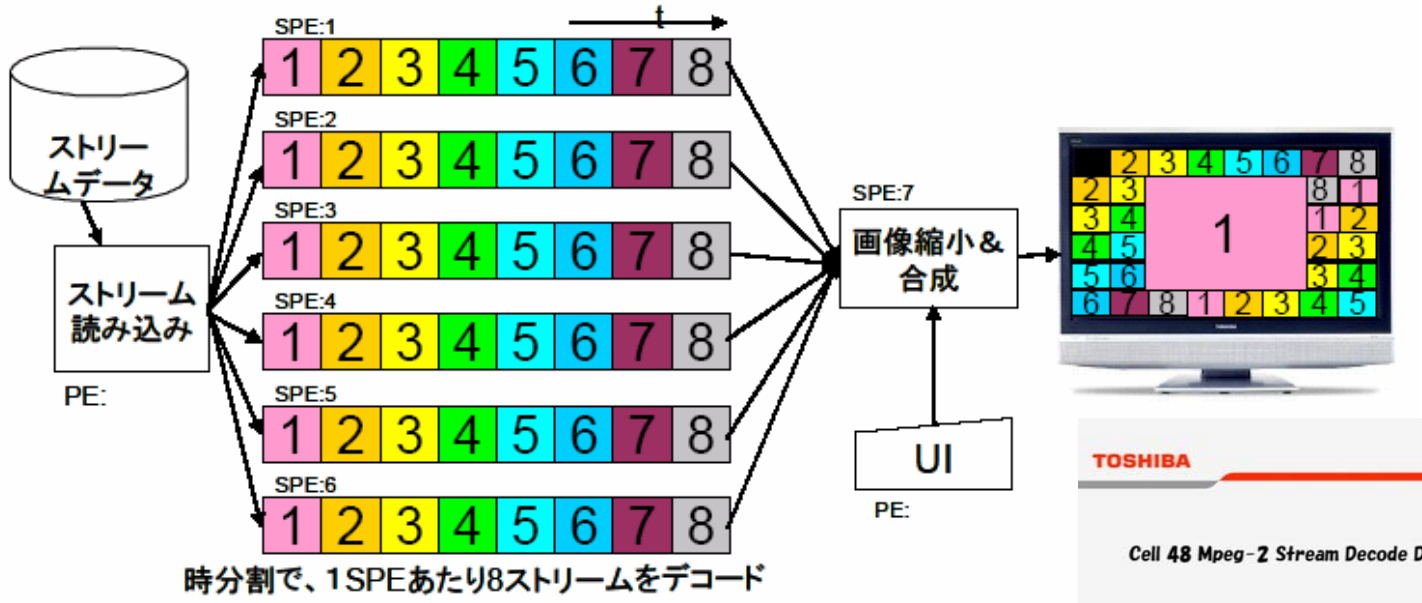


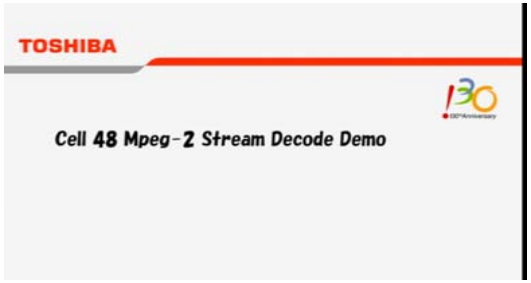
Trend of HW→SW



48 Streams (MPEG2) Decode Demo

- **MPEG2 (About 4Mbps) ・・・ 720 x 480**
- **Read out 48 streams from HDD and Decode**
- **Shrink to 1/3 and arranged to one picture for displaying on the TV**

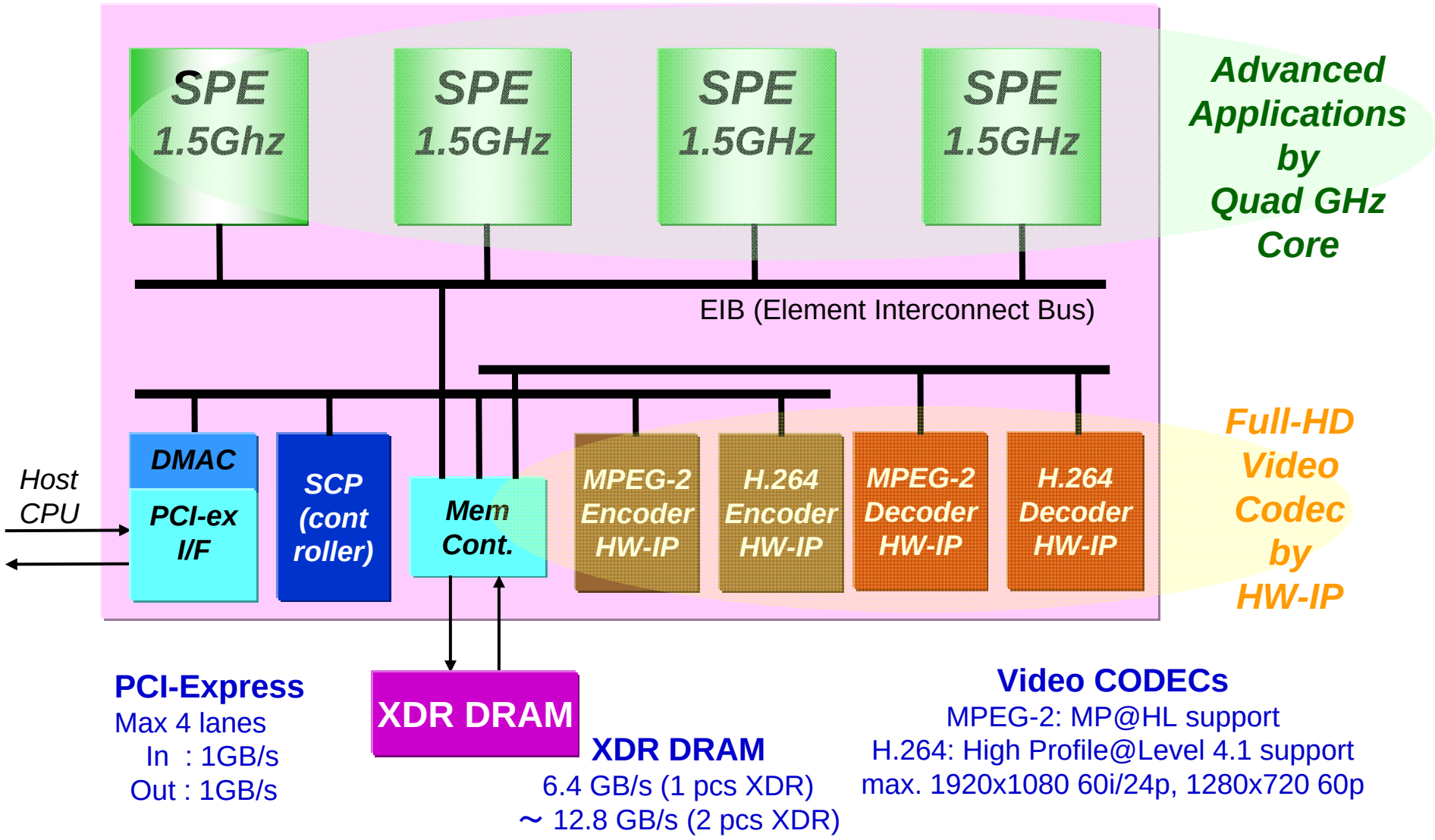




Hard to Find Customers in this Field

So, by Focusing on Video Application for PC!

SpursEngine™ Block Diagram



PCI-Express
Max 4 lanes
In : 1GB/s
Out : 1GB/s

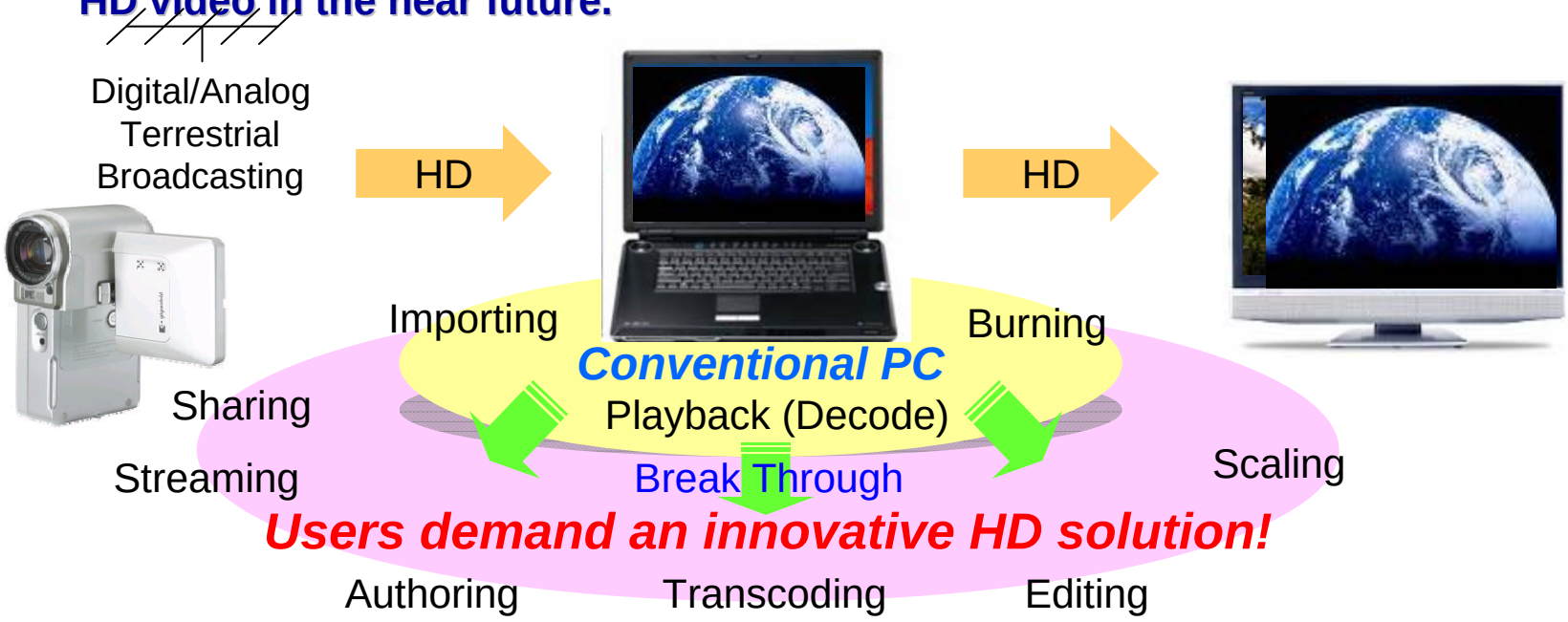
XDR DRAM
6.4 GB/s (1 pcs XDR)
~ 12.8 GB/s (2 pcs XDR)

Video CODECs
MPEG-2: MP@HL support
H.264: High Profile@Level 4.1 support
max. 1920x1080 60i/24p, 1280x720 60p

XDR™ DRAM is trademark of Rambus Inc. in the United States and other countries.

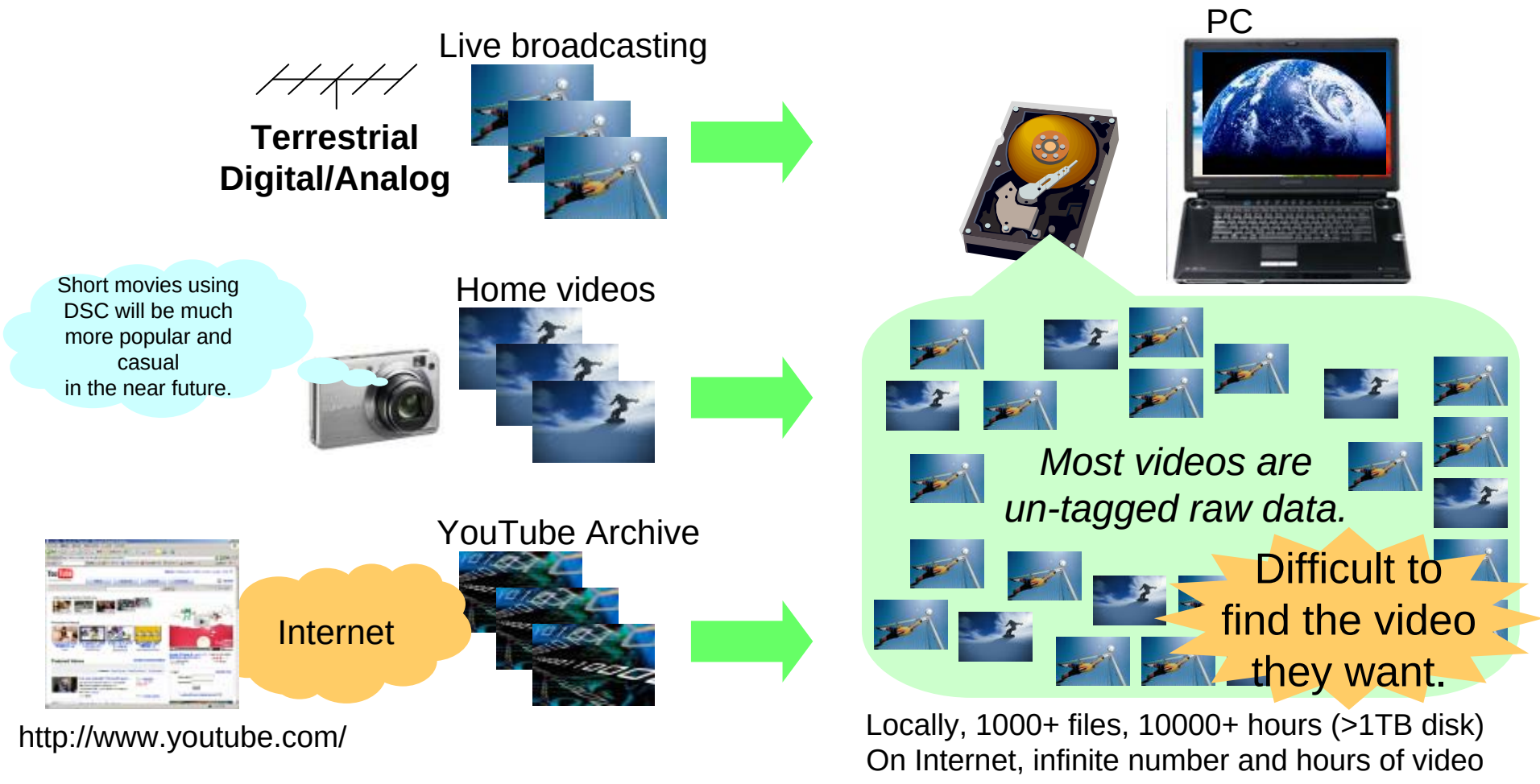
What is the Next Target for PC? Answer is HD.

- **Emergence of HD Contents**
  - **High Definition (HD) era has been quickly emerging. For instance, video content from digital terrestrial broadcasting, digital video cameras, and optical disks are all HD ready.**
- **HD contents require much more processing power than SD contents.**
  - **HD needs 6 times higher bandwidth than Standard Definition (SD). Conventional PC architecture of CPU and GPU can only decode HD video in real-time.**
  - **CPU, even though it keeps getting faster, will not be capable of real-time encoding HD video in the near future.**



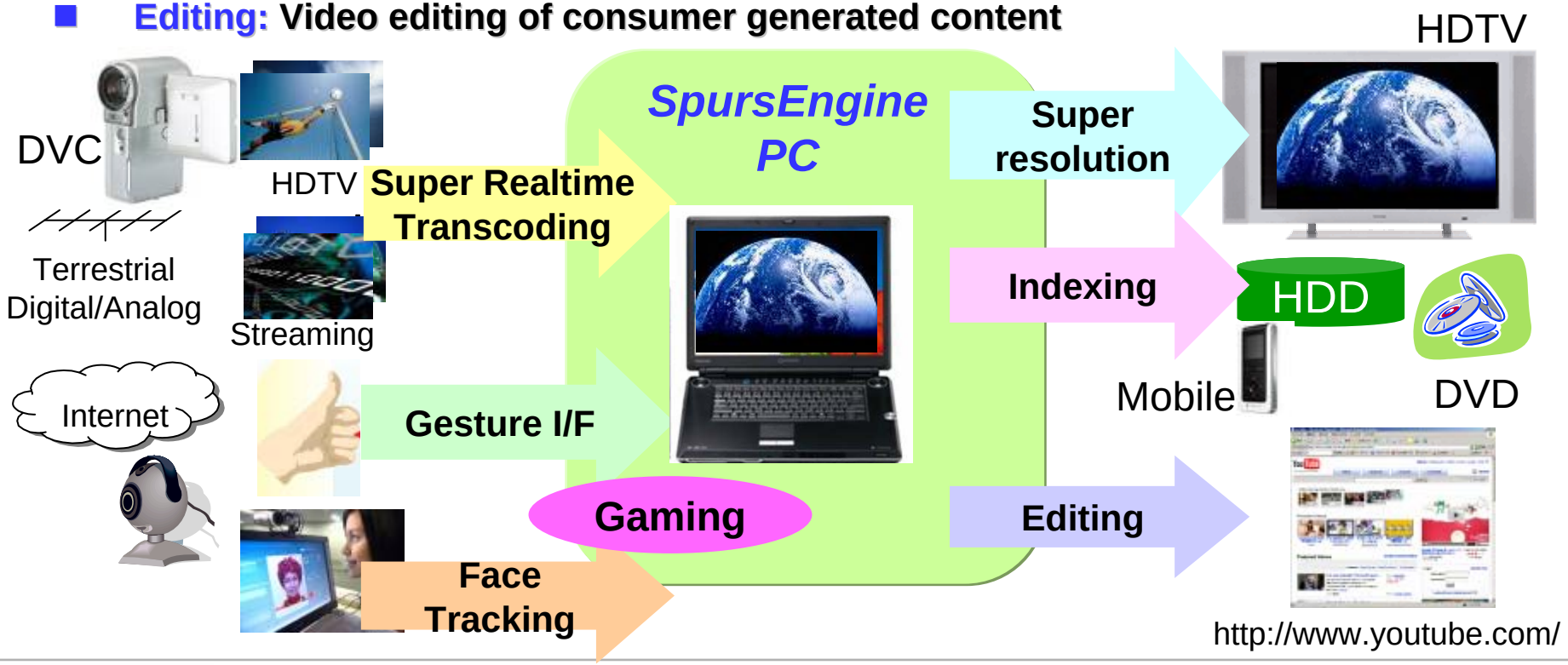
Demand: Video Indexing and Searching

Future demands: not only transcoding, but also *indexing and searching features* to easily find the video which they want to watch.



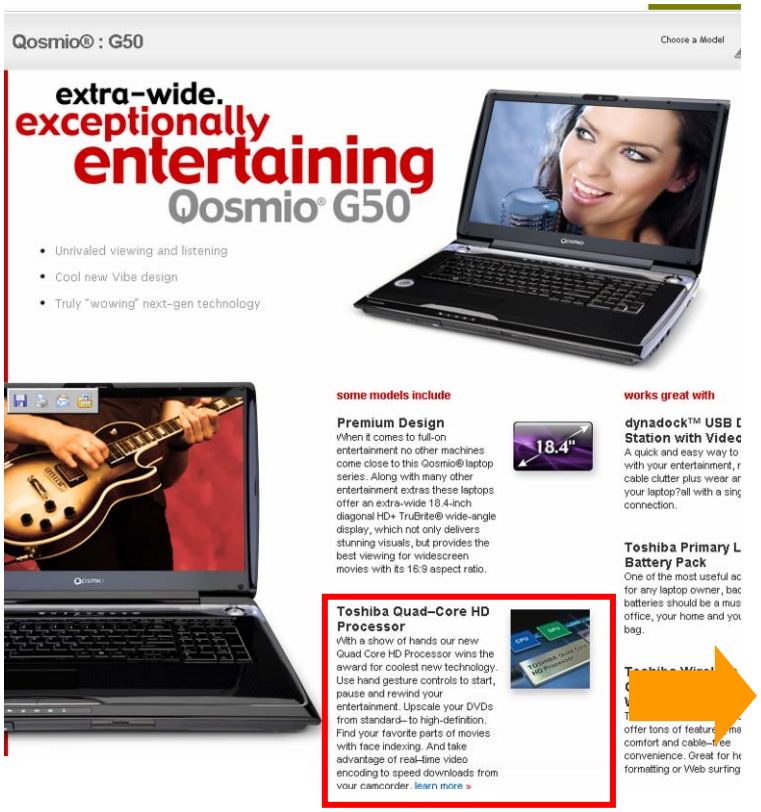
Further Advantages: New applications by SpursEngine

- **Super realtime Transcoding: Transcoding at faster than real-time**
- **Super Resolution: Picture resolution up-scaling for HDTV**
- **Indexing: Video categorizing during HDD storing, DVD burning**
- **Gesture I/F: Control various devices in the living room by hand gestures**
- **Face Tracking: Realtime 3D face tracking for communication tools**
- **Interactive Gaming: New type of realtime game with Gesture I/F and Face Tracking**
- **Editing: Video editing of consumer generated content**



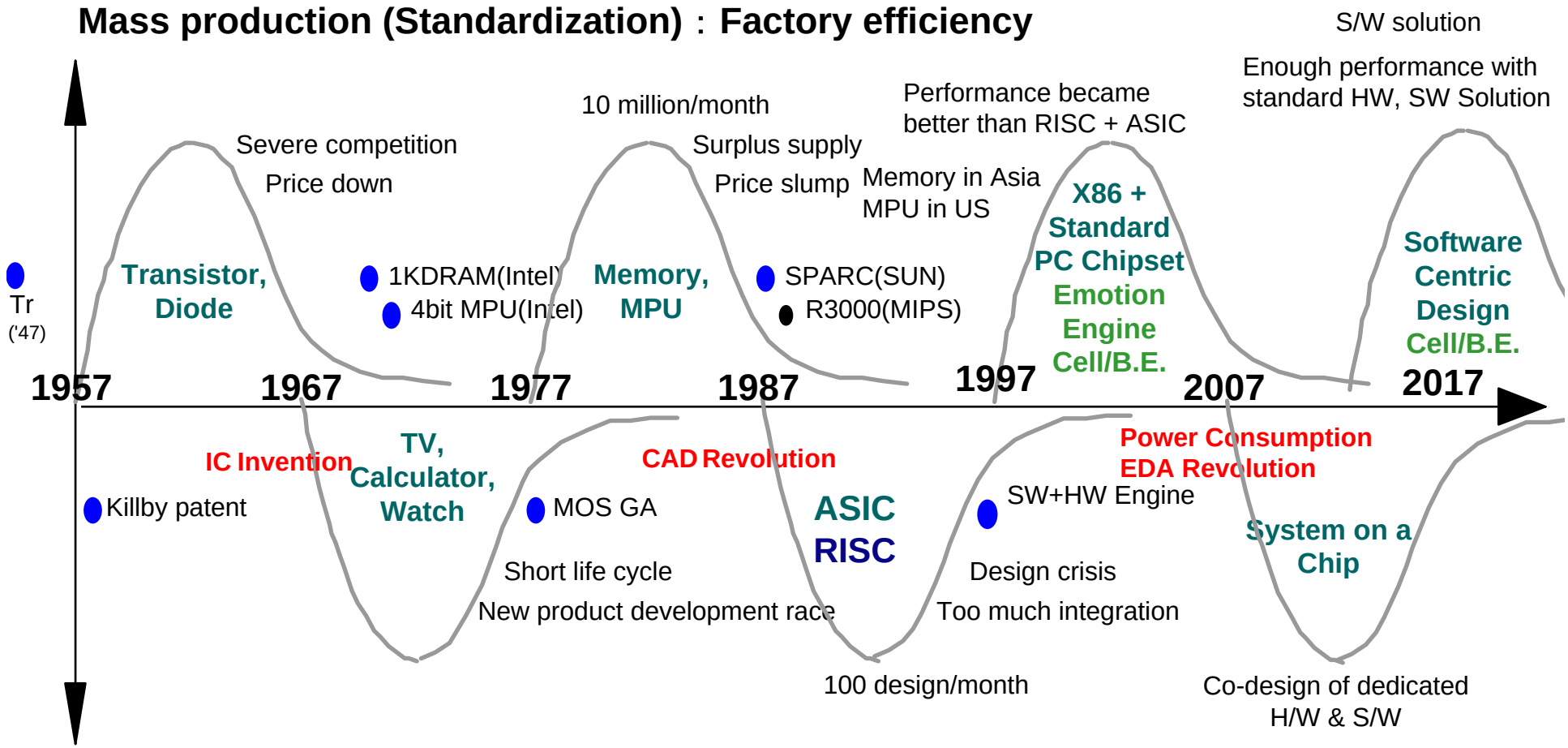
Toshiba PC: Qosmio with SpursEngine

- **Toshiba released Qosmio empowered by SpursEngine in July 2008.**



Reference URLs:
http://explore.toshiba.com/laptops/qosmio/G50
http://explore.toshiba.com/innovation-lab/quad-core-processor

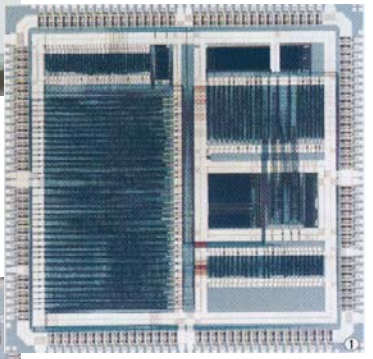
Waves to Standardization and Customization

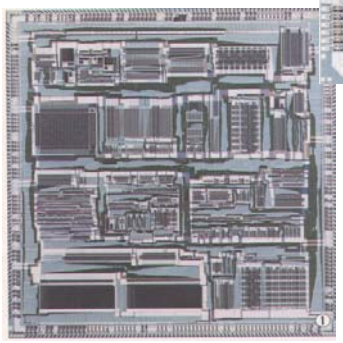


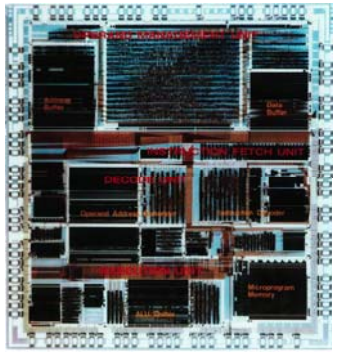
Source : Makimoto's Wave

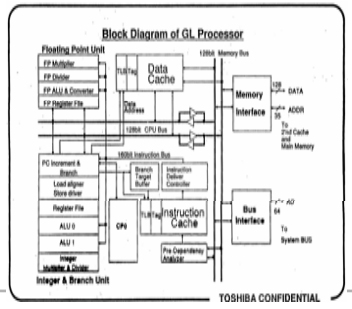
Starting ASIC, RISC Processor Era (From ‘87)

- **Starting HDL Design by Semiconductor Company’s Proprietary CAD**
- **AI Workstation (1985 to 1987)**
  - Last trial for designing processor using standard parts
- **3D Graphics Processor (from 1986)**
  - First chip using proprietary HDL CAD H^2DL、and standard Cell
  - Revolutionary design efficiency, small design team was arrowed
- **AI Processor Chip(1987 to 1988)**
  - Designed by using Silicon Compiler “Genesil”
  - Defeated by severe RISC competition with declining AI booming
- **TRON Processor (1986 to 1989)**
  - Disappeared in the CISC/RISC debates
- **GL Processor (1989 to 1991)**
  - Again relatively large team, and couldn’t reach final stage
  - Prologue to R8000



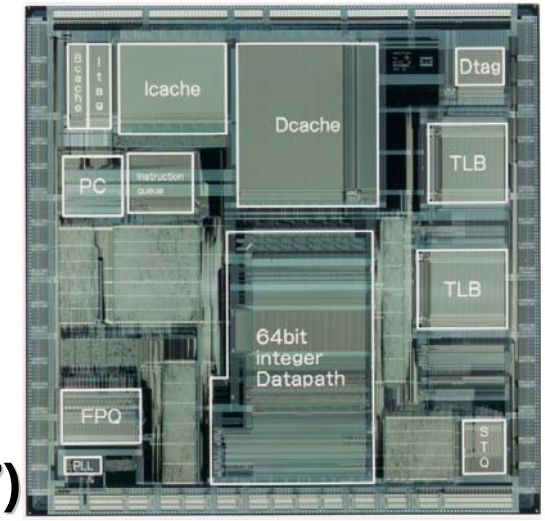




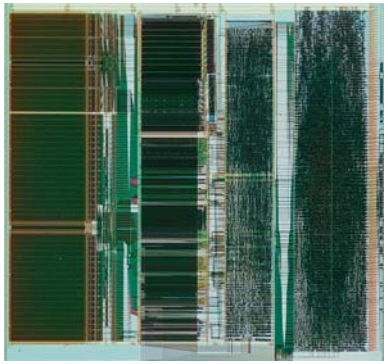


Processor Development Became a Big Project Again

- **Proprietary EDA was expelled by third party EDA vendors**
- **R8000 for Server(1991-1993)**
  - **Successor of GL Processor Team**
  - **Joint Development with Silicon Graphics Inc**
  - **Verilog HDL and logic Synthesis tool was used**
  - **Random verification and C reference model**
  - **Start of Standard EDA Era**

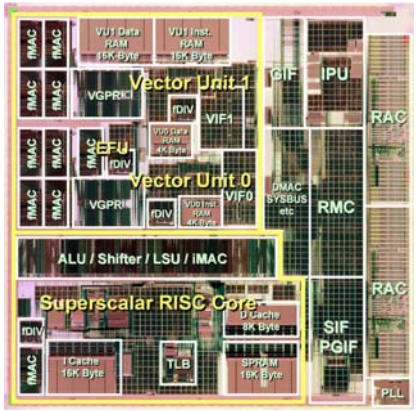


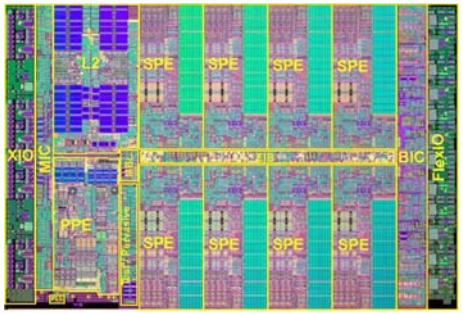
- **R10000 for Server and Workstation (1994-1997)**
  - **Very Early out of order processor**
  - **One year project delay**
  - **Big competition era**
- **TX39, 49 for Embedded Application(1993-1998)**
  - **Embedded RISC Processor raised**
  - **Good power performance**
  - **Started to have revenue, though,,**



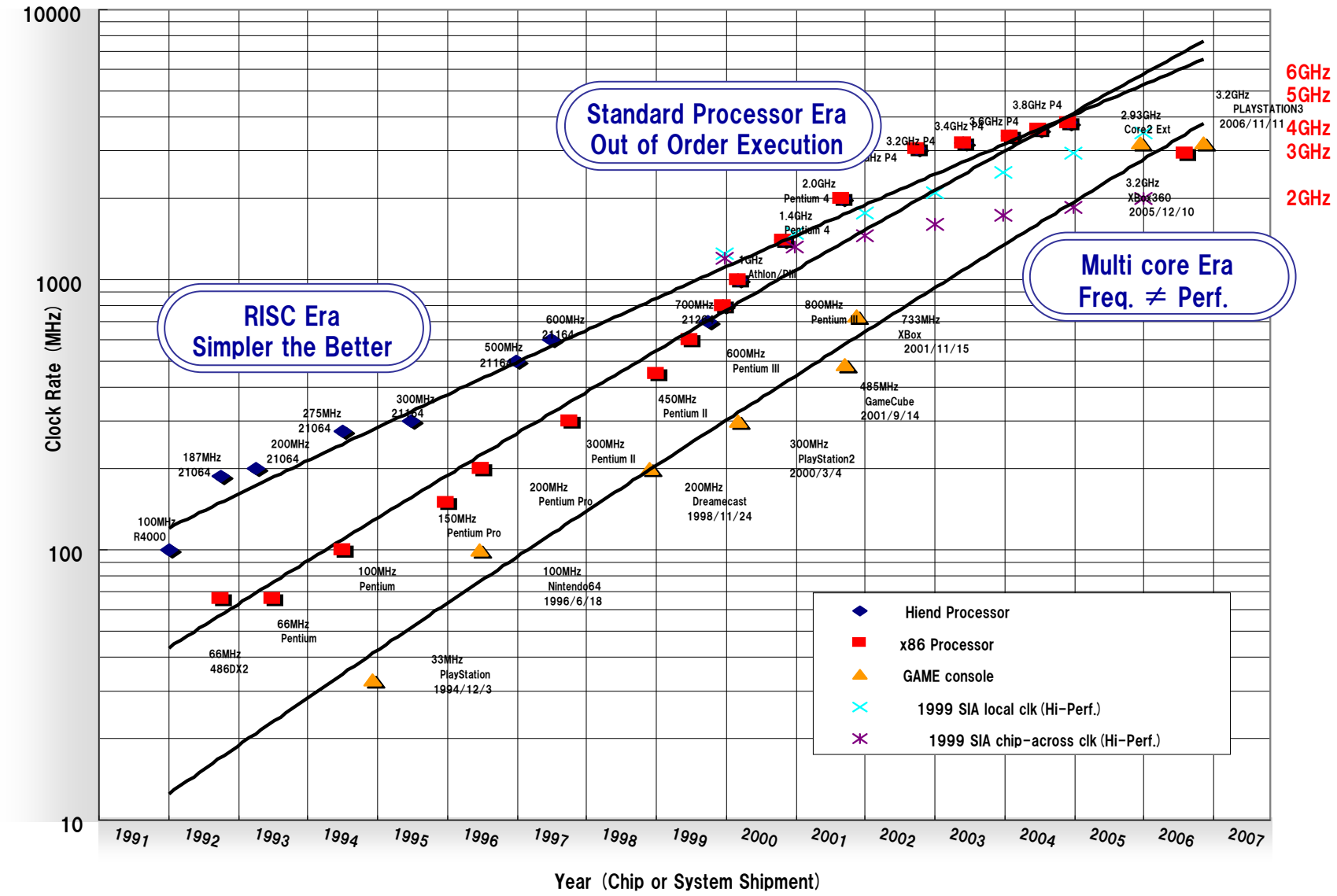
Standard Processor Era Since 1997

- For the leading edge development, proprietary EDA was necessary combining with standard flow
- X86 Architecture became standard (RISC was defeated)
  - Less advantage by super scalar architecture
  - Out of order made no advantage for RISC
- Emotion Engine(1996-1999)
  - Multi-core Architecture was adopted
  - STA, Formal Verification, Extraction
- Cell Broadband Engine(2000-2005)
  - Al most IBM Proprietary EDA was used
  - DFT, Assertion、DFM、Power Estimation
  - Was good enough for the fastest processor
  - Too early for replacing HW solution



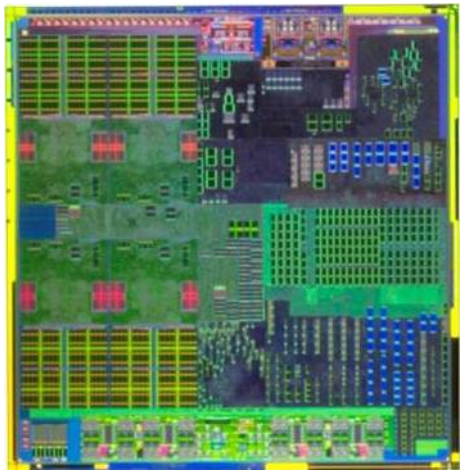


Processor Clock Rate per Year

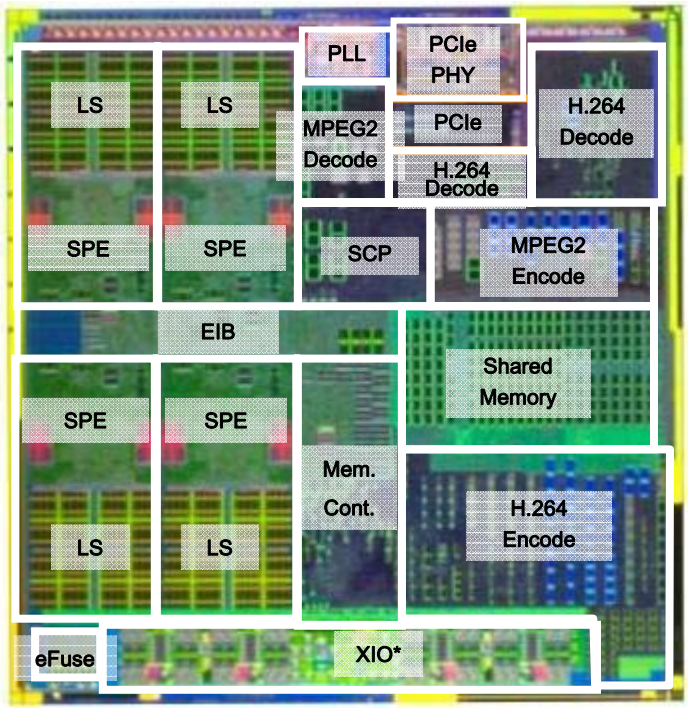


What is going on to the MPU and SOC Now?

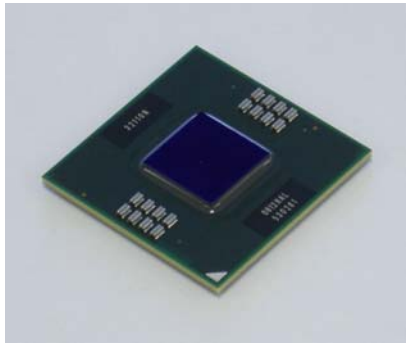
- Just Transition from Standard MPU Era to Custom SOC Era
  - Change of technology direction : Big chance in ten years
  - Out of order changed the direction ten years ago
    - RISC→CISC
  - From frequency competition to multi-core
    - Player increase by matured technology
  - What is SOC as a technology driver?
    - Combination of processor and fixed function unit
    - SpursEngine will be one of the early example
  - Big change is necessary for EDA too
    - Backend design will change too : no custom block
    - Model based design with coverage based random verification
    - High level design including software is the next key
- Manufacturing Technology is Also Changing
  - DFM is needed
  - A lot of new materials, for low power
  - New transistor structure



SpursEngine™ Physical Implementation



- **Process:**
  - 65nm bulk CMOS with 7 levels of copper layers
- **Die Size:**
  - 9.98mm x 10.31mm, 102.89mm^2
- **Fmax: 1.5GHz**
- **Transistor Counts:**
  - 239.1M
    - Logic: 134.3M
    - SRAM: 104.8M
- **TDP**
  - < 20W (depending on application sets)
- **Package:**
  - FC BGA 624



* XIO™ is trademarks of Rambus Inc. in the United States and other countries.

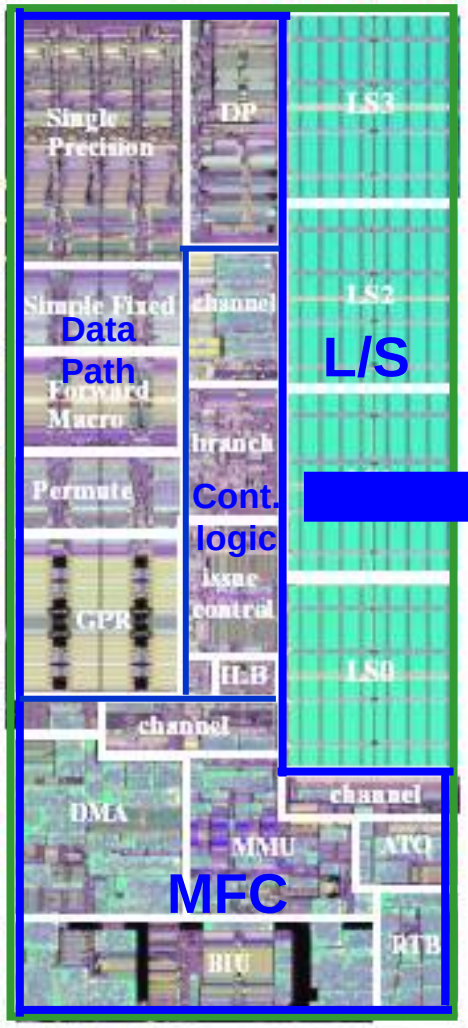
Key Design Feature: Synthesizable Over GHz SPE

- **Synthesizable design**
  - **shorter design TAT**
    - (estimation: 1/4 compared with custom migration)
  - **Technology Independent**
    - To Develop Different Target SoC
- **Key Feature**
  - **floor plan optimization**
  - **hybrid standard cell height**
  - **RTL abstraction**
  - **register retiming**
  - **semi-custom clock tree**
  - **wire width control**

Floor Plan Optimization

Original Floor Plan (Cell/B.E.™)

Cell/B.E.™ (65nm) 2.09mm x 5.30mm

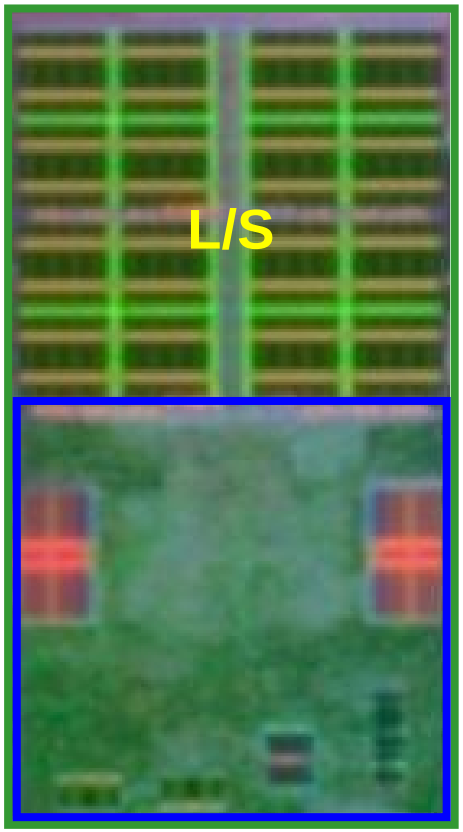


Square & Compact

- more cell placement flexibility
- area:
  - 27% smaller
- total wire length:
  - 28% shorter

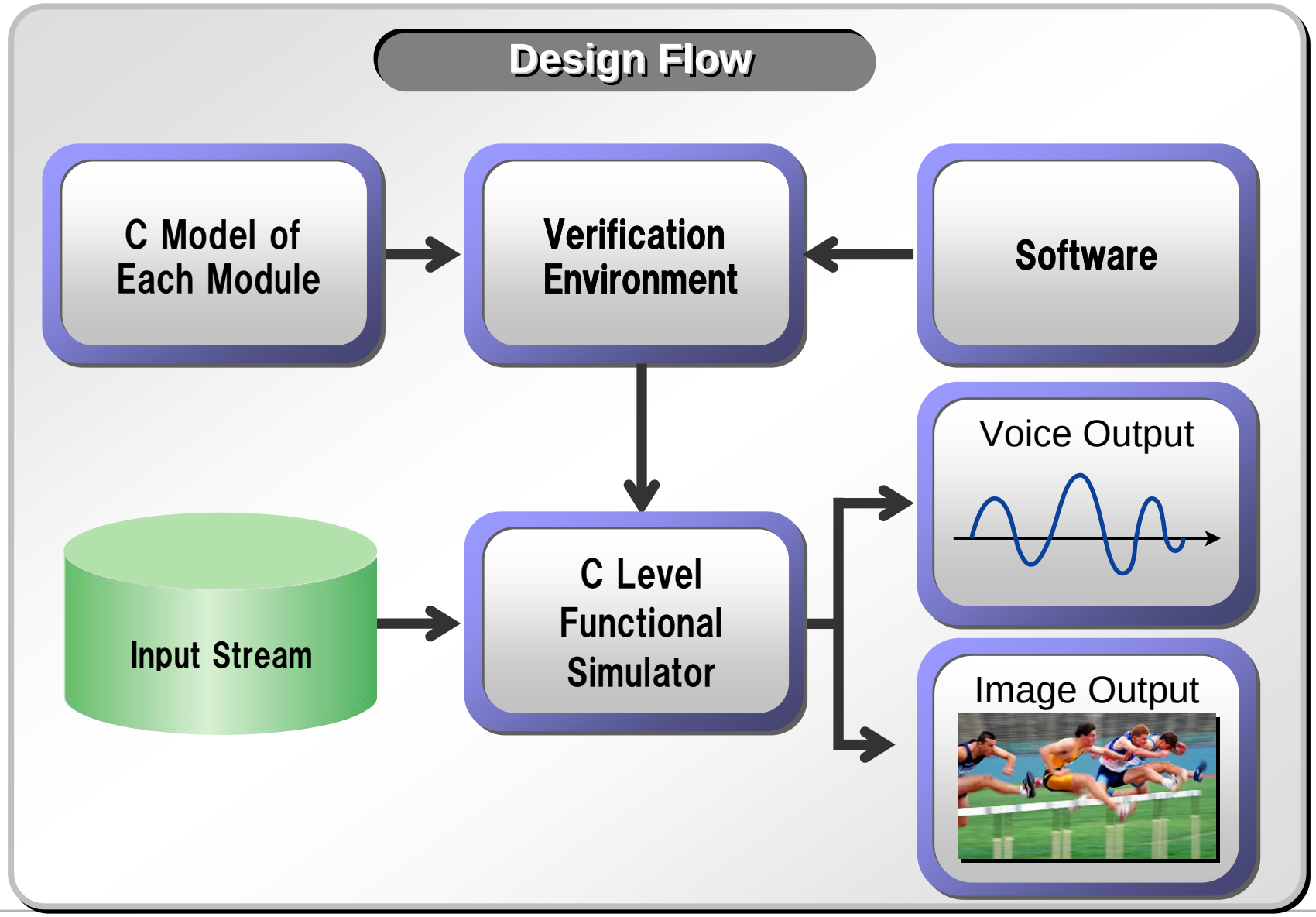
New Floor Plan

SpursEngine™ (65nm) 2.07mm x 3.93mm

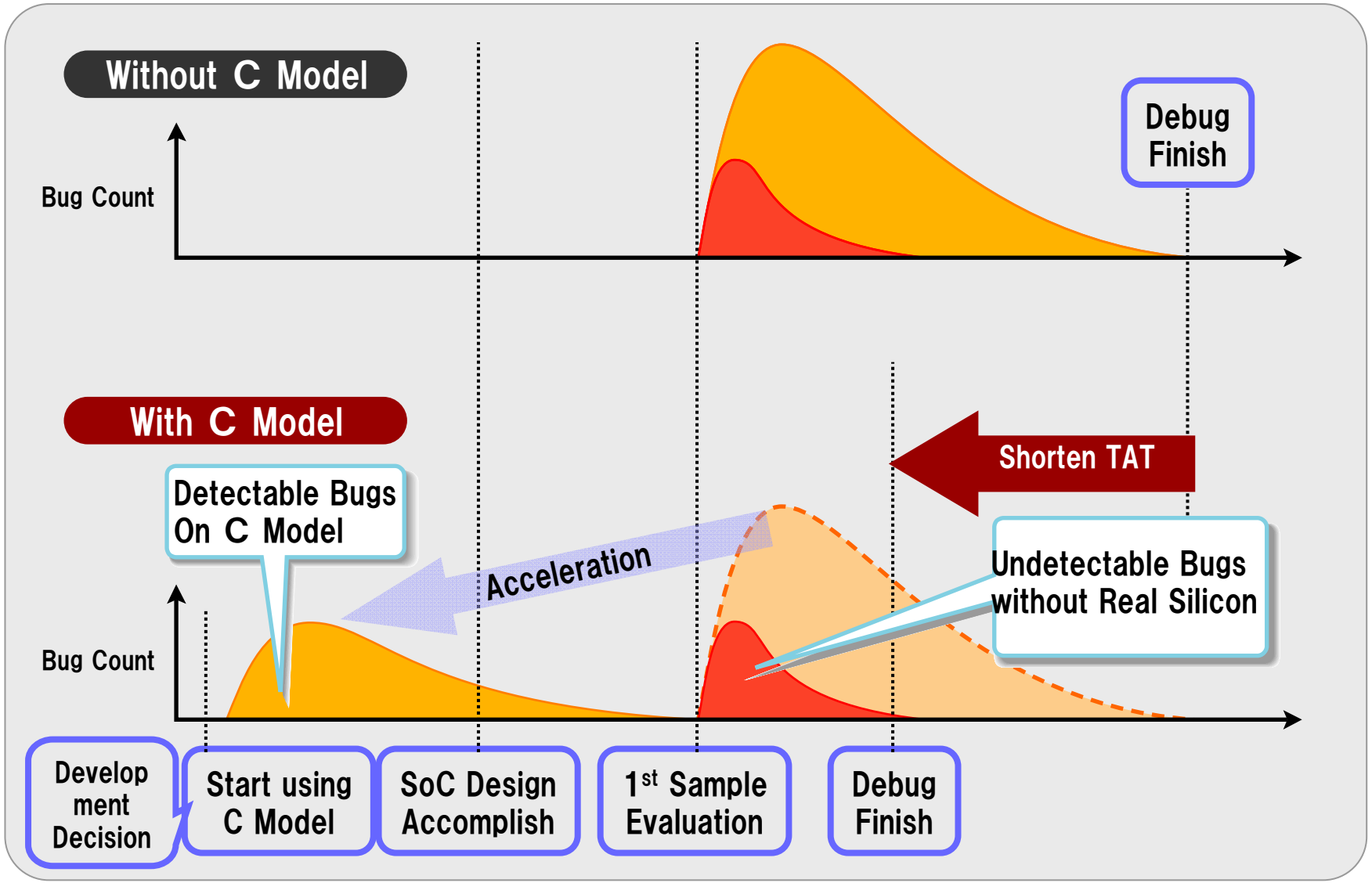


L/S : Local Storage
MFC : Memory Flow Controller

Introduction of C Model for DTV-SoC



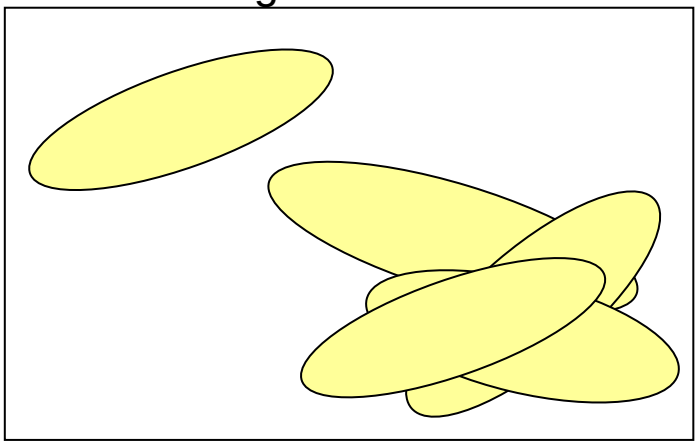
Effect of C Model : Shorten TAT



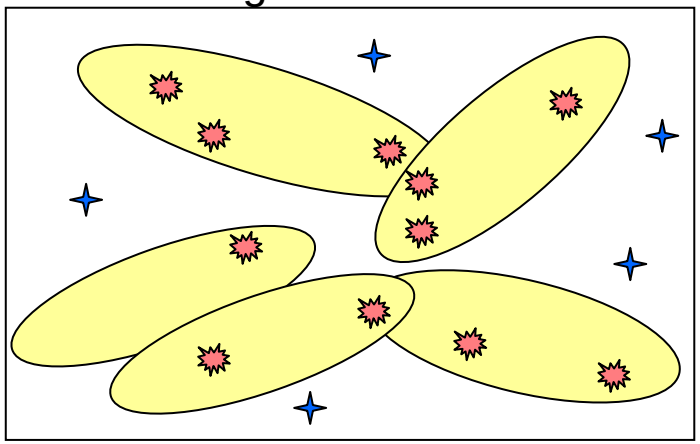
Coverage Base Random Verification

- **The limitation of Directed Test**
  - **Many good engineers are necessary to write enough test cases**
  - **Test cases must be rewritten by design changes**
  - **Cannot write unknown test cases**
- **Random Test is Mandatory though,**
  - **No hand written assembler level test cases**
  - **No way to cover all the test case**
  - **To randomize many parameters is most important thing**
  - **Simulation cycle count doesn't mean verification quality →Coverage Base verification**

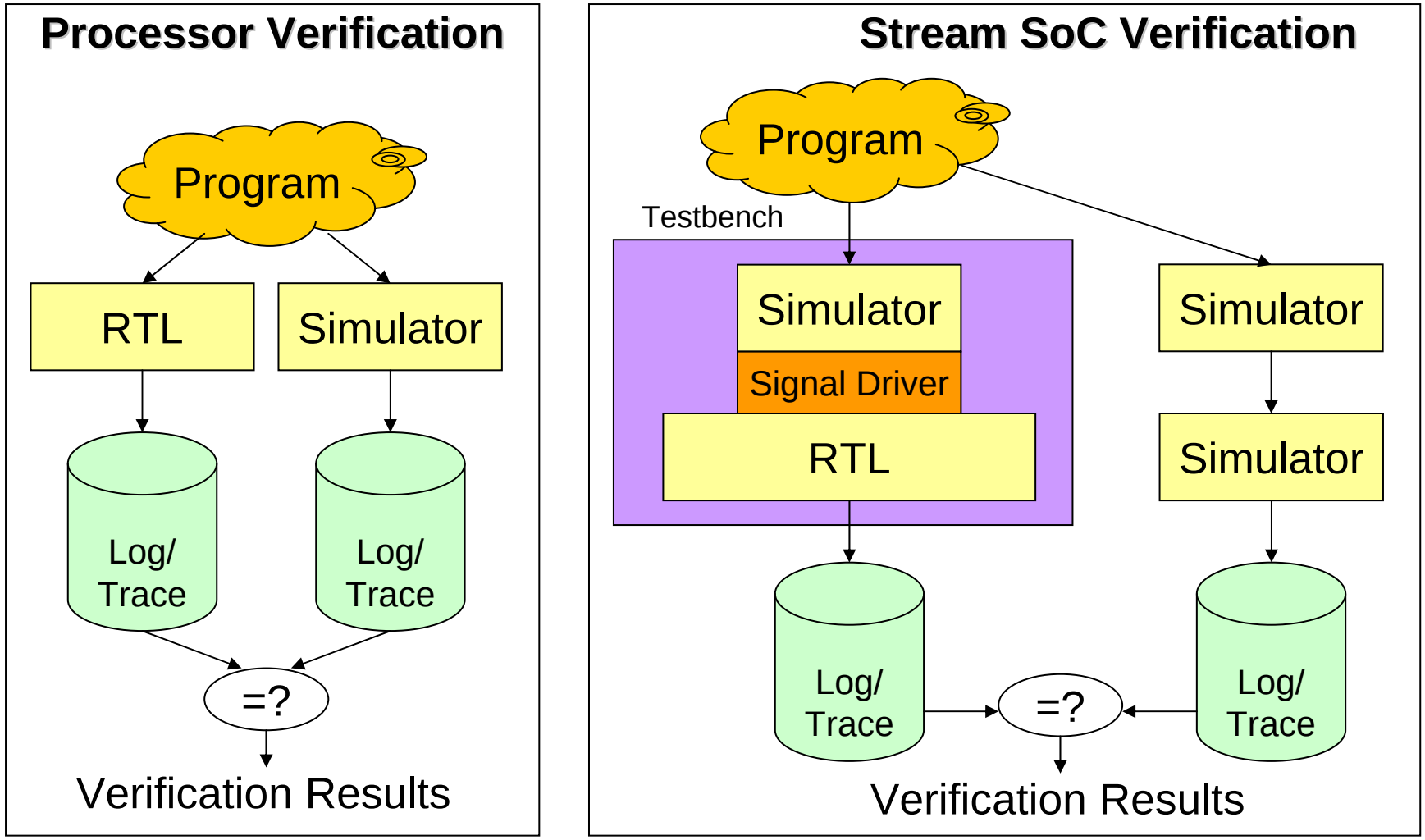
w/o Coverage



w/ Coverage

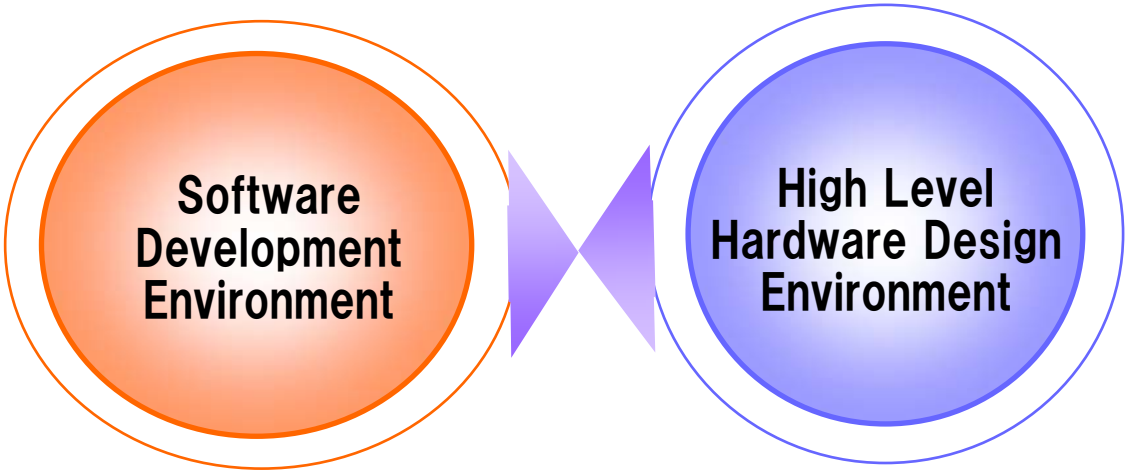


Random Simulator for SoC



EDA for Technology Driver SoC

Now, it is not considered as an EDA

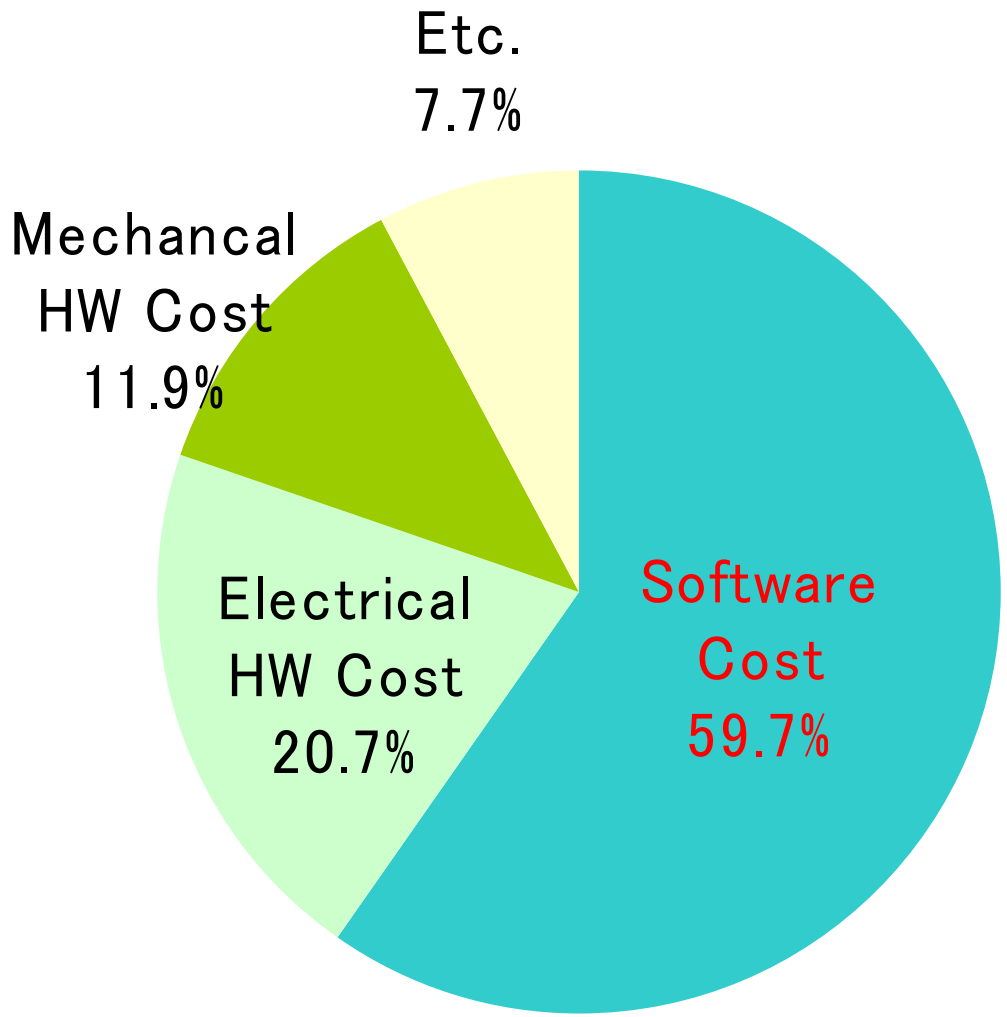


- Software environment for hardware engine control sequences
- Automatic Random vector generation
- System level development

- Highly abstracted EDA for defining algorithm and hardware architecture
- Coverage base random simulation
- Higher level description
- System level development

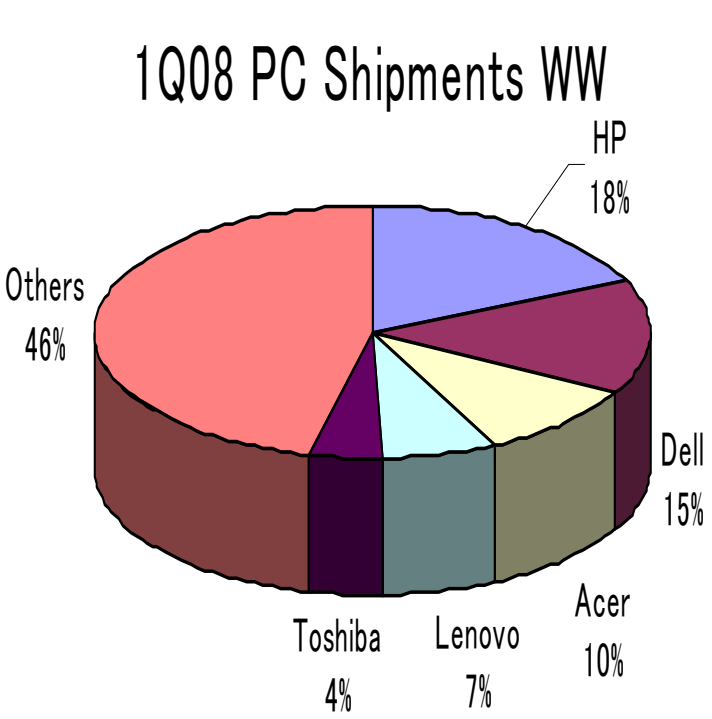
Fusion of Two Environments is the Key Point!

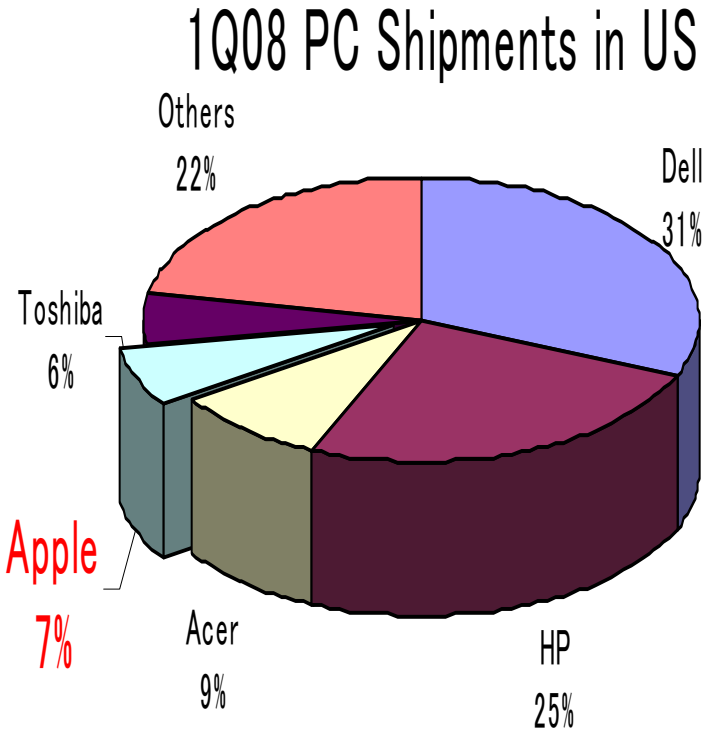
Software Development Cost is Dominant Even Today



Source : Embedded Software Investigation by METI (2007)

HW Variation is Very Effective for Software Environment





Apple is supporting proprietary OS with only 7% US market share

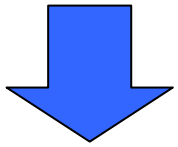
Source: Gartner (April 2008)

Towards Software Centric Era (After 2017?)

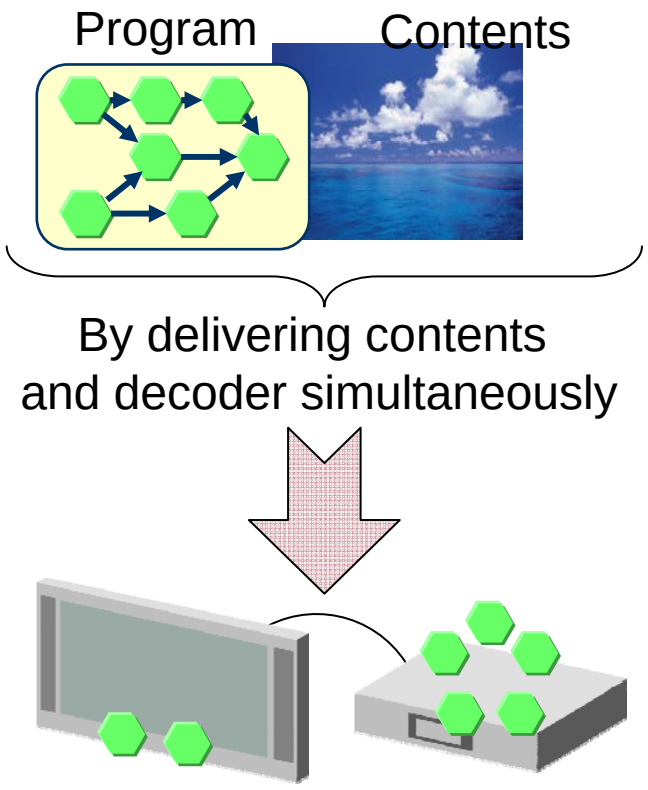
- Software Development Cost will be much more than Today
  - It will be impossible to support many platforms
- HW Design Cost will also Increase a Lot
  - Design methodology won't meet design complexity increase
  - Verification will be the critical issue
  - Single purpose LSI will not pay off any more
  - More expensive prototyping
    - Complicated mask process
- Enough Performance with Software Solution
  - Less cost and power for the same function
    - It will be possible to replace dedicated HW such as software radio
  - Protocols will be more complex and varies
    - MPEG2 lasted for 10 years, but next is confusing such as H264,DIVX,VC1
    - MPEG4 varies more than 20 derivatives
    - Voice Codec are innumerable (AAC3,MP3,WMA,,,,)
  - Softness will have bigger advantage
- New Revolution will be Necessary for After Software Centric Era

Software solution of HW makes possible to….

- **Freedom from standardization**
- **Quick service startup with new technology becomes possible**

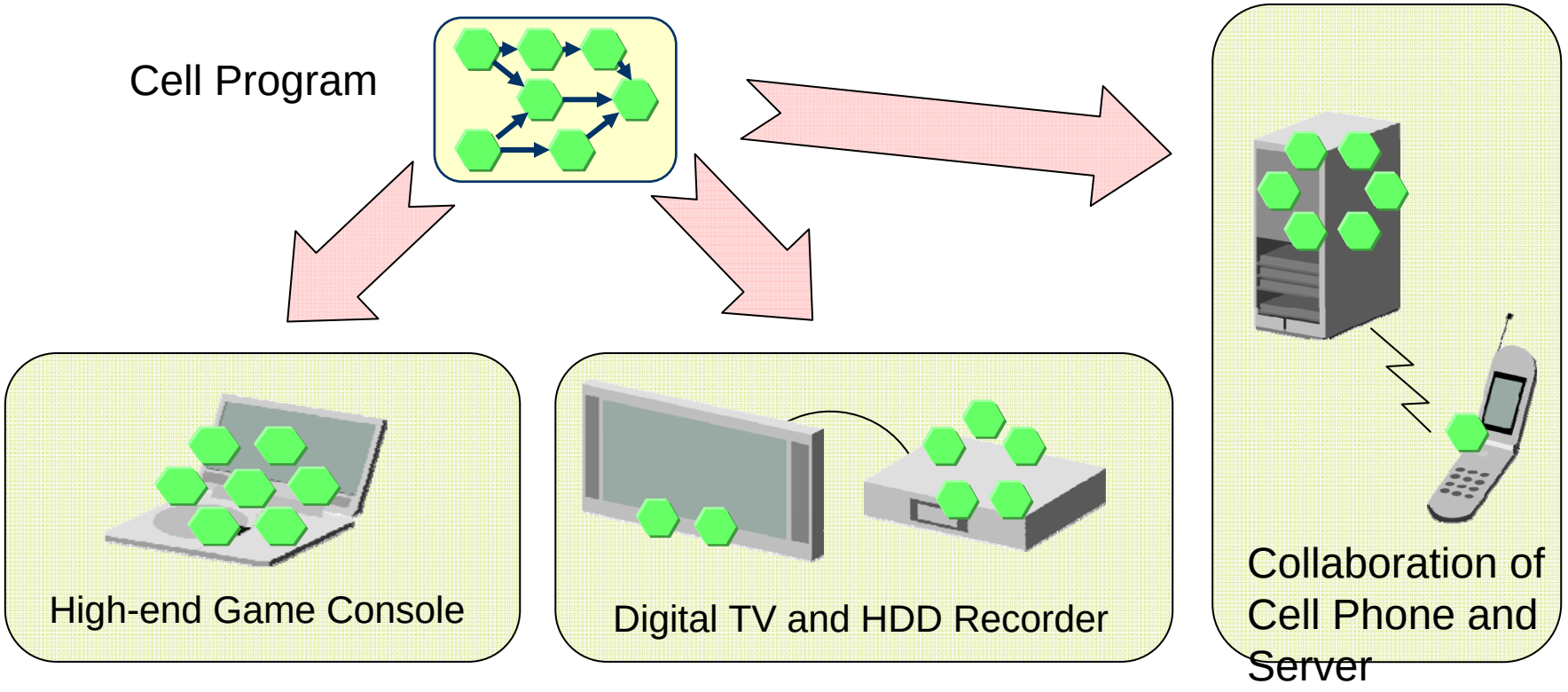


- **Proprietary Contents delivery**
  - **Better compression technology than standard**
  - **Hi-level Contents protection**
  - **Apply various charging system**
  - **Efficient usage of Network Infrastructure**
- **Communication with proprietary protocol**
- **Proprietary cipher system**

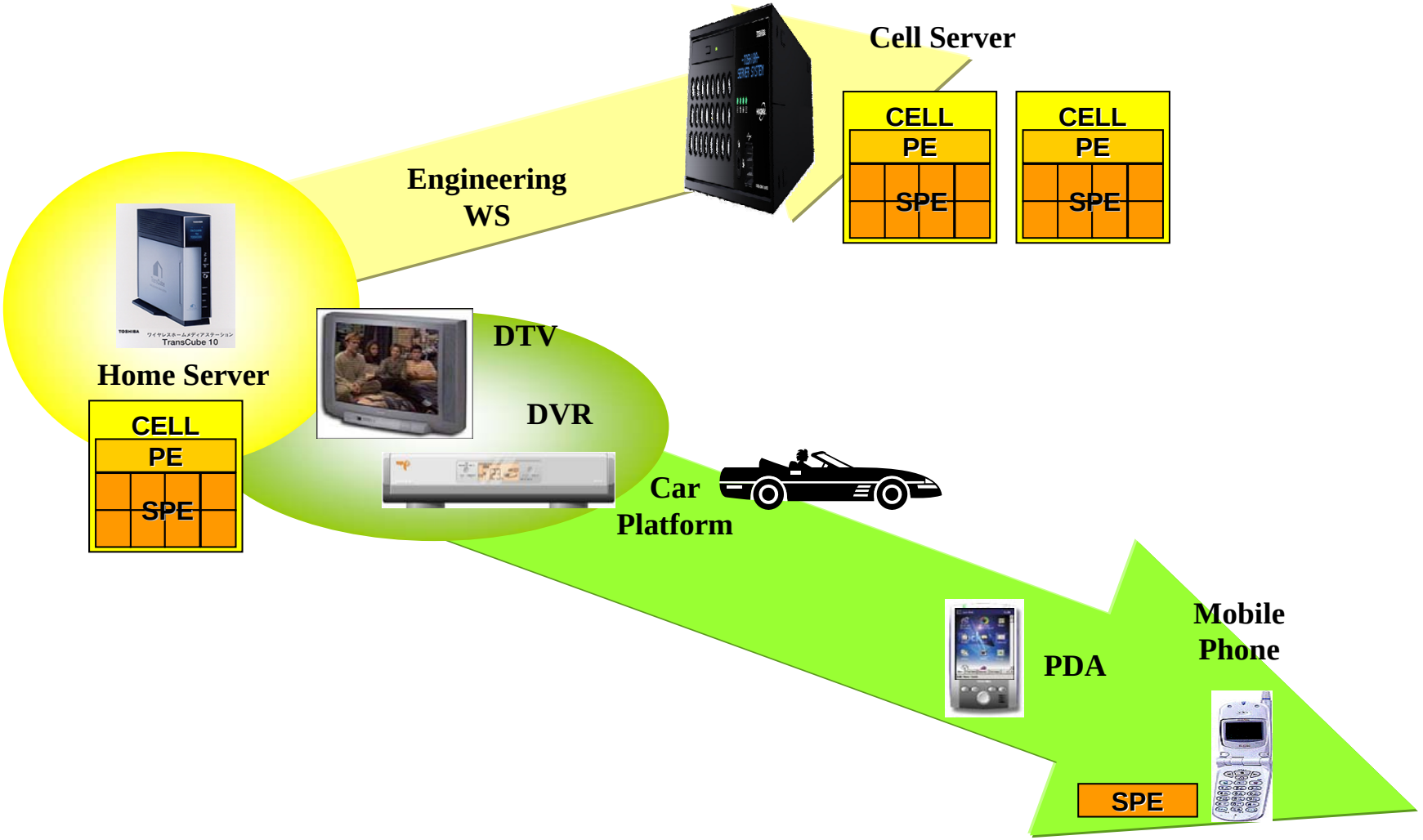


Network Transparent Model Makes…

- **Heavy function is achievable by collaborating multiple machines on the network**
- **Same Program is applicable to various performance machines with keeping real-time-ness from Cell phone to Server**

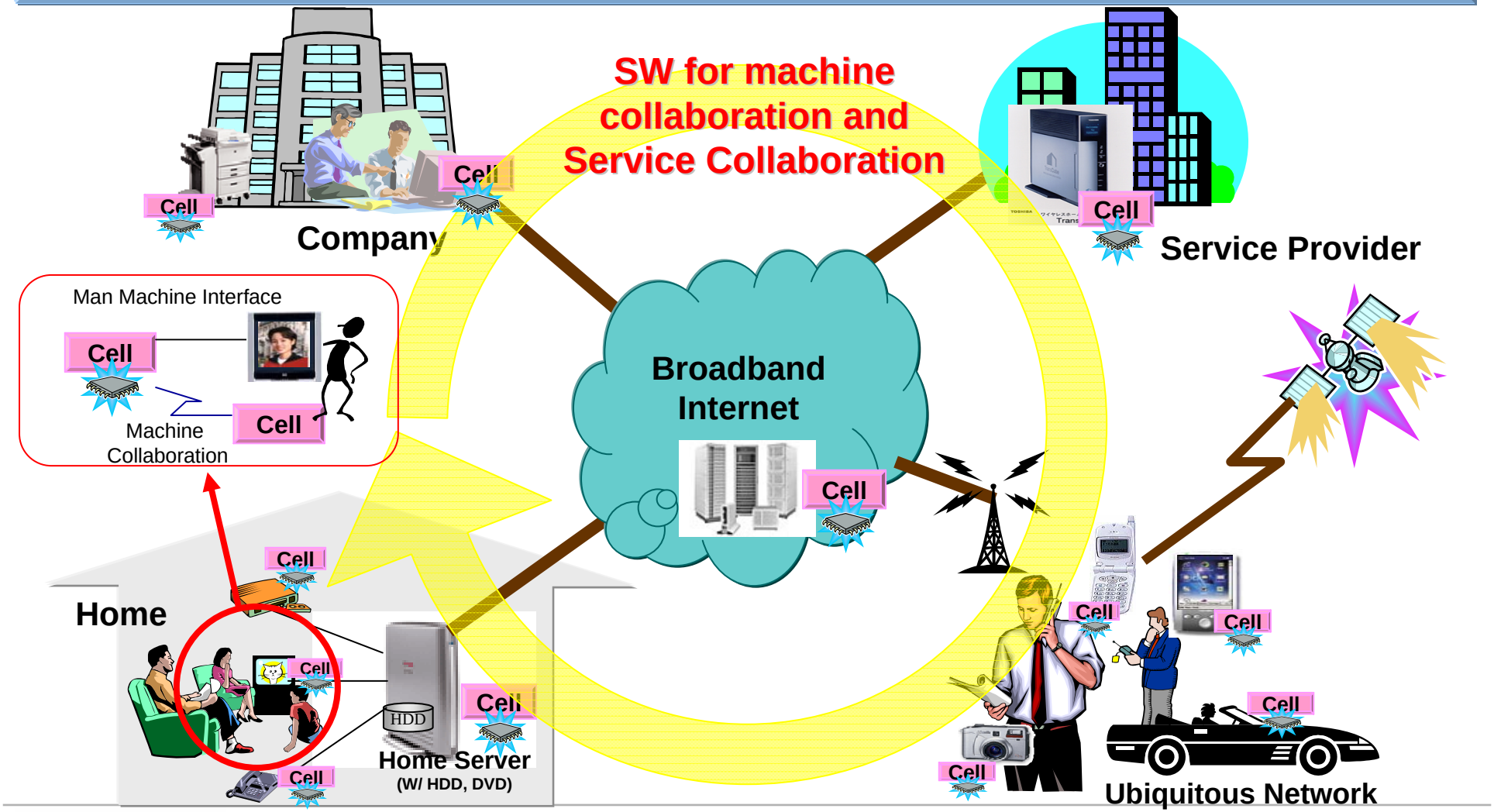


Scalability of Cell BE



Towards Cell World

**By taking advantage of overwhelming performance,
Cell BE is aiming at the new software standard world**



Summary

- **Semiconductor Roadmap is Straight Forward, But application is not**
  - **Moore's Law is forever!?**
  - **Technology Driver is changing**
  - **Makimoto's Wave is still surviving**
- **Our Microprocessor Development History was Also Following the Wave**
  - **Design Methodology is Dramatically Effective for this Wave**
  - **Requirement for EDA for Technology Driver was Changing**
    - Description, Timing, Backend, Verification
  - **Positioning of Emotion Engine and Cell was Standard Processors**
- **Today is Transition from Standard Processor to SoC**
  - **No More Frequency Increase**
  - **Need Purpose Oriented SoC's**
  - **SpursEngine is One of the Typical Example**
  - **Verification Methodology for Processor began to be applied for designing SoC's**
  - **Needs High Level and Software Oriented Design Environment**
- **Next Wave will be Software Centric**
  - **Will take some more time for new revolution after software era**
- **Take Advantage of Today's Transition**

Crisis = 危機

- Danger
- Chance

Transition = 変転

- Change
- Revolution

Cell Everywhere!!

Thank you