IEICE VLD Student Forum
at
14th Asia and South Pacific Design Automation Conference
(ASP-DAC 2009)
January 21, 2009
Pacifico Yokohama, Yokohama, Japan
Call for Posters

Committee Members:

Co-Chairs:

Yasuhiro Takashima
(University of Kitakyushu, Japan)

Ting-Chi Wang
(National Tsing Hua University, Taiwan)

Poster Selection Committee Members:
Koji Hashimoto
(Fukuoka University, Japan)
Tohru Ishihara
(Kyushu University, Japan)
Kazuhito Ito
(Saitama University, Japan)
Yih-Lang Li
(National Chiao Tung University, Taiwan)
Chien-Nan Jimmy Liu
(National Central University, Taiwan)
Yung-Hsiang Lu
(Perdue University, United States)
Nozomu Togawa
(Waseda University, Japan)
Chun-Yao Wang
(National Tsing Hua University, Taiwan)
David Wu
(Chinese University of Hong Kong, Hong Kong)
Chia-Lin Yang
(National Taiwan University, Taiwan)

Advisory:
Farzan Fallah
(Fujitsu Labs. of America, USA)
Atsushi Takahashi
(Tokyo Institute of Technology, Japan)

ASP-DAC liaison:
Yasuhiro Takashima
(University of Kitakyushu, Japan)

The Student Forum at ASP-DAC 2009 is a poster session for graduate students to present their research work. This is a great opportunity for students to get feedback and have discussion with people from academia and industry. Travel grants will be provided for some of the students attending the forum and awards will be given to outstanding presentations. Please check the website for updates.

URL: http://www.aspdac.com/aspdac2009/student_forum/index.html

Eligibility:
Graduate students are eligible for the Student Forum.

Important Dates:

Submission Deadline	October 27, 2008
Notification Date	November 24, 2008
Forum Date	January 21, 2009 12:20-13:30

Submission Requirements:

1. Abstract of the poster presentation including name, advisor, institution, contact information, estimated graduation date, track number, figures, tables and bibliography (if applicable). The abstract must be at most two pages (hard limit).
2. A list of all papers related to the poster presentation authored or co-authored by the student, including posters in Ph.D Forum at DAC or DATE and Student Forum at ASP-DAC.
3. A published supporting paper authored or co-authored by the student and related to the poster presentation.

Please send the above, to merge them into one pdf file if possible, to Yasuhiro Takashima: vld-student-forum09 @ mail.ieice.org.

Please Note:

- Abstracts of completed research as well as research in early stages can be submitted.

- Submitted abstracts will be reviewed by the poster selection committee. The following points will be mainly taken into account in the review process in addition to the normal paper selection criteria:
  (1) Achievements and methodologies for a completed (or almost completed) research.
  (2) Directions and potentials for research in the early stages.

- The poster selection committee gives the priority to the abstracts that meet the following criteria:
  (1) Achievements and methodologies are supported by experiments.
  (2) Directions and potentials are supported by feasibility analysis.
  (3) It has not been presented at the Ph.D. Forum at DAC or DATE or the Student Forum at ASP-DAC.

- The abstract must be in .pdf format. The font should not be smaller than 10 points. Please make sure all pages print well.

- The abstract must be well organized and should not have any spelling error.

- The bibliography and the list of published papers must be in IEEE style
  (See http://www.ieee.org/web/publications/authors/transjnl/index.html).

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Tracks:

[1] System-Level Design Methodology:
System modeling, specification, language, design methodology, performance analysis, hardware-software co-design/co-simulation/co-verification, HW-SW interface synthesis, IP/platform-based design, etc.

[2] System Architecture and Optimization:
System-on-Chip and multi-processor SoC (MPSoC) architecture design, low power system design, network on chip, system communication architecture, memory architecture, application-specific instruction-set processor (ASIP) synthesis, virtual platforms, etc.

[3] Embedded and Real-Time Systems:
Embedded system design, real-time system design, OS, middleware, compilation techniques, memory/cache optimization, interfacing and software issues

[4] High-Level/Behavioral/Logic Synthesis and Optimization:
High-Level/behavioral/RTL synthesis, technology-independent optimization, technology mapping, interaction between logic design and layout, sequential and asynchronous logic synthesis, resource scheduling, allocation, and synthesis

[5] Validation and Verification for Behavioral/Logic Design:
Logic simulation, symbolic simulation, formal verification, equivalence checking, transaction-level/RTL and gate-level modeling and validation, assertion-based verification, coverage-analysis, constrained-random testbench generation

[6] Physical Design (Routing):
Routing, repeater issues, interconnect optimization, interconnect planning, module generation, layout verification, post-placement layout and optimization, clock network design.

[7] Physical Design (Placement):
Placement, floorplanning, partitioning, hierarchical design, interaction between physical design and logic synthesis.

[8] Timing, Power, Thermal Analysis and Optimization:
Deterministic and statistical static timing analysis, statistical performance analysis and optimization, low power design, power and leakage analysis, power/ground and package analysis and optimization, thermal analysis, etc.

[9] Signal/power Integrity, Interconnect/Device/Circuit Modeling and Simulation:
Signal/power integrity, clock and bus analysis, interconnect and substrate modeling/extraction, package modeling, device modeling/simulation, circuit simulation, high-frequency and electromagnetic simulation of circuits, etc.

[10] Design for Manufacturability/Yield and Statistical Design:
DFM, DFY, CAD support for OPC and RET, variability analysis, yield analysis and optimization, reliability analysis, design for resilience and robustness, cell library design, design fabrics, etc..

[11] Test and Design for Testability:
Testable design, fault modeling, ATPG, BIST and DFT, memory test and repair, core and system test, delay test, analog and mixed signal test.

[12] Analog, RF and Mixed Signal Design and CAD:
Analog/RF synthesis, analog layout, verification and simulation techniques, noise analysis, mixed-signal design considerations

[13] Emerging technologies and applications
(i) System-level design case studies for emerging applications: multimedia, consumer electronics, communication, networking, ubiquitous computing, biomedical applications, etc.
(ii) Post CMOS technologies: nanotechnology, quantum, optical interconnect, 3D integration, probabilistic architecture, microfluidics, molecular, bioelectronics, etc., with emphasis on modeling, analysis, novel circuit/architecture, CAD tools, and design methodologies.

Sponsor :
IEICE ESS Technical Group on VLSI Design Technologies

Supported by :
ASP-DAC 2009

Contact Information:
Should you have any questions, please send e-mail to Yasuhiro Takashima: vld-student-forum09 @ mail.ieice.org.