Temporal Circuit Partitioning for a 90nm CMOS Multi-Context FPGA and its Delay Measurement

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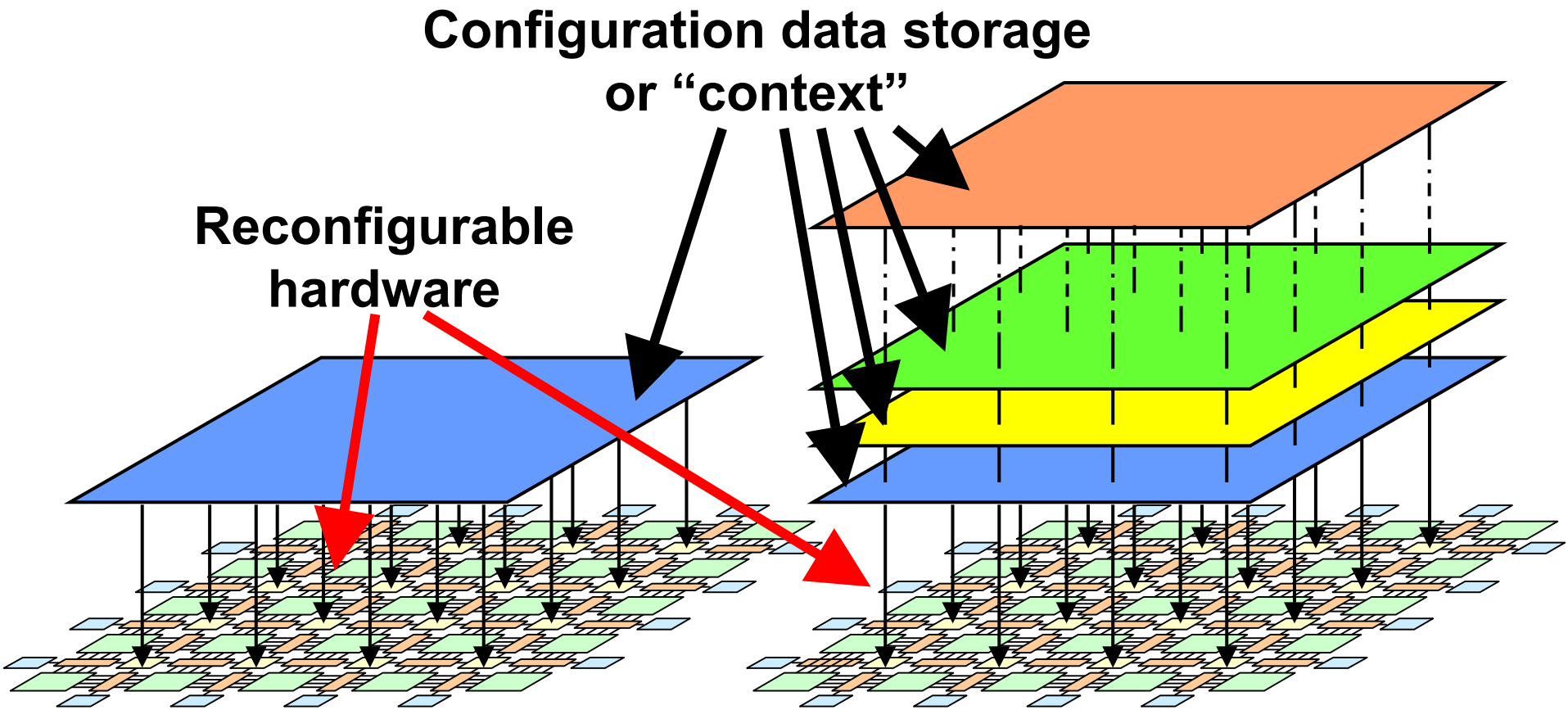
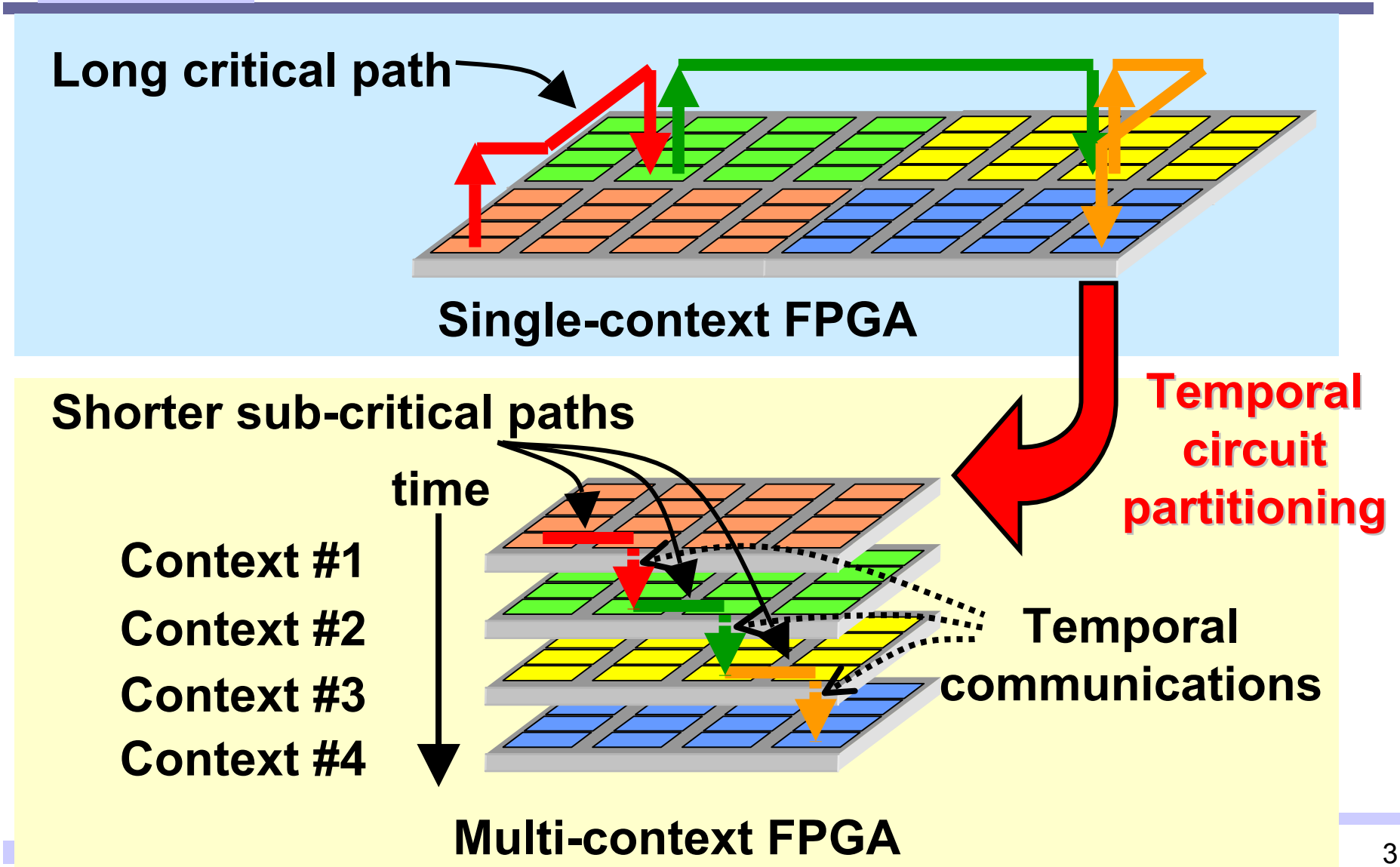
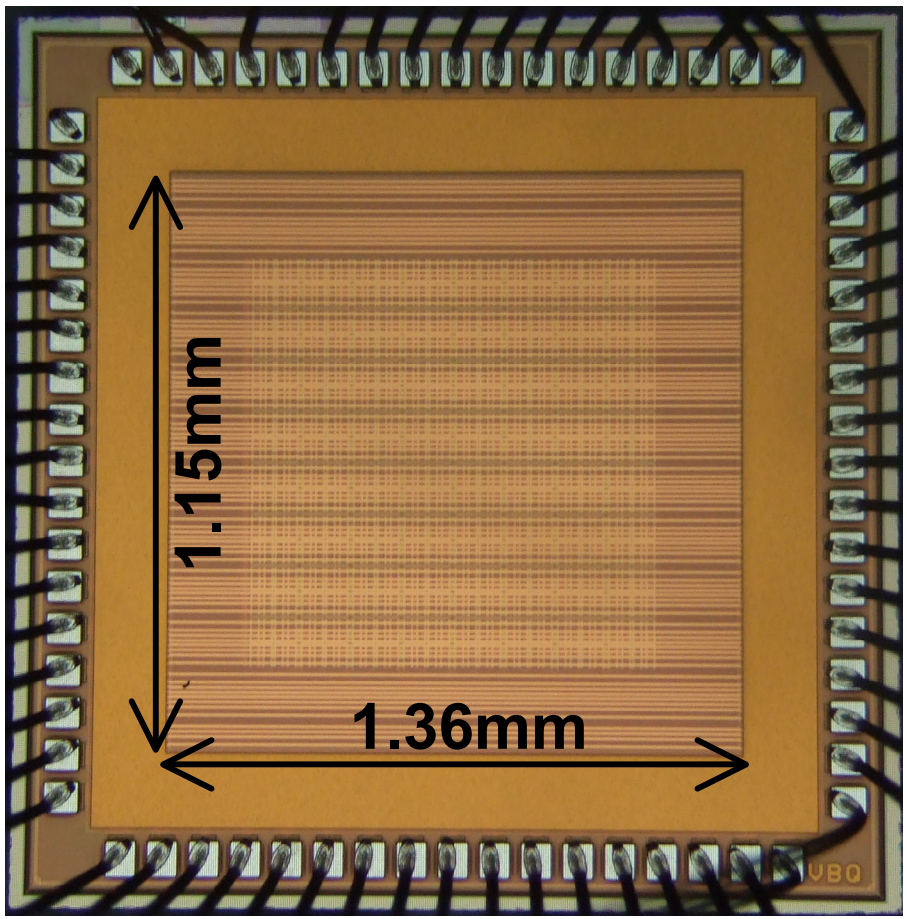
Multi-Context FPGA



Temporal Circuit Partitioning



90nm CMOS Multi-Context FPGA



Process Technology

90nm CMOS
1-layer poly
6-layer metal

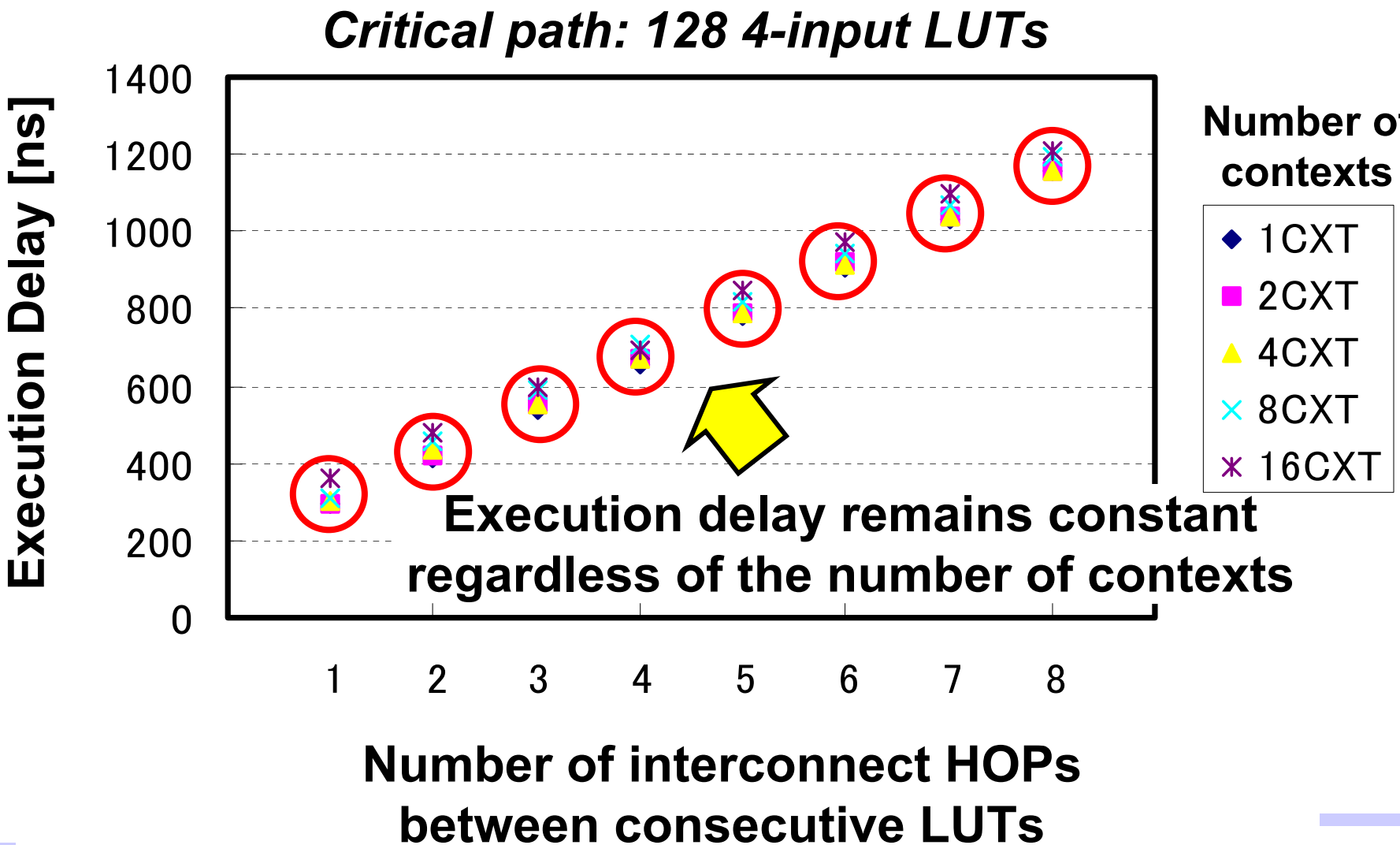
Specifications

16 Contexts
16 x 16 Logic elements
16 x 4 User I/Os

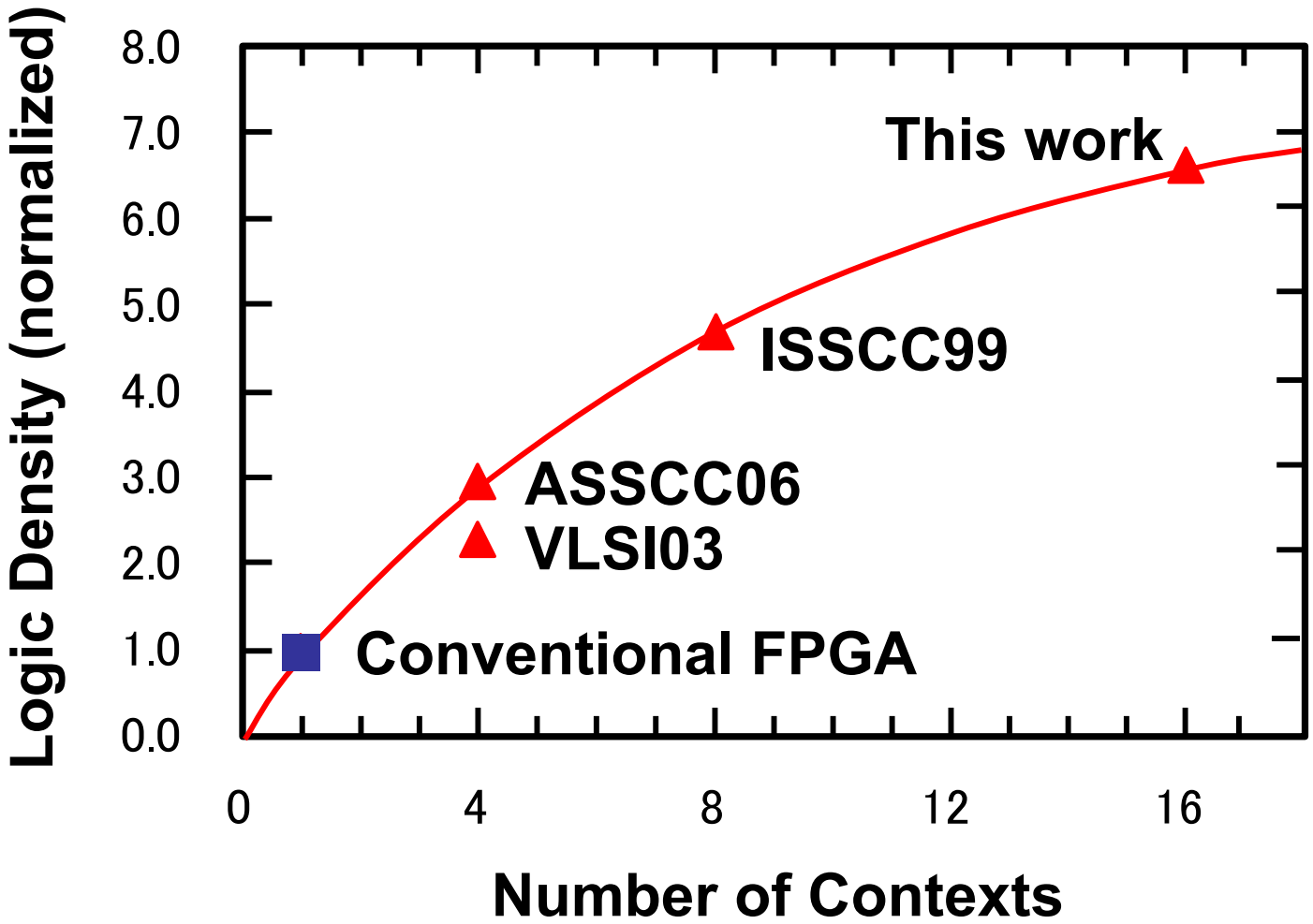
Operation Condition

Core: 1.0V
I/O: 2.5V

Delay Measurement Results



Logic Density Comparison



Conclusions

- We present a 90nm CMOS multi-context FPGA.
- Temporal circuit partitioning has been proposed, which divides a long critical path into a set of shorter paths for the multi-context FPGA.
- From measurement results, it is found that the execution delay remains constant regardless of the number of contexts.
- Moreover, logic density of the multi-context FPGA is larger than conventional FPGA by a factor of 7.

Thank you for your kind attention,
and I'm looking forward to the poster discussion!!