

HIROSAKI UNIV
VLSI PROJECT



Design and Chip Implementation of an Instruction Scheduling Free Ubiquitous Processor

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➤ VLSI trend

- ✓ Not high clock speed but power conscious high performance
- ✓ Parallelism

➤ H/S collaboration parallelism

- ✓ Hardware parallelism
 - Multicore
 - Multiple pipeline
 - Not only integer but also floating point arithmetics for multimedia computing
- ✓ Software support
 - Parallelizing compiler
 - TLP/ILP abstraction
 - Instruction scheduling for arithmetics
 - Performance degradation due to pipelining disturbance

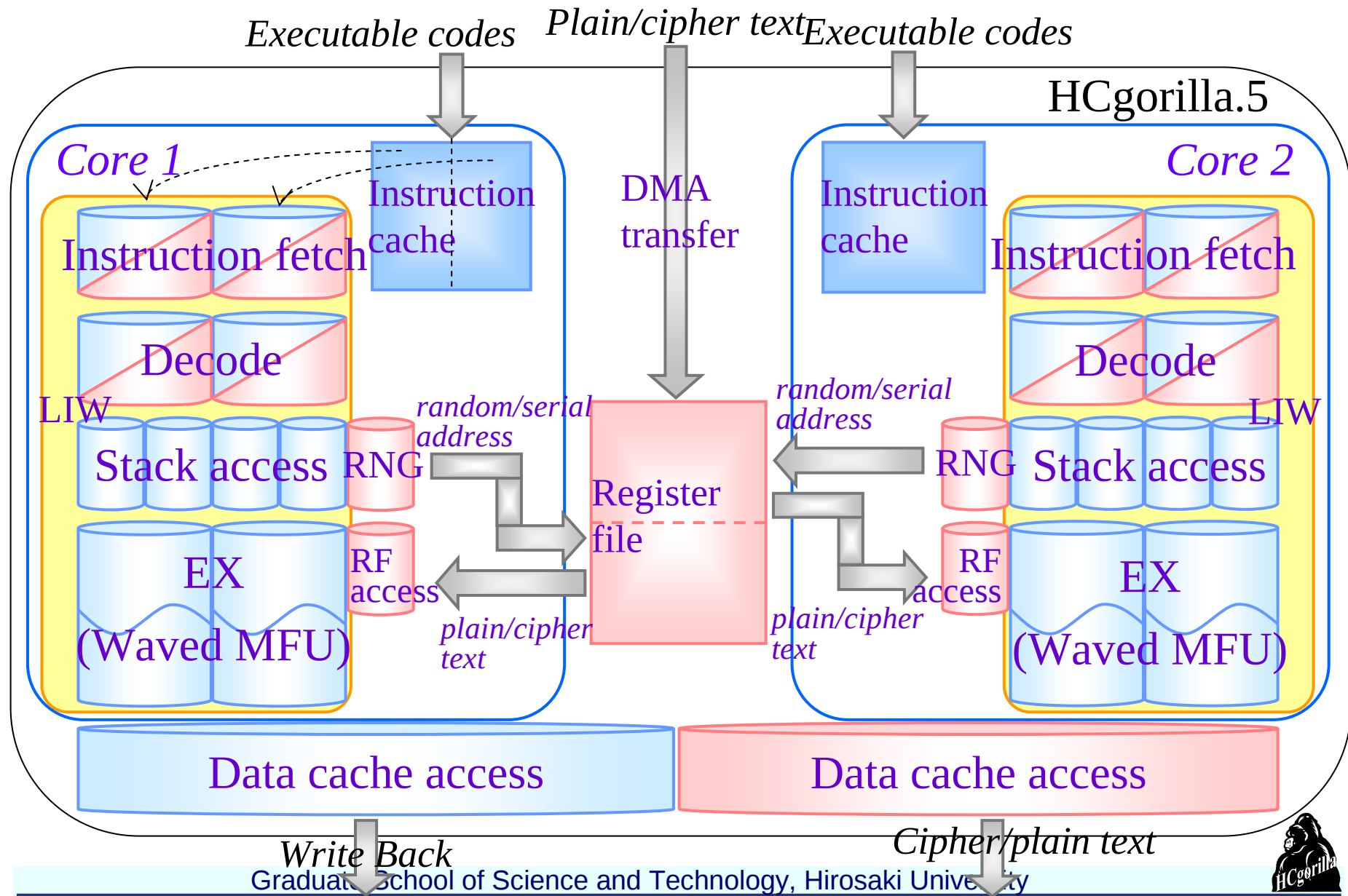
Research objective

- Compact scheme for arithmetic parallelism
- Instruction scheduling free (out-of order) hardware parallelism
 - ✓ Double scheme
 - Merge of scalar units (IU, FPU)
 - Wave-pipelining of the resultant MFU
 - ← Power conscious speedup
 - ✓ Parallelization of multifunctional media pipes
 - ✓ Support the by an LIW compiler for ILP extraction
- HCgorilla chip implementation

Specifications of HCgorilla family

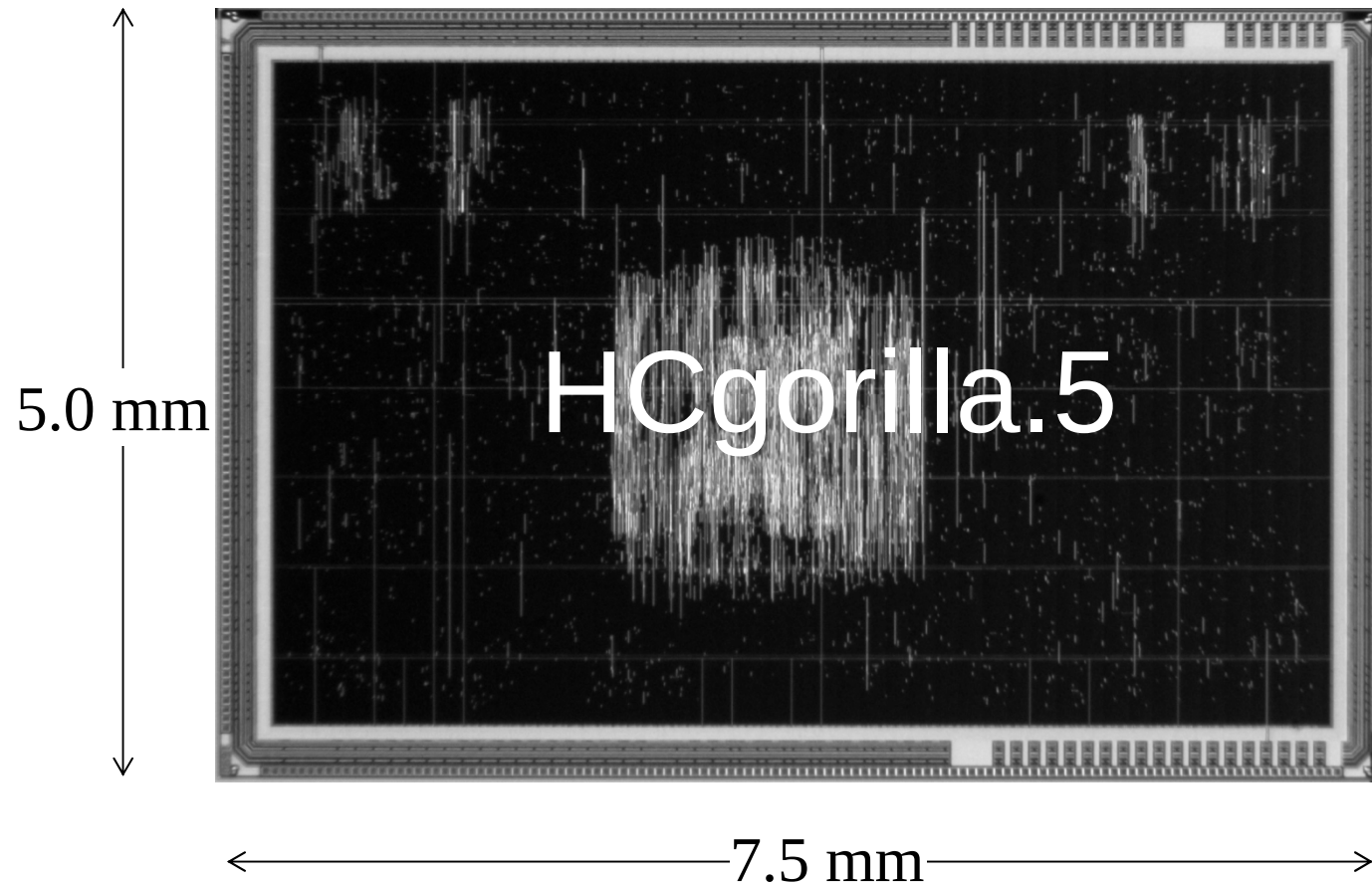
Chip version				HCgorilla.3	HCgorilla.4	HCgorilla.5		
Design Rule				ROHM 0.18 μm CMOS				
Per processor	Chip area			5.0 mm × 7.5 mm				
	Power Supply			1.8 V (I/O 3.3 V)				
	Power consumption			241 mW		274 mW		
	Clock frequency			330 MHz	400 MHz	200 MHz		
	Instruction cache			2 byte × 32 word × 2		2 byte × 64 word × 2		
	Data cache			2 byte × 128 word		2 byte × 128 word × 2		
	Stack memory			2 byte × 8 word × 4		2 byte × 16word × 8		
	Register file			2 byte × 64 word		2 byte × 128 word		
	No. of cores			2				
Per core	Pipeline	Media	Number		2			
			EX	IU	2-wave × 2		2-wave MFU × 2	
				FPU	NA	5-clock × 2		
			No. of stacks		1		2	
			ILP degree		2		4	
			Throughput			0.07-0.09 GIPS	0.13 GIPS	
			Java bytecode		61	77	58 (102)	
		Cipher	Number		1			
			RNG		4-bit LFSR		6-bit LFSR	
			Throughput		0.1-0.2 GOPS			
			SIMD code		2			
		Remarks				ASP-DAC 2009	Synthesis	ASP-DAC 2010

Organization of HCgorilla.5





HCgorilla.5



VDEC Annual Report 2009



Running time of an arithmetic test program

