Rapid Prototyping on a Structured ASIC Fabric

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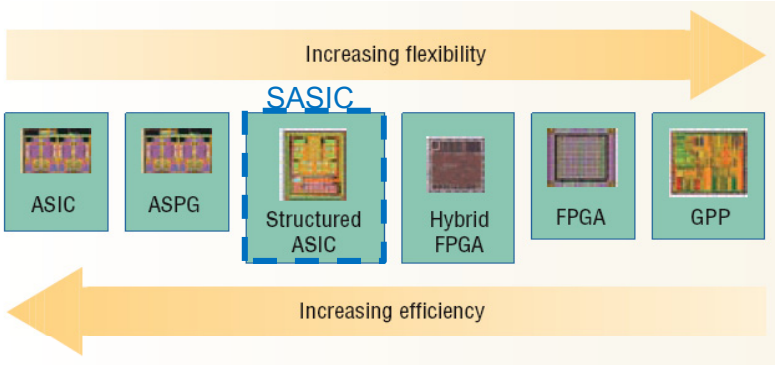
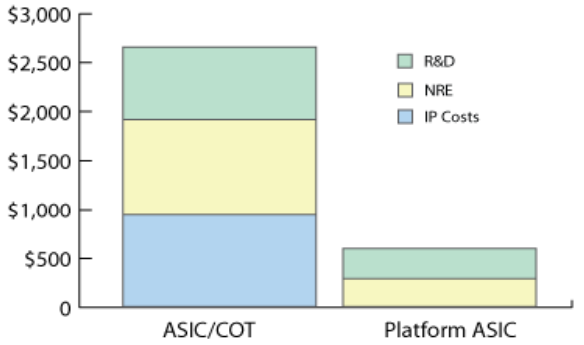


Source: Lach, J., Application-Specific Product Generics, IEEE Computer, Volume 42, Issue 8, Aug 2009 Page(s): 64-74

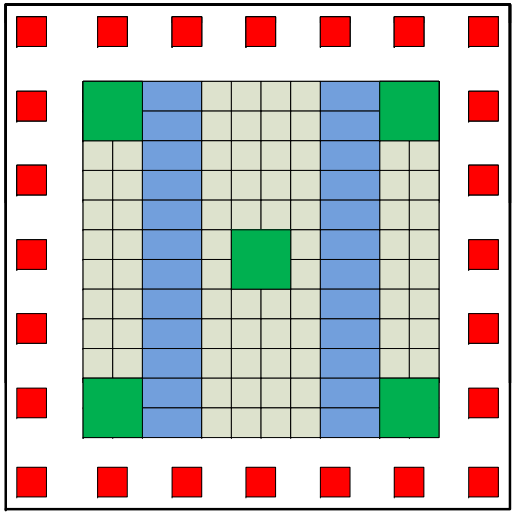
- Structured ASIC (SASIC) is intermediate silicon product between ASIC and FPGA.
- Structured ASIC reduces the development cost by sharing between customers:-
  - Mask set NRE
  - IPs
  - R&D effort
  - Risk for re-tapeout
  - Time-to-market

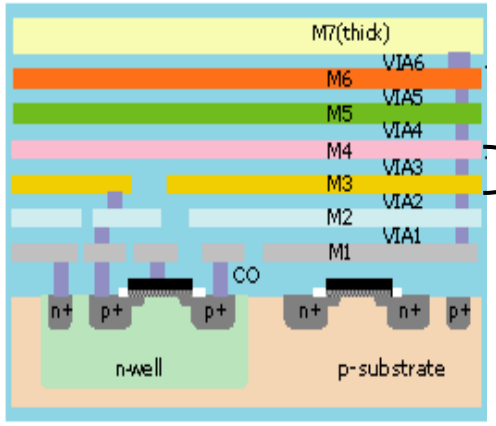


Source: http://www.faraday-tech.com/html/products/structuredASIC.html

ARCHITECTURE AND DEVICE

- Three types of structured elements
  - Lookup Table (LUT)
  - Sequential element, e.g. D-type Flip-flop
  - Embedded block, e.g. RAM/ROM
- Programmability
  - M3, VIA3 and M4 (cell programming and routing)
  - Upper layers (VIA4 to M7) are optional for routing





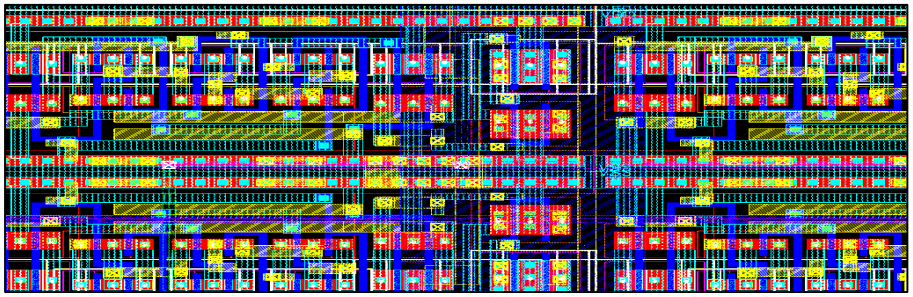
Cell programming and routing for 1P7M process

Programming layers for 1P7M Process

Source: http://www.faraday-tech.com/html/products/structuredASIC.html

LIBRARY FEATURE

- 3-input Look Up Table (LUT) cells
- Scan flip-flop with async. set and reset
- Filler cells and Antenna diode for design rule fix
- Metal 3 to metal 4 for cell programming and routing
- Clock-gating latch, latch, tri-state buffer and inverter support
- Cell density 20 KLUT/sq. mm @0.13um
- Cell delay 0.4ns



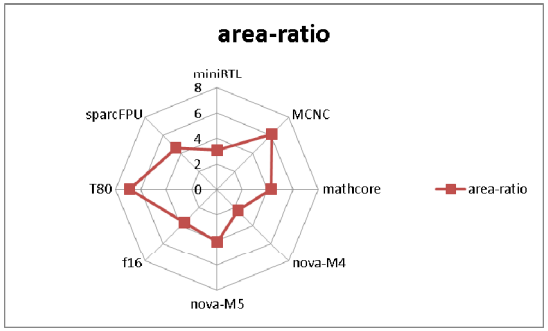
BENCHMARK CIRCUIT

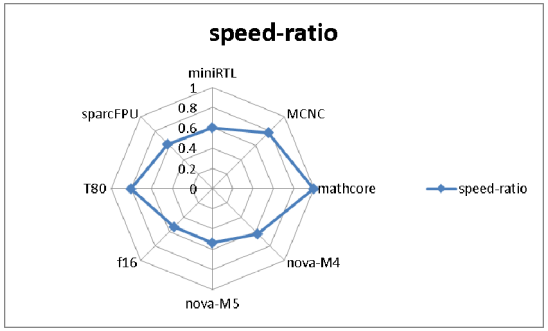
Applications

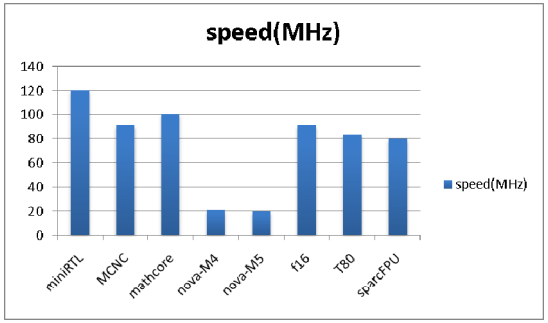
- miniRTL - A part of a LED backlit controller circuit
- MCNC - The largest from the MCNC benchmark suite
- Mathcore - A custom wrote math circuit consisting several DesignWare cores (32-bit fixed and floating point adder, multiplier)
- NOVA (M4/M5) - A low power H.264 decoder, using M4/M5 as top metal (2 or 3 routing layer)
- F16 - A small size 16-bit processor core
- T80 - A 8-bit microcontroller with tri-state bus and clock-gating logics from Opencores
- sparcFPU - The floating-point unit from the OpenSparc core (64-bit)

Summary

- Good for applications up to 120MHz
- Achieve 0.7x speed, with 4x area gain typically, comparing to ASIC 0.13um std-cell library.
- 46%-60% of TAT time saved

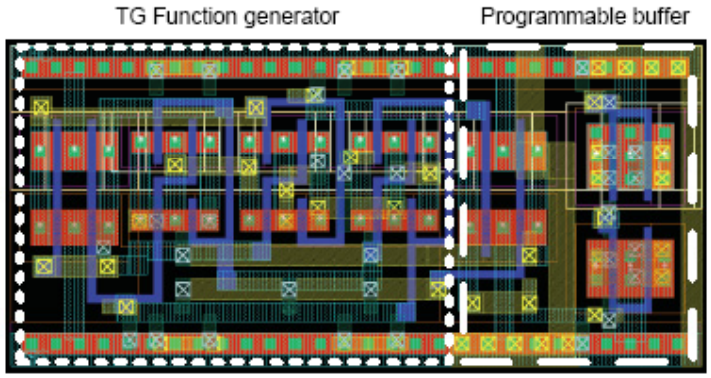




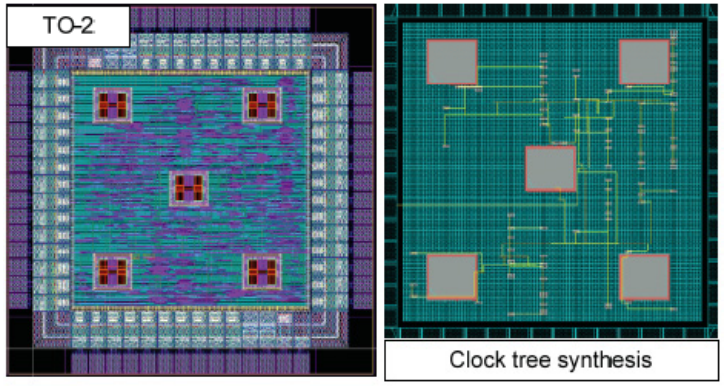


TO2:hermes

- Purpose: evaluate the mapping methodology and scan(test) capability
- Chip description
  - Process:
    UMC 0.13um MS/LOGIC 1P8M2T
  - Application:
    Active dynamic LED backlight controller (computationally intensive part)
  - Target Speed:
    100Mhz
  - Equivalent gate count:
    3.6K
  - Area :
    0.157 sq. mm
  - Chip utilization:
    82%



Screen capture of configurable cell in transmission gate technology

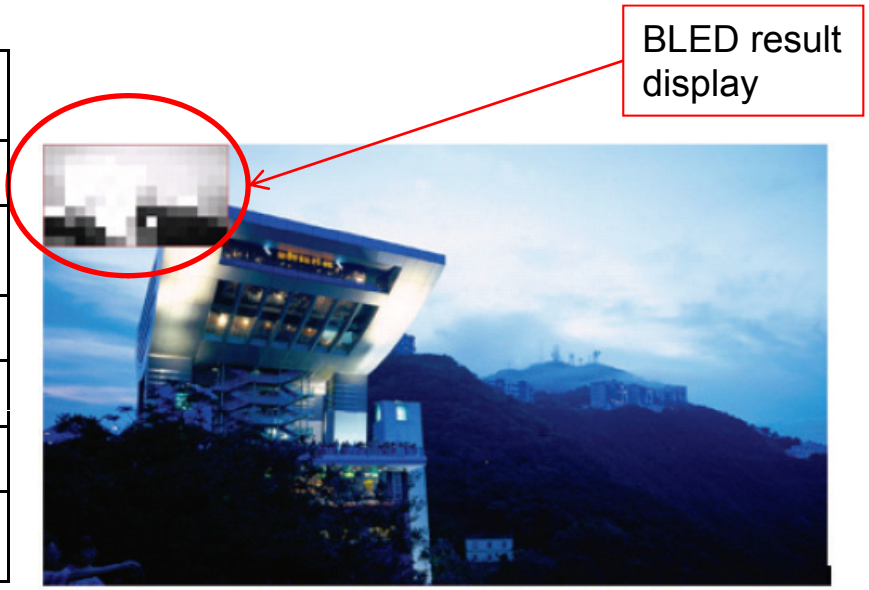


Screen capture of Layout TO2:hermes

ASTRI BLED APPLICATION

- Active Dynamic LED Backlight (BLED), for SoC implementation

	SASIC fabric	ASIC
Area (sq. mm)	0.157	0.045
Max. operating frequency (MHz)	100	118
Density (per sq. mm)	20 KLUT	250 Kgate
Chip density (utilization)	82%	80.5%
Routing layers	2 (M3-M4)	3 (M2-M4)
Number of mask for change of design	3	All



Simulated output

SUMMARY

- Lower NRE costs (about 1/6 of first design)
- Lower design risk because of proven silicon and regular fabrication structure
- Fast turn-around-time (about 1/3 of ASIC fabrication time)
- Comparable performance (speed and power consumption) as standard cells
- Verified on and estimated for 0.13um CMOS process
- Adopts the commercial timing-driven (Cadence Encounter) PnR flow with custom plug-ins.
- NO custom logic synthesizer, placer, or router required
- Source code is open to the user

SEM photos of TO-1:meh for cell characterization