A High Performance Low Complexity Joint Transceiver for Closed-Loop MIMO Applications

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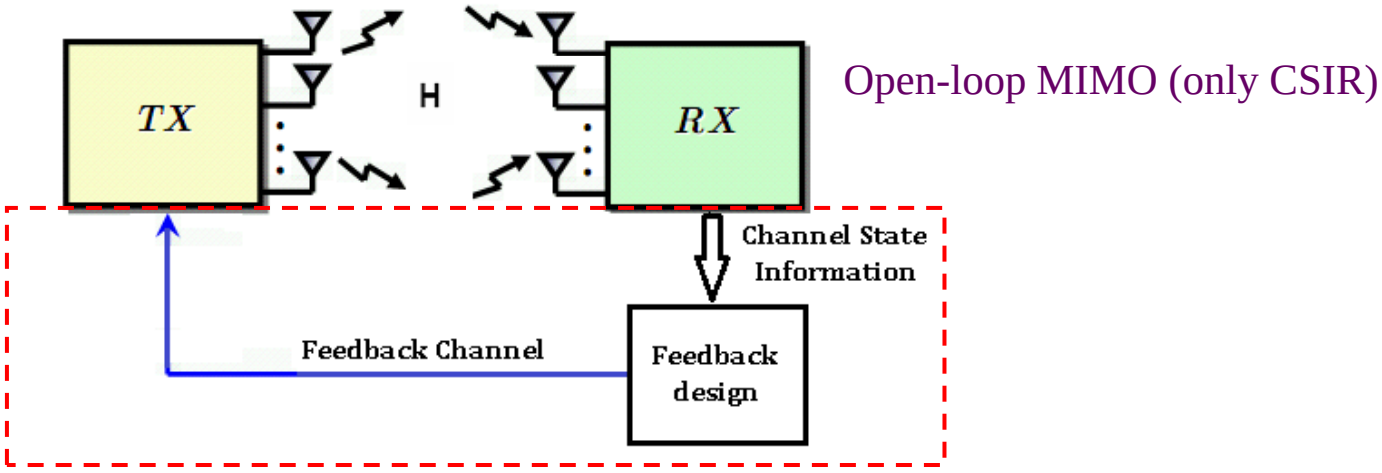
Motivation

- Joint Transceiver Design for Closed-Loop MIMO
  - TX can take advantage of CSI to apply the advanced processing to enhance the performance of communications.
  - Target
    - High performance
    - Low complexity
    - Low feedback overhead

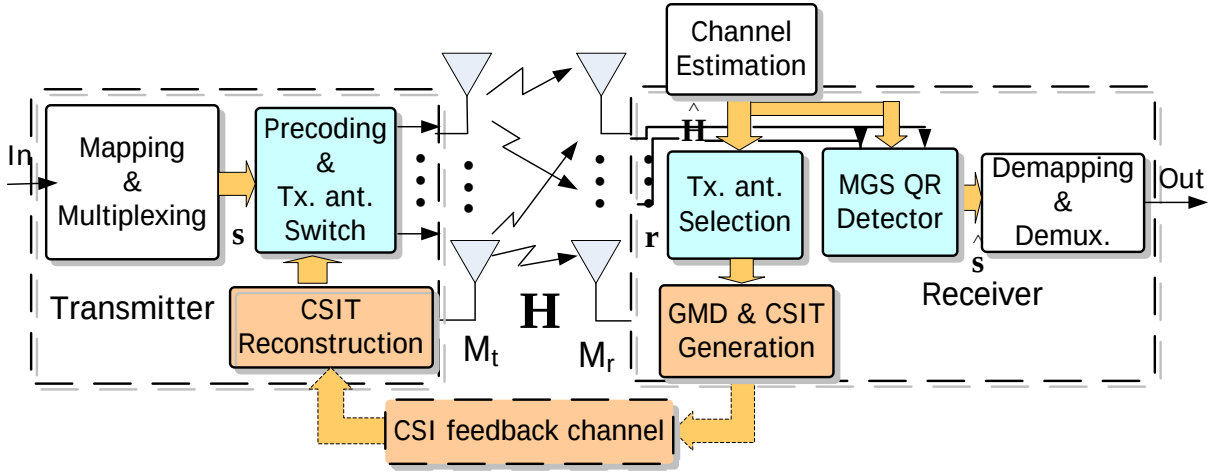


Open-loop MIMO (only CSIR)

Closed-loop MIMO (both CSIT & CSIR)

System Description

- An efficient and practicable MIMO transceiver in which transmitter antenna selection is applied to QR detector and GMD precoding through limited feedback channel is proposed.



- $\mathbf{y} = \mathbf{HVs} + \mathbf{n}$

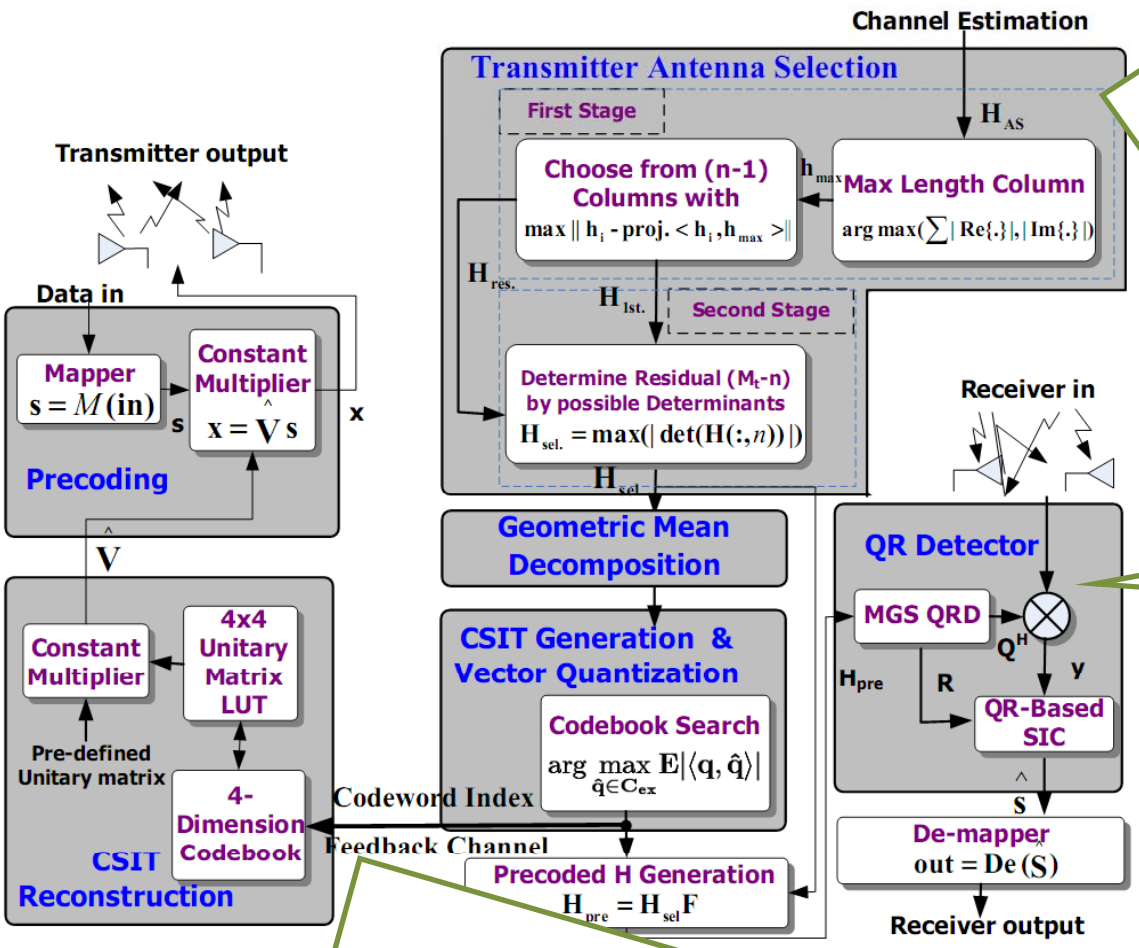
$= \mathbf{QRs} + \mathbf{n}$

$(\mathbf{H} = \mathbf{QRP}^*)$

$(\mathbf{PrecoderV} = \mathbf{P})$

Channel Model	i.i.d. Rayleigh flat fading
Antenna selection	4 Tx ant. from 6 Tx ant.
Spatial multiplexing	4x4
Modulation	QPSK, 16QAM, 64QAM

Architecture of the Proposed Transceiver



Compare with the exhausting det. search method, the complexity is 50% reduction and the performance is consistent.

The simple and robust QR detection.

Favorable amount of feedback bit. Low complexity and efficient precoder quantization and reconstruction.

Implementation Results

FPGA Demonstration

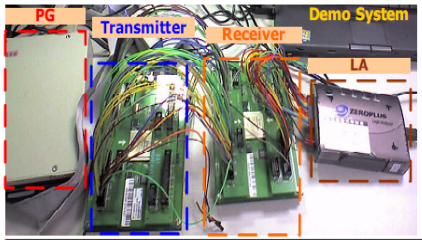
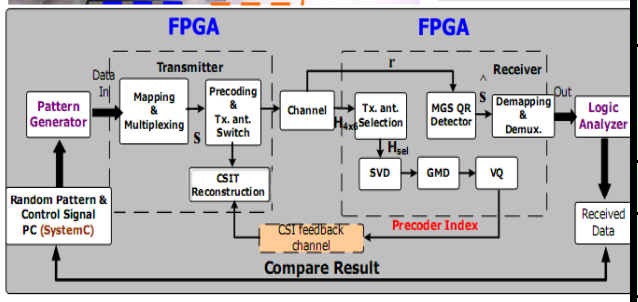


Table III
Device utilization for XC4VLX160

Resources	Transmitter	Receive
DFF	939	6585
LUT	1672	30648
Block RAMs	22	37
DSP48s	16	80



Specification

Application	- WLAN - DSL Systems
Channel Condition	Rayleigh i.i.d. fading MIMO channel & Quasi-stationary
Tx. Antenna Selection	4 Tx ant. from 6 Tx ant.
Support Modulation Type	QPSK (BPSK) 16-QAM 64-QAM
Clock Rate	45 MHz
Code book Size	Unit 4-vector with 64 entries
Maximum clock freq.	50 MHz (FPGA)
Maximum throughput	120 Mbps (FPGA)

Comparison

FEEDBACK OVERHEAD COMPUTATION.

	2 × 2	3 × 3	4 × 4	5 × 5
Scalar quant. [a][4]	20 bits	45 bits	80 bits	125 bits
Parameter method [b][4]	10 bits	30 bits	60 bits	100 bits
SVQ [c][5]	5 bits	11 bits	18 bits	26 bits
Modified SVQ [d]	5 bits	6 bits	7 bits	8 bits

		Exhausted Det.	Modified GSO-based
4 x 5	Real Multiplication	800	712
	Real Addition	710	735
4 x 6	Real Multiplication	2400	1250
	Real Addition	2130	1236
4 x 7	Real Multiplication	5600	1948
	Real Addition	4970	1879

Features

- Better performance than the MLD and 6dB SNR improvement over the V-BLAST at BER=10^{-2}.
- Reduce more than 50% hardware complexity in antenna selection compared to exhausting determinant search method.
- Efficient precoder quantization and reconstruction.
- Favorable amount of feedback bit.
- Full implementation and practical FPGA platform emulation.