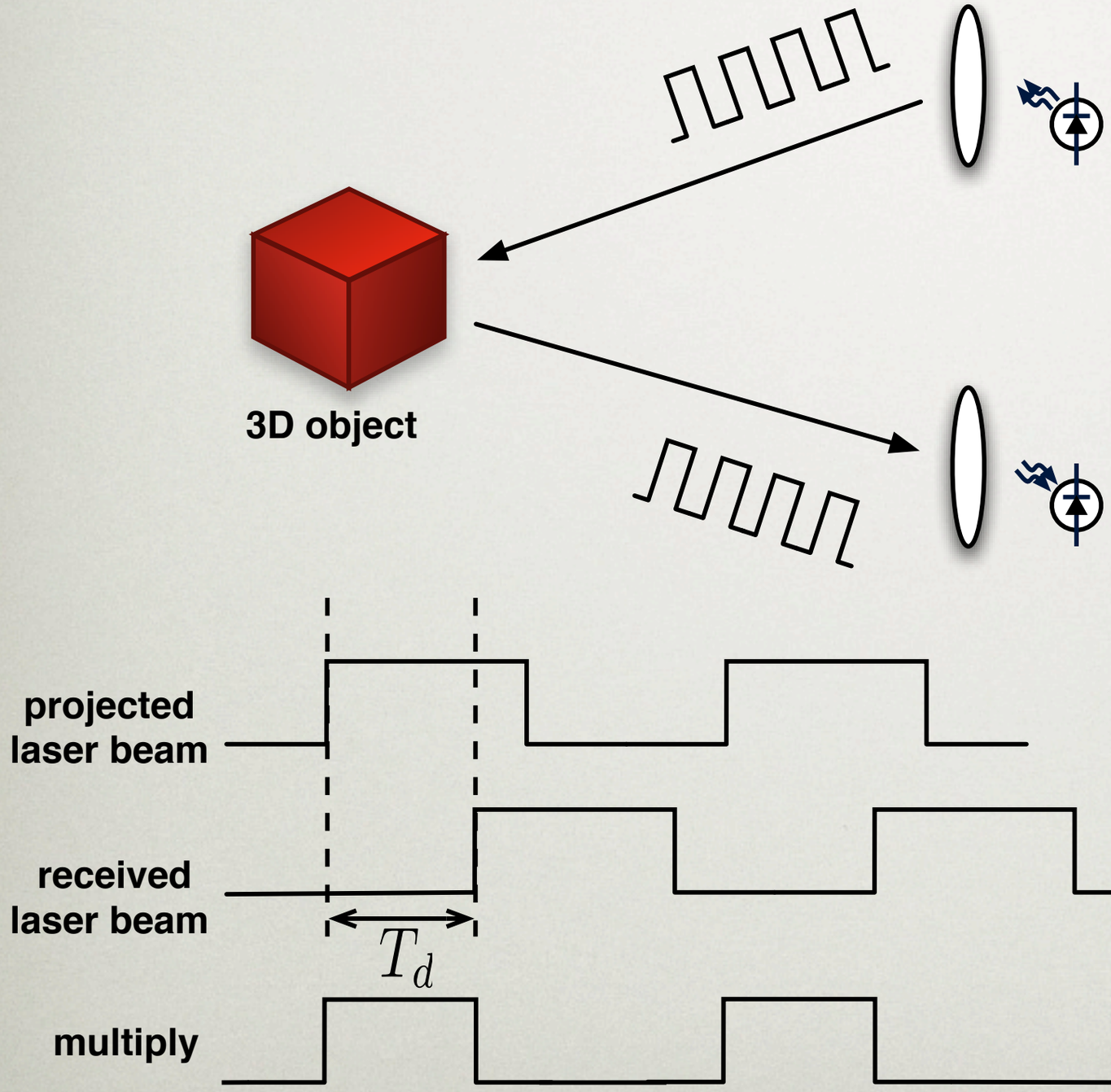
ASPDAC 2010(UDC)
in *Taipei*

Cascaded Time Difference Amplifier using Differential Logic Delay Cell

S. Mandai[1], T. Nakura[2], M. Ikeda[1,2], and K. Asada[1,2]

[1] Dept. of Electrical Engineering and Information Systems
[2] VLSI Design and Education Center(VDEC)
The University of Tokyo

Time-of-Flight (Pulse based method)



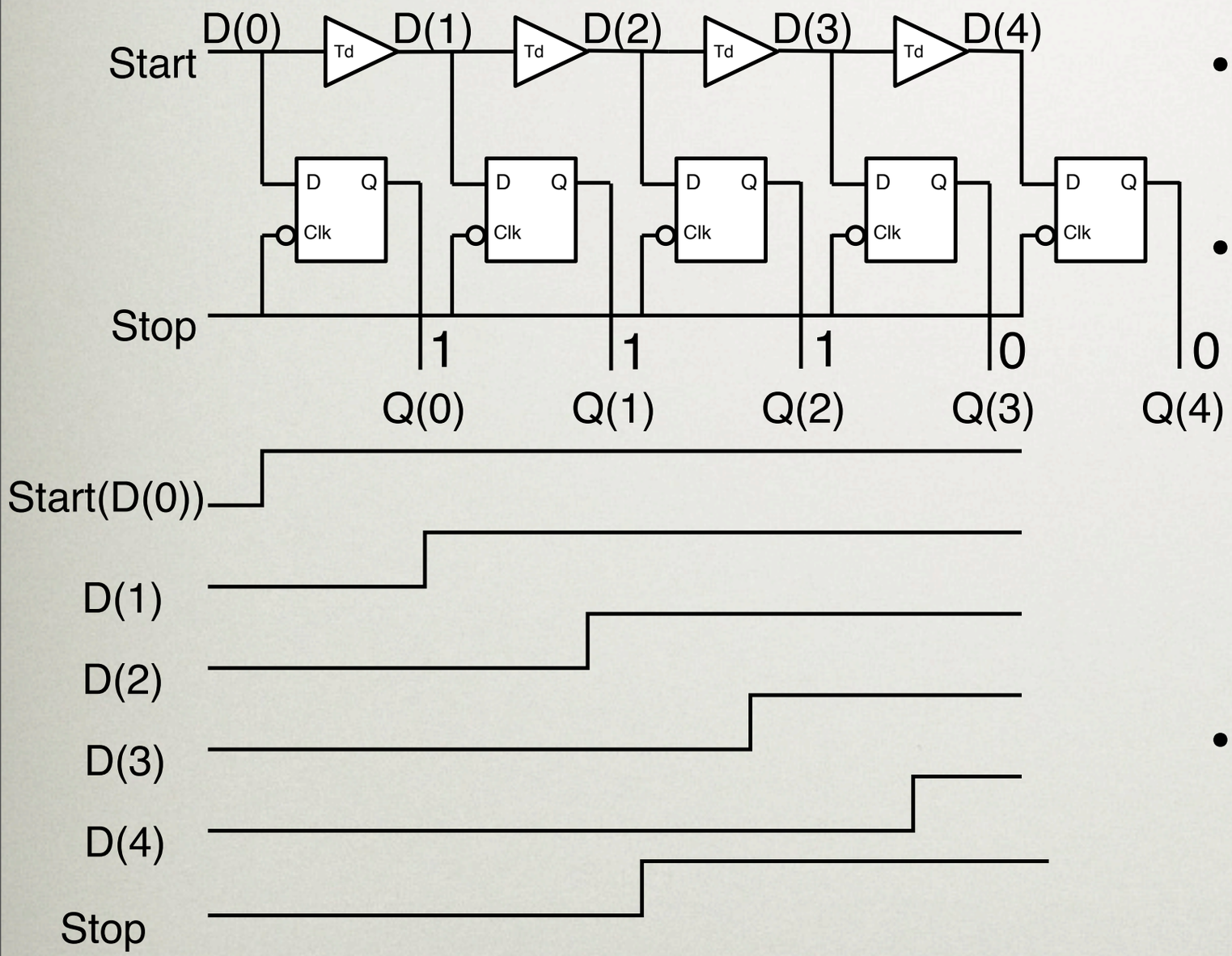
- Light source is simple
- Range calculation is easy
- Range accuracy depends on the detection of Td

- Use analog multiplier
- Use Time-to-Digital Converter

Resolution -> Range accuracy

- 100ps -> 15mm
- 10ps -> 1.5mm
- 1ps -> 0.15mm

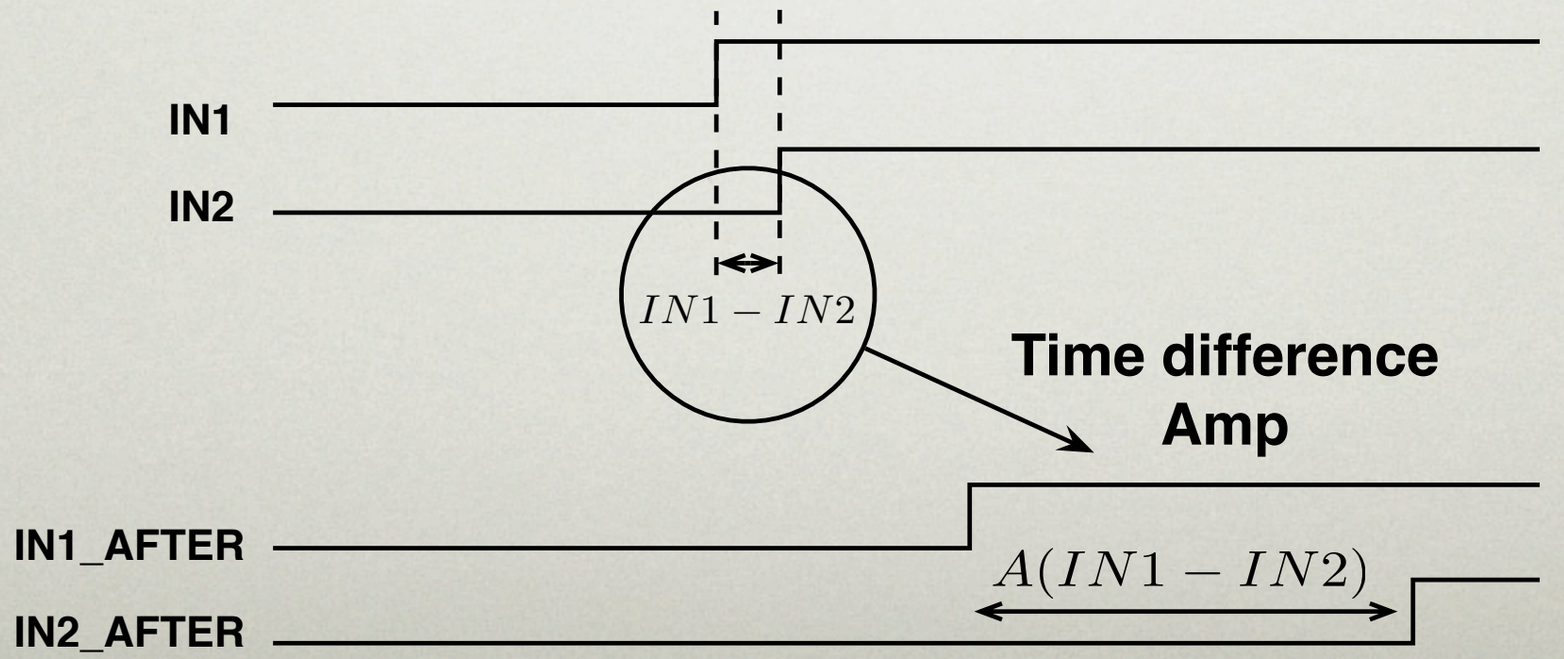
Time-to-Digital Converter



- **A chain of buffers and flip-flops are often used**
- **As scaling of Tr., time resolution is higher**
  - **180nm : about 30ps**
  - **90nm : about 15ps**
  - **65nm : about 10ps**
- **Minimum time resolution is limited by a buffer delay(gate delay)**

Time Difference Amplifier to Realize Fine Resolution TDC

- **There are many methods to realize sub-gate delay**
  - **The Vernier TDC(Large area)**
  - **Passive interpolation(Low resolution)**
- **The TDC using time difference amplifier(TDA can realizes high resolution with small area**



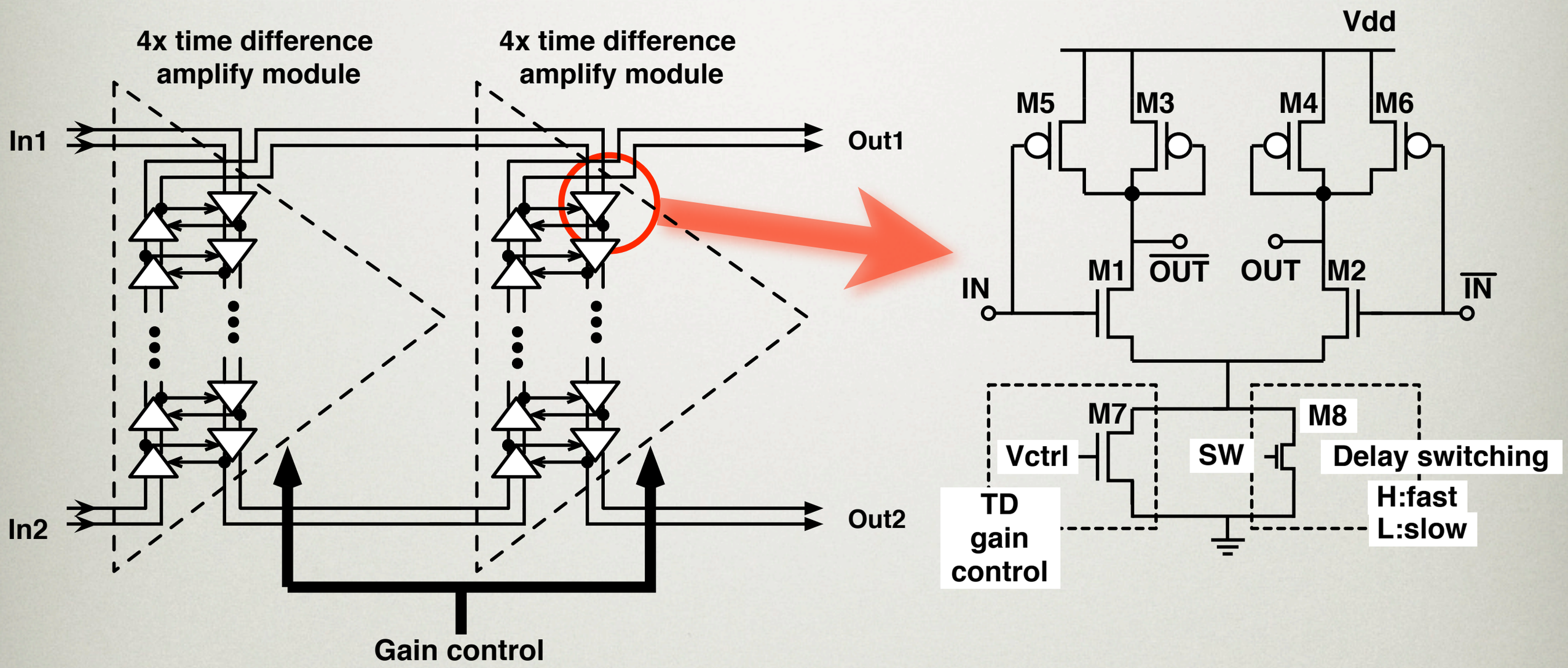
Conventional TDA

✓ Advantage

✓ Drawback

- **Open loop structure (M. Lee, VL2007)**
  - ✓ High gain
  - ✓ Simple structure
  - ✓ Sensitive to PVT variation => Fatal Drawback
- **Closed loop structure(T. Nakura, VL2009)**
  - ✓ Strong to PVT variation
  - ✓ Low gain => Can be solved!!
  - ✓ weak in circuit noise =>

Proposed Cascaded Time Difference Amplifier using Differential Logic Delay Cell



- ***High TD gain***
- ***Strong to periodic noise, cross talk and realize high resolution***

Measurement Result of In-Out TD