A Dual-MST Approach For Clock Network Synthesis

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Presentation Overview

- Introduction
- Background
- Methodology
- Experimental result
- Conclusion

Introduction

- Distribution of clock network
- PVT (process, voltage, temperature) variation-tolerant
- Previous works
  - Equidistant clock routing [M. A. B. Jackson et al. DAC'1990]
  - Exact zero skew [R.-S. Tsay, ICCAD'1991]
  - Cross links insertion [A. Rajaram et al. DAC'2004]

Background

- ISPD2009 Clock Network Synthesis Contest [Sze et al., ISPD′2009]
- Slew rate constraint
  - Less than 100ps along the whole network
- Power consumption constraint
  - Use total capacitance as a representation
- Blockage for buffer insertion
- Clock Skew and Latency Range
  - The range of skew values under two voltage settings (1.0 V and 1.1 V)

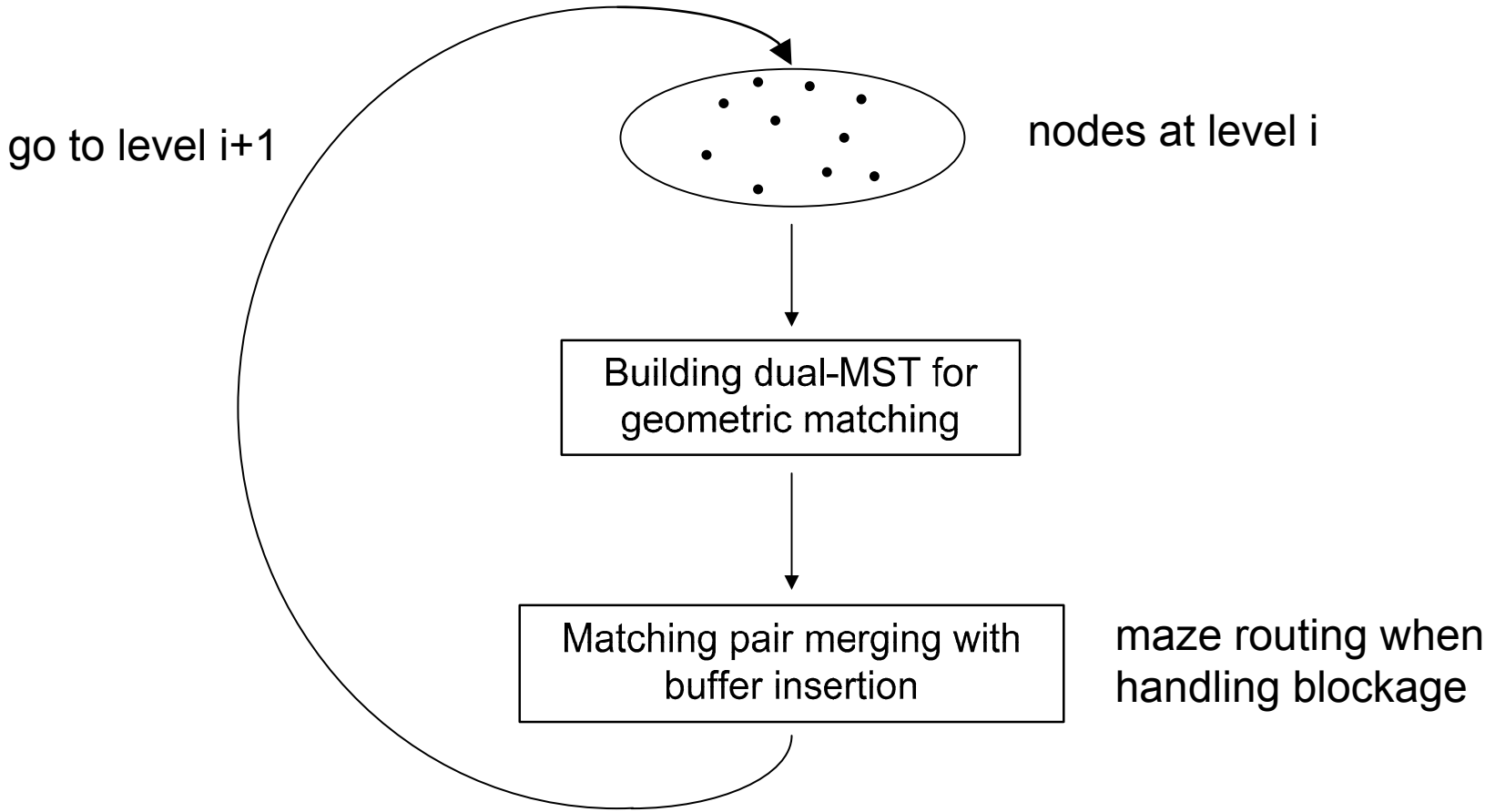
Synthesizer Overview

- A bottom-up approach of clock tree construction
- DME [Chao et al., DAC'1992] is applied
- Look-up table is pre-built for slew rate reference
- Two approaches of CTS are developed
  - DMST
    - Elmore RC model
    - Zero skew synthesizer
  - DMSTSS
    - An advancement of DMST
    - SPICE simulation for delay estimation

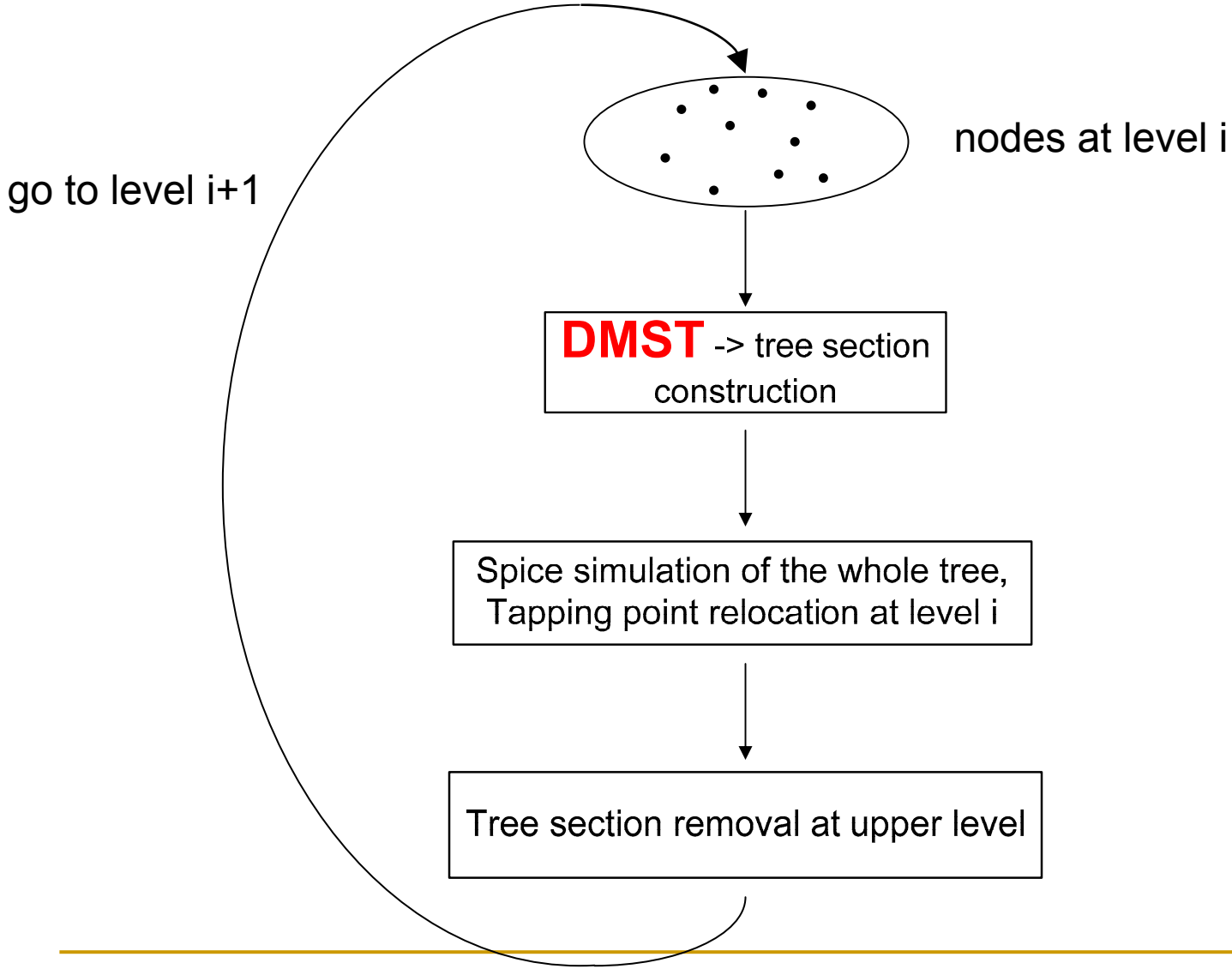
Methodology Overview

- Level-divided tapping point relocation
- Iterative removing and rebuilding of upper tree sections
- A dual-MST topology construction
- Dynamic buffer sizing
- Recursive nodes merging and buffer insertion
- Improved maze router for blockage handling

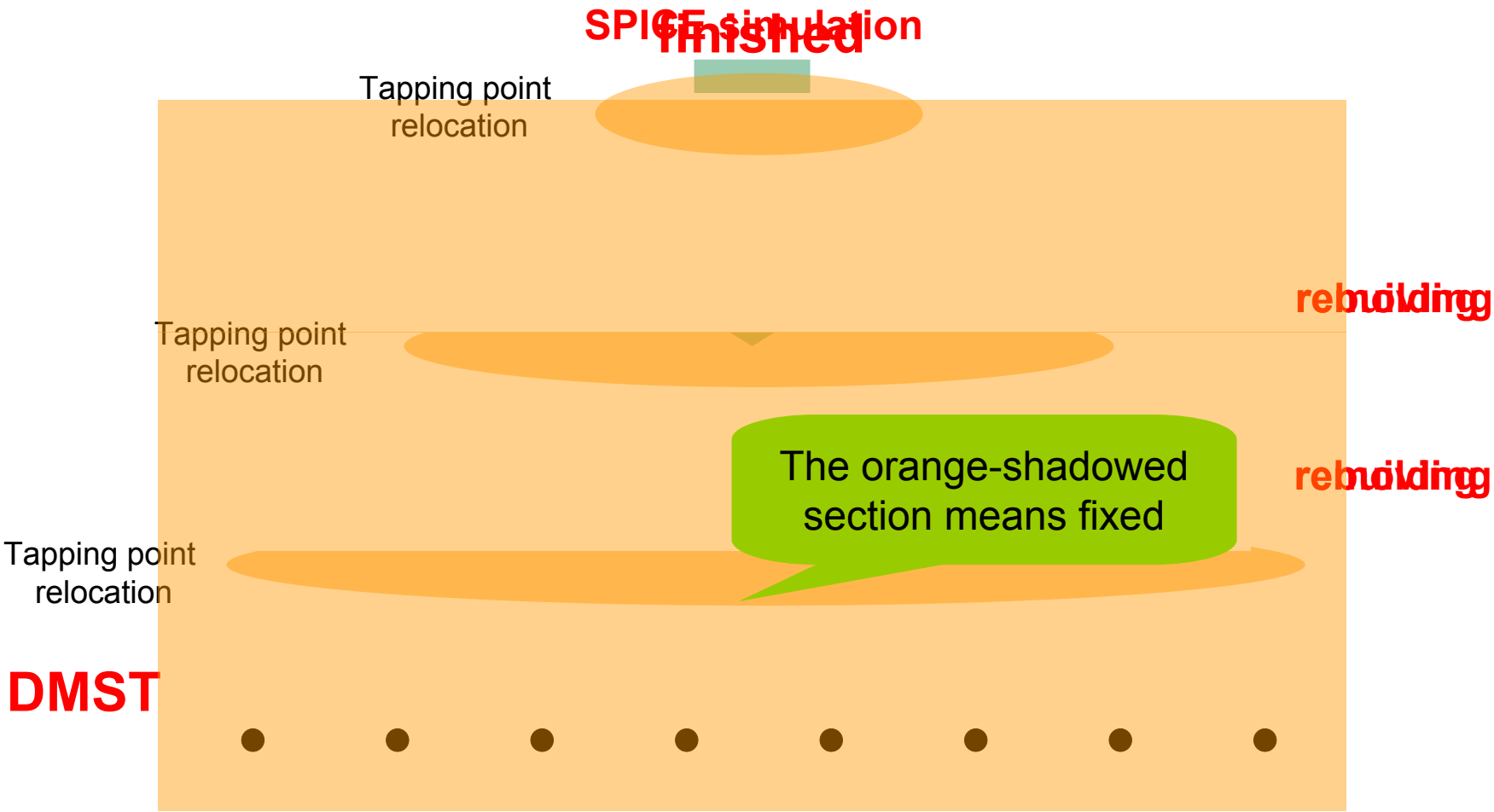
DMST Overview



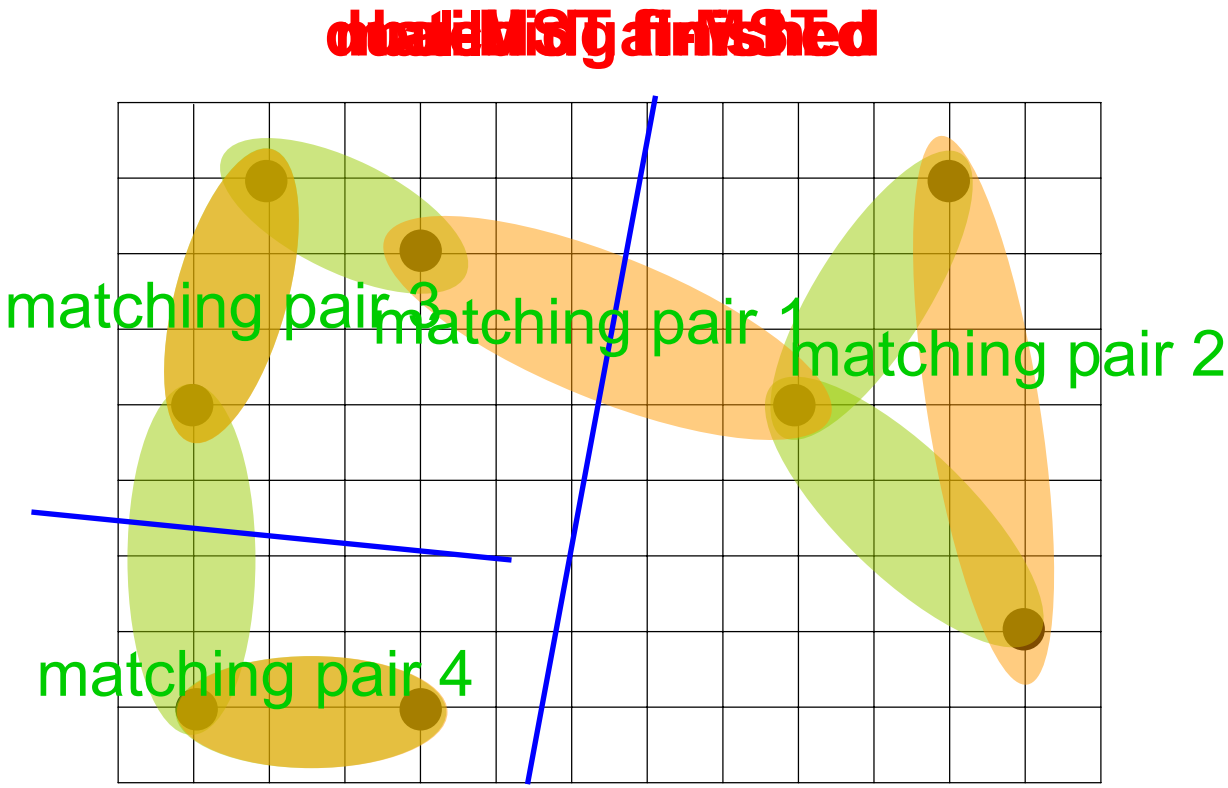
DMSTSS Overview



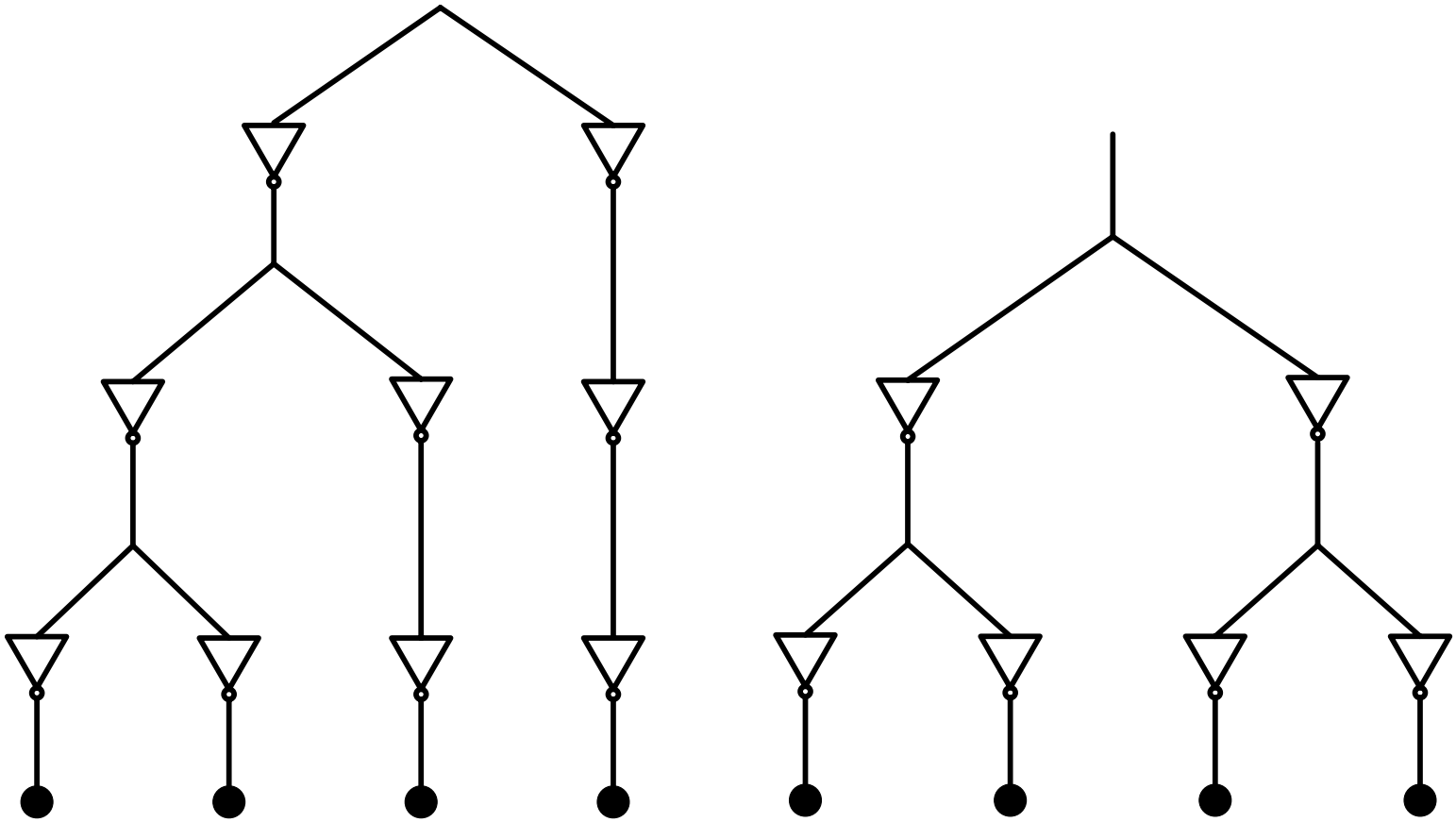
Clock Tree Construction



Dual-MST


matching pair 3
matching pair 1
matching pair 2
matching pair 4

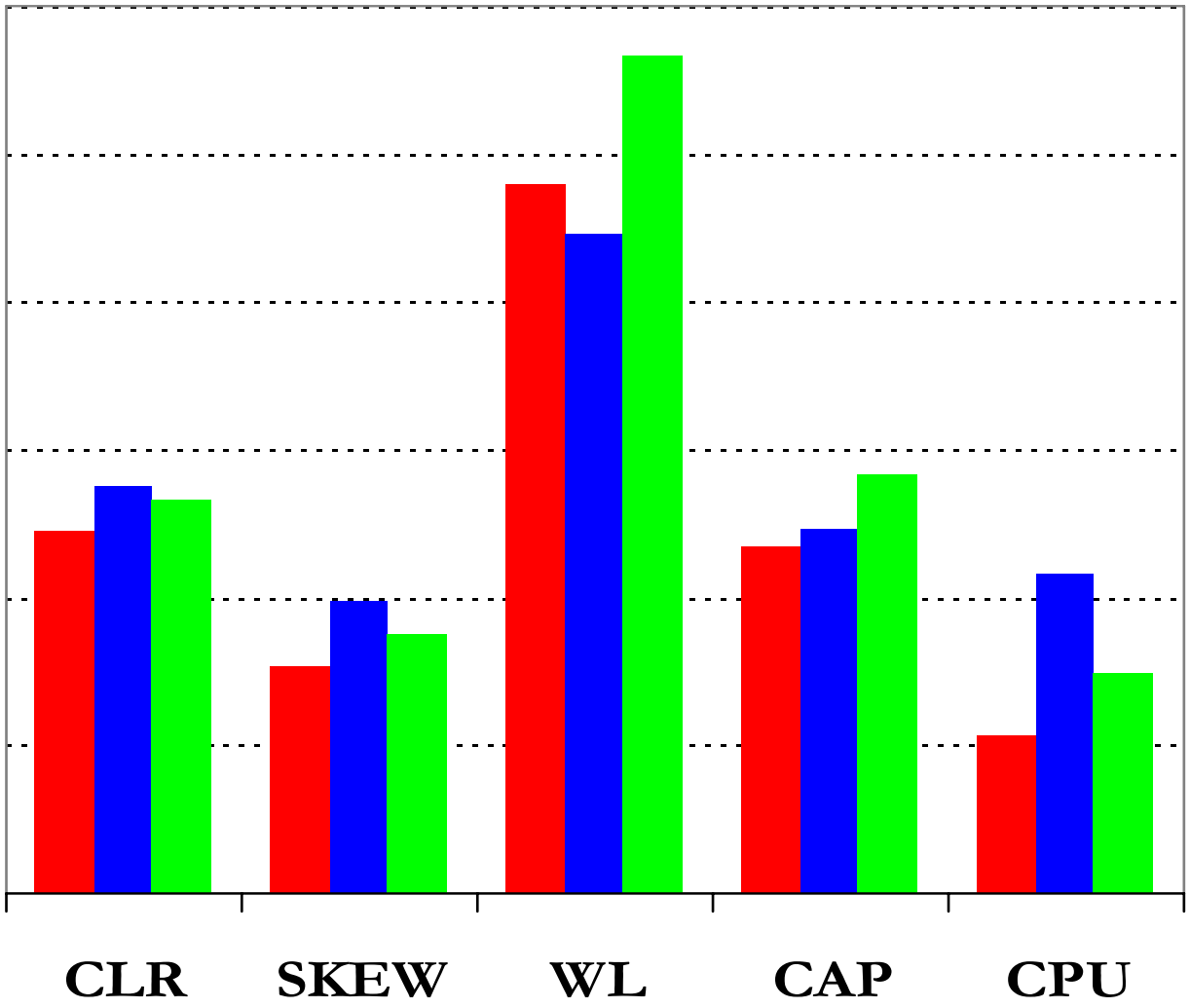
Topology Comparison



CLUSTERING

dual-MST

Performance Comparison

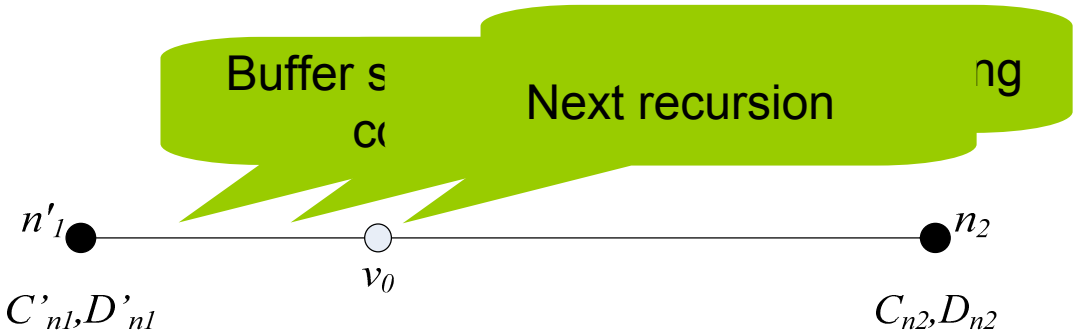


It is a modified version of original MMM with a bottom-up procedure

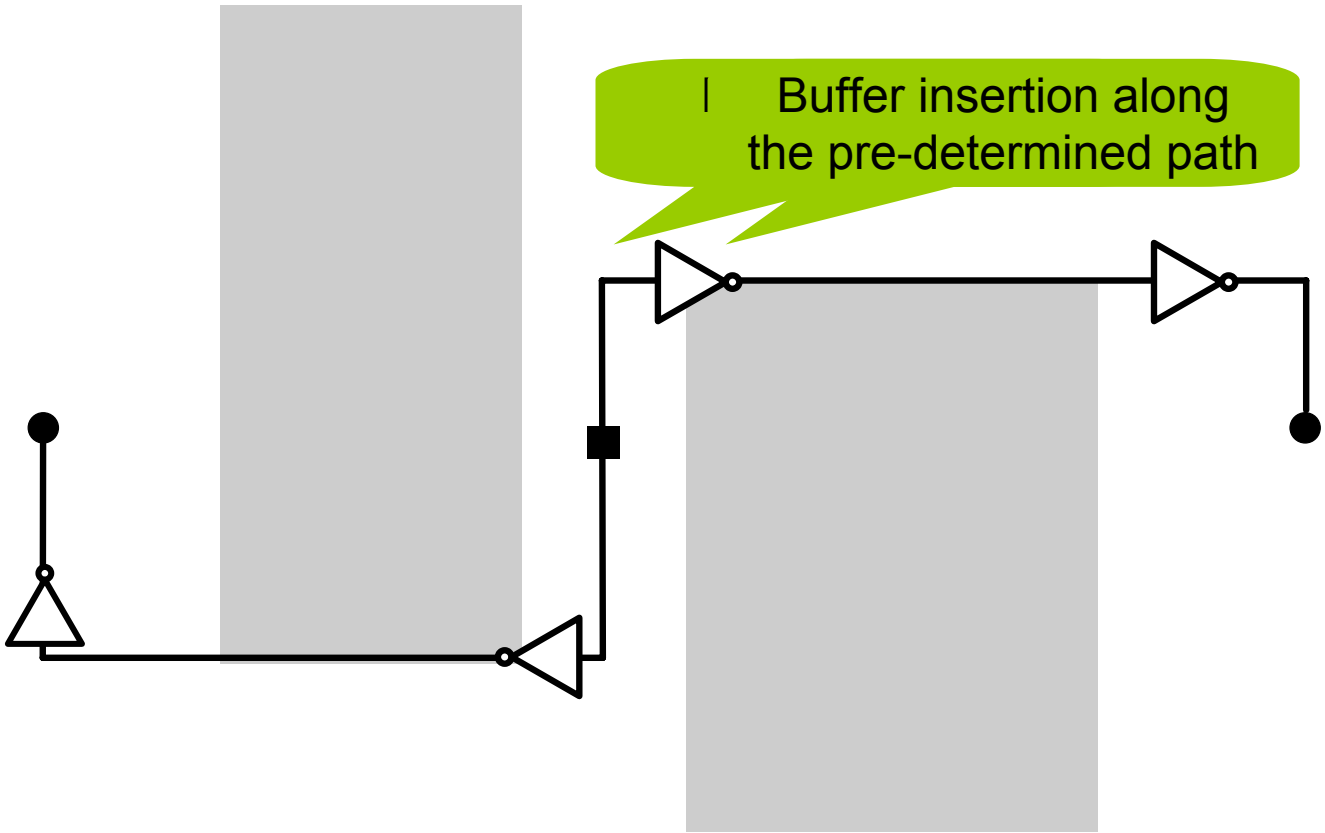
Buffer Sizing

Bigger buffer size on common paths

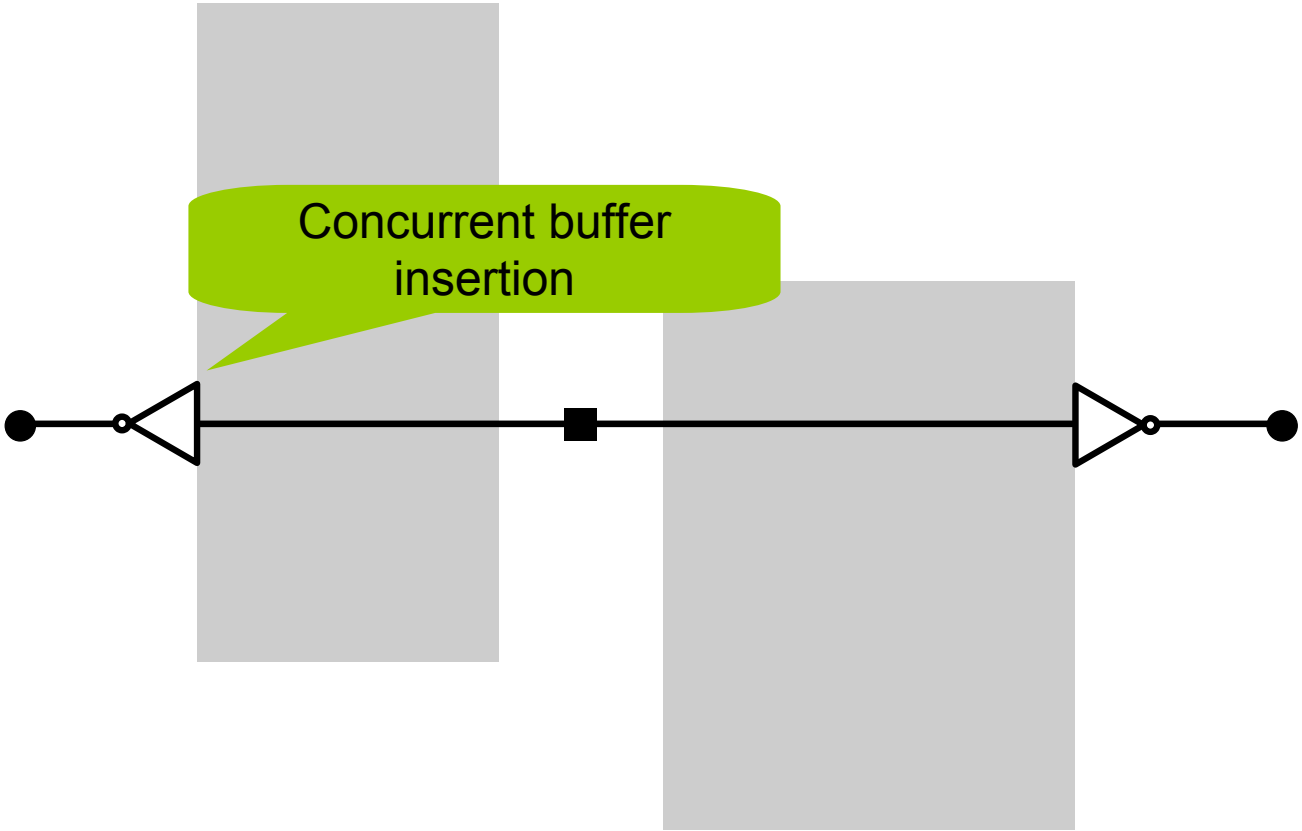
Buffer Insertion



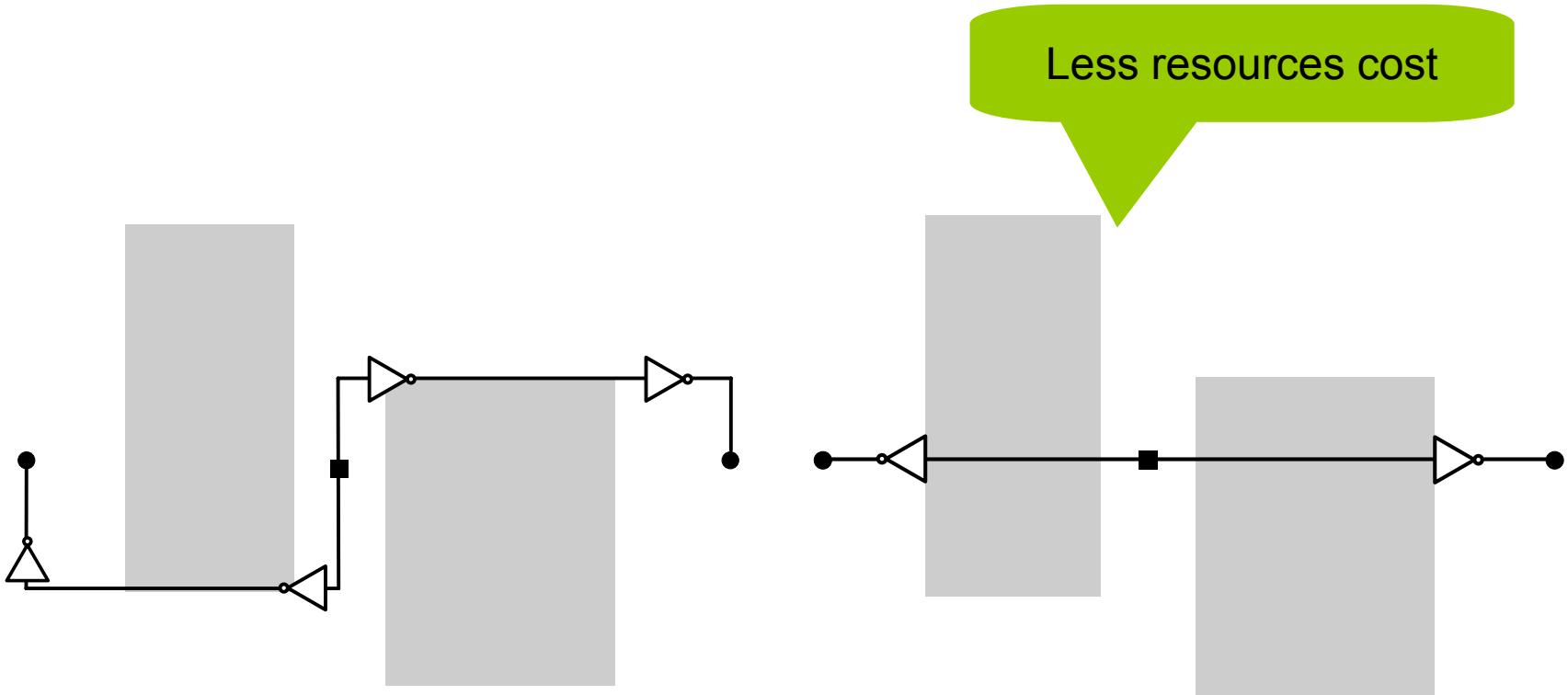
Blockage



Blockage



Comparison



full detour

our approach

ISPD2009 Circuits Table

CUICIRTS	SINK #	BLOCKAGE (%)	CAPACITANCE (fF)
11	121	0%	118000
12	117	0%	110000
21	117	0%	125000
22	91	0%	80000
31	273	24.38%	250000
32	190	34.26%	190000
33	209	27.68%	195000
34	157	38.67%	160000
35	193	33.22%	185000
nb1	330	37.69%	42000
nb2	440	63.88%	88000
AVG	203.5	23.62%	140273

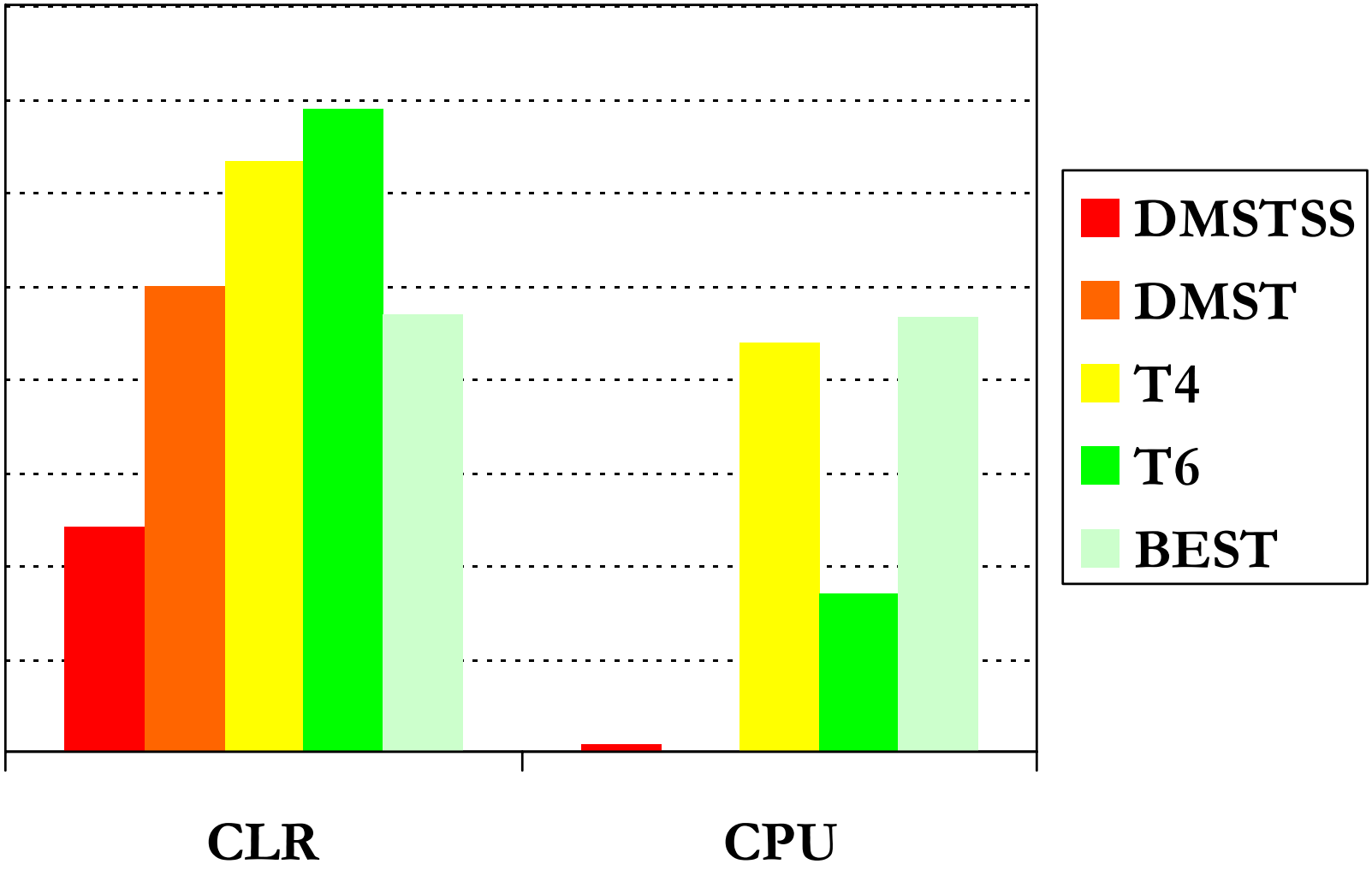
CLR & SKEW

CIRCUIT	DMSTSS		DMST		T4		T6		BEST	
	CLR	SKEW	CLR	SKEW	CLR	SKEW	CLR	SKEW	CLR	SKEW
11	**12.2**	6.5	20.5	15.6	26.7	4.7	32.3	5.2	22.3	6.4
12	**10.9**	7.0	22.2	18.6	25.7	4.8	32.2	5.9	22.2	5.4
21	**12.1**	6.7	22.0	17.3	30.5	5.3	34.3	6.1	19.6	3.2
22	**9.9**	4.3	17.1	11.9	24.5	3.4	30.4	7.1	16.4	3.0
31	**13.4**	10.1	39.1	36.7	45.1	7.6	51.3	10.9	45.1	7.6
32	**11.5**	8.8	27.7	24.3	36.9	5.3	40.3	6.4	18.4	7.7
nb1	**13.8**	7.9	26.1	17.1	NA	NA	19.8	7.2	19.8	7.2
AVG	**12.0**	7.3	25.0	20.2	31.6	5.2	34.4	7.0	23.4	5.8
33	13.4	6.2	22	23.1	NA	NA	NA	NA	NA	NA
34	11.3	11.1	26.2	18.8	NA	NA	NA	NA	NA	NA
35	13.1	7.8	20.2	21.2	NA	NA	NA	NA	NA	NA
nb2	13.1	8.7	35.4	30.1	NA	NA	NA	NA	NA	NA

CAPACITANCE & CPU

CIRCUIT	DMSTSS		DMST		T4		T6		BEST	
	CAP	CPU	CAP	CPU	CAP	CPU	CAP	CPU	CAP	CPU
11	79.3	**180**	79.6	0.3	85.5	14764	73.9	3892	89.9	23358
12	89.3	**213**	90.3	0.3	84.7	13934	73.5	3944	87.9	14992
21	83.2	**210**	83.6	0.3	80.8	14978	74.3	4587	86.7	26420
22	79.4	**113**	79.4	0.3	81.8	7189	70.0	2005	85.0	9432
31	83.4	**777**	84.6	1.3	73.5	40088	81.5	17333	73.5	40088
32	82.4	**420**	82.6	0.4	80.1	3566	77.4	10599	89.9	2888
nb1	82.0	**82**	84.3	0.6	NA	NA	63.1	477	63.1	477
AVG	82.7	**285**	83.5	0.5	81.1	15753	73.4	6119	82.3	16807
33	83.6	483	83	0.4	NA	NA	NA	NA	NA	NA
34	85.7	354	85.7	0.4	NA	NA	NA	NA	NA	NA
35	85.0	453	84.9	1.9	NA	NA	NA	NA	NA	NA
nb2	87.9	202	89	1.6	NA	NA	NA	NA	NA	NA

Result Comparison



Conclusion

- We have proposed two approaches for clock tree synthesis, DMST and DMSTSS
- CLR (clock latency range) is greatly reduced
- CPU time is greatly reduced
- Neither slew rate violation nor blockage violation is met
- Link insertion can be applied for further improvement

Q&A

THANK YOU !