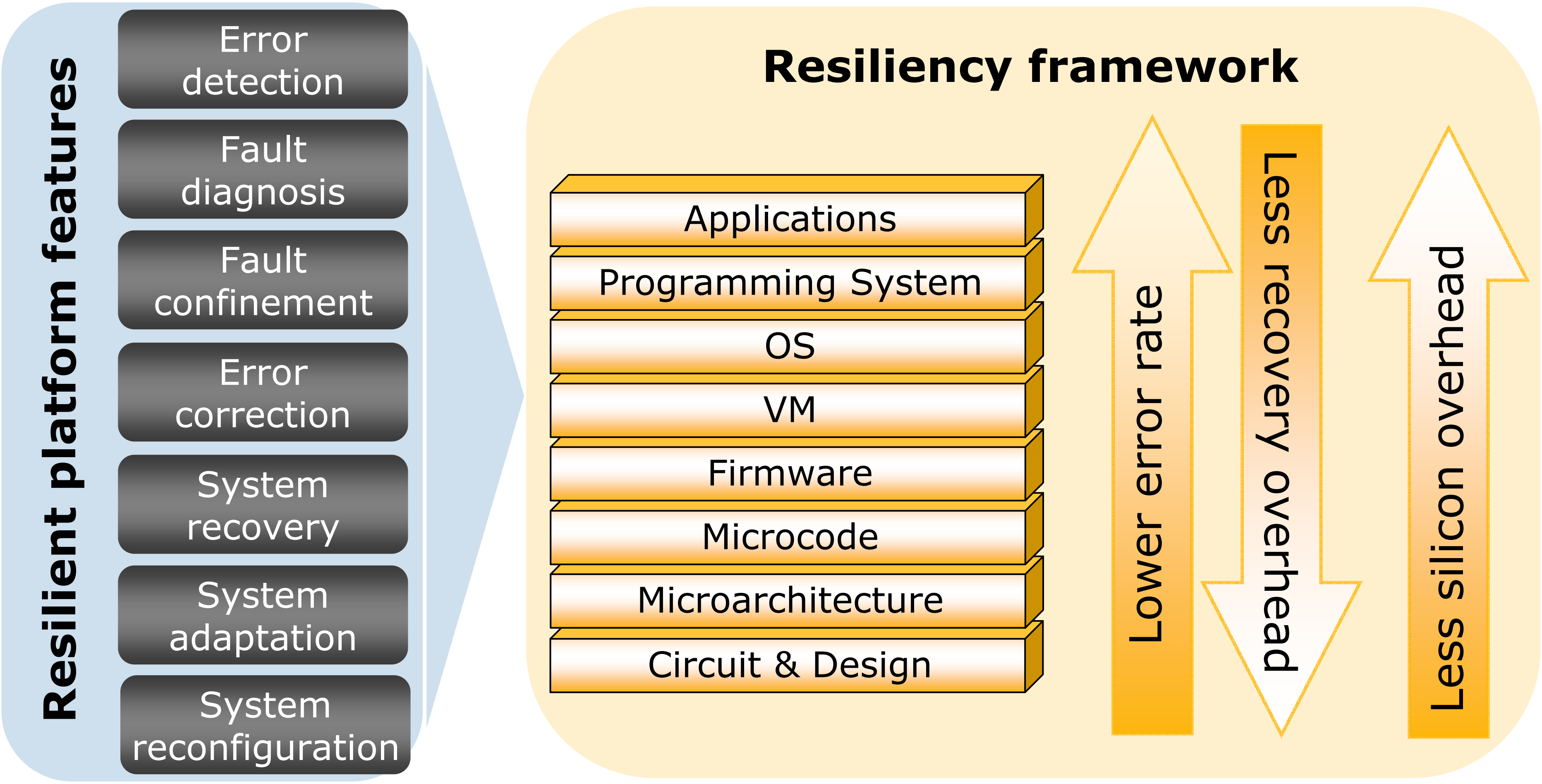
Resilient Design in Scaled CMOS for Energy Efficiency

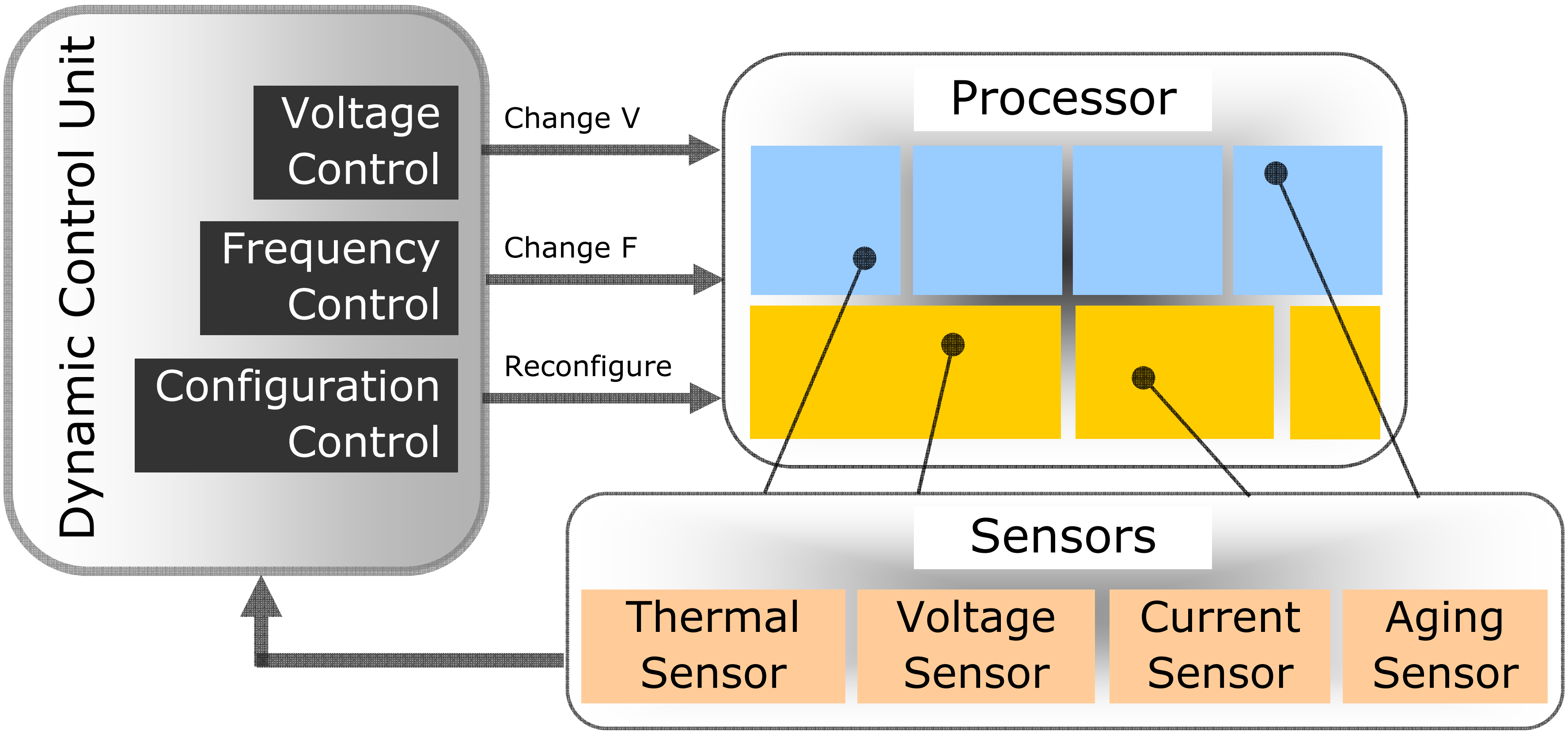
Vivek De
Intel Fellow
Director of Circuit Technology Research
Circuits Research Lab
Intel Labs

Resilient platforms



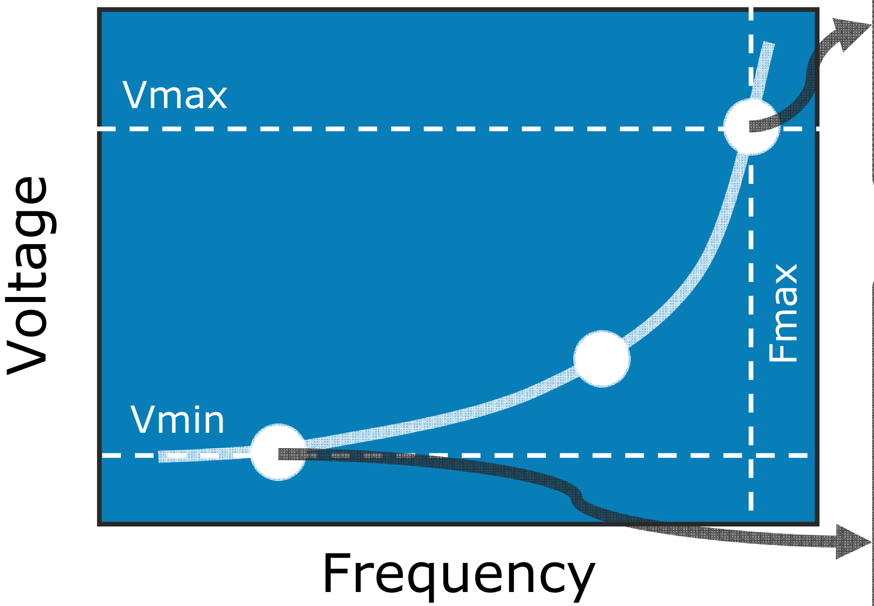
<u>Resiliency</u> for performance, efficiency & reliability

Dynamic adaptation & reconfiguration



Adapt & reconfigure for <u>best</u> power-performance

Voltage-frequency range limiters



Vmax/Fmax limiters

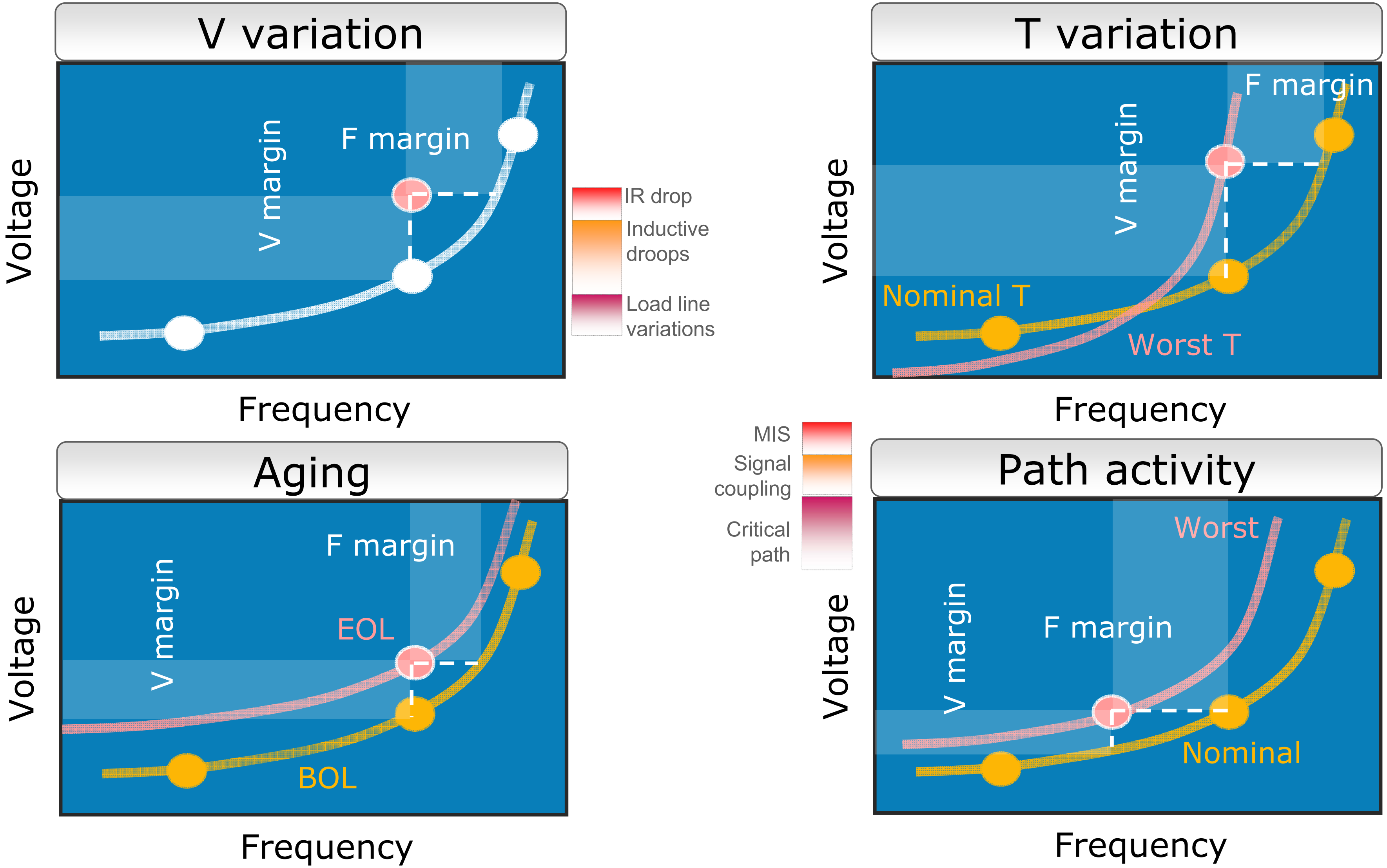
- Reliability
- Thermals
- Power delivery

Vmin limiters

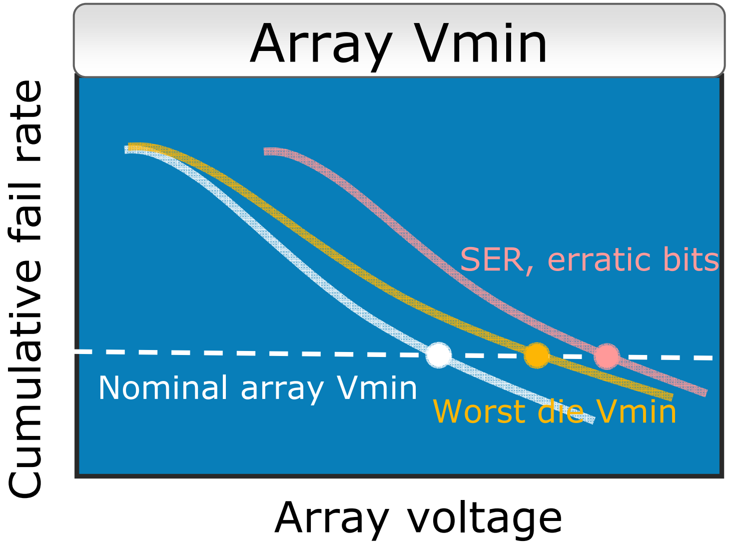
- Circuit functional failures
- Soft errors
- Steep frequency roll-off
- Aging

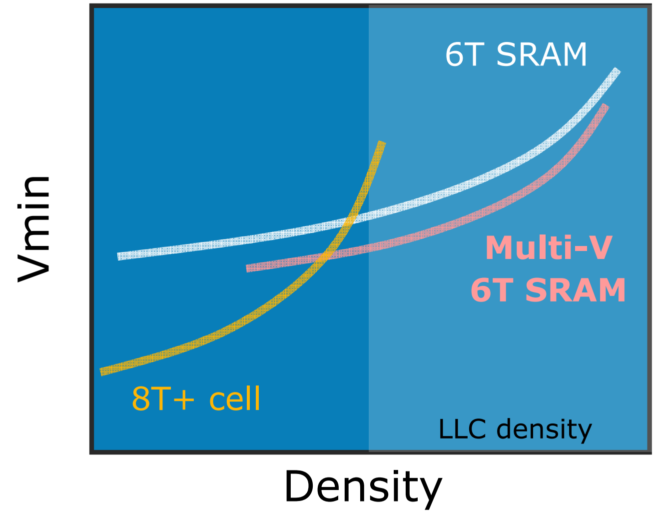
Reliability & functional failures limit range

Voltage-frequency margins

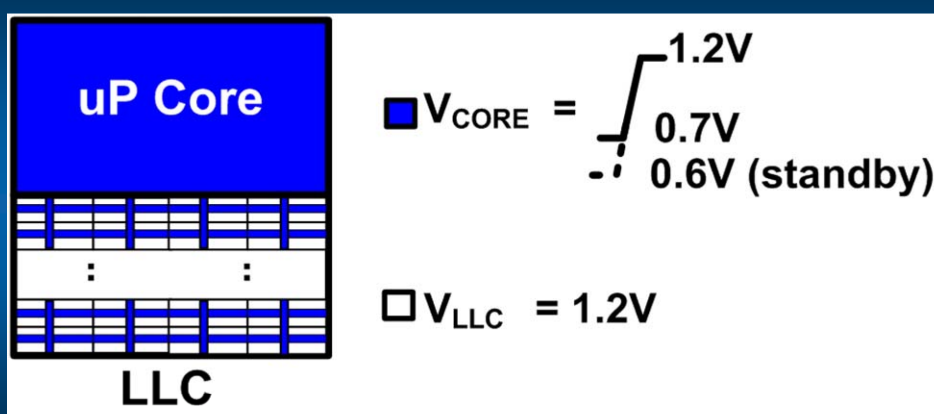


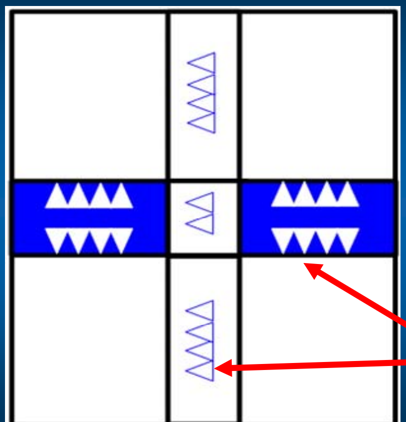
Multi-voltage cache





Push active Vmin limit to Vmax

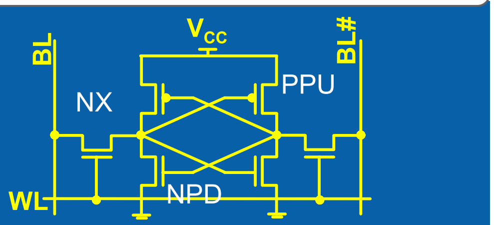




Embedded level shifters for wordline & write drivers minimize area & power overhead

Dynamic multi-voltage cache

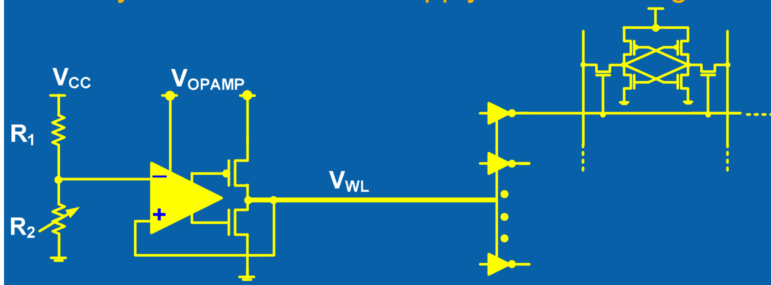
6T SRAM cell



	Read	Write	Retention
NX	Weak	Strong	-
NPD	Strong	Weak	Balanced
PPU	Strong	Weak	Balanced

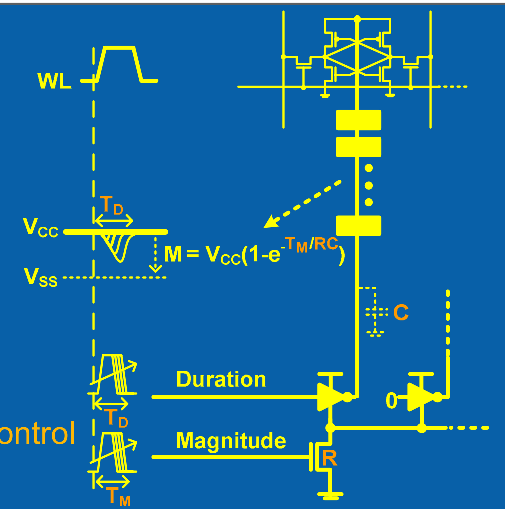
Wordline underdrive for read

Array to WL differential supply noise tracking



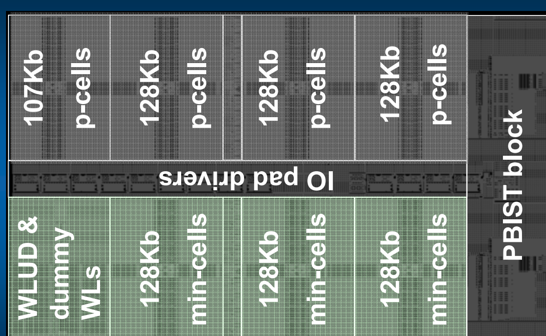
Dynamic voltage collapse for write

Pulse width control

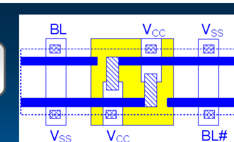


45nm dynamic multi-V testchip

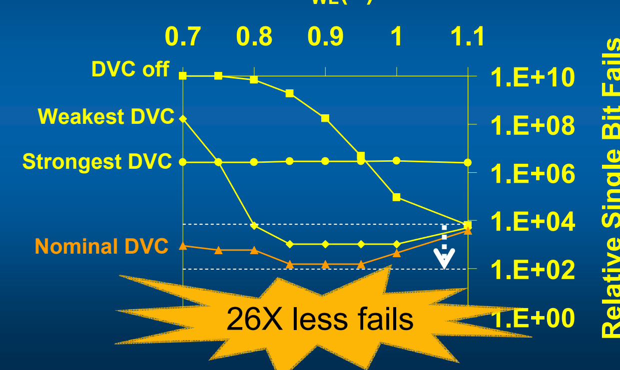
Transistor count	6.2M
Chip Area	$0.91mm^2$
Vcc	1.1V-0.7V
Testing interface	membrane probe card



MIN cell



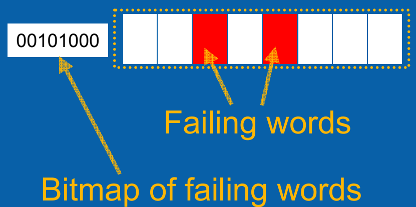
Source: Intel



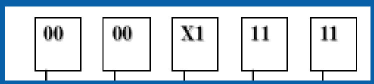
Cache reconfiguration

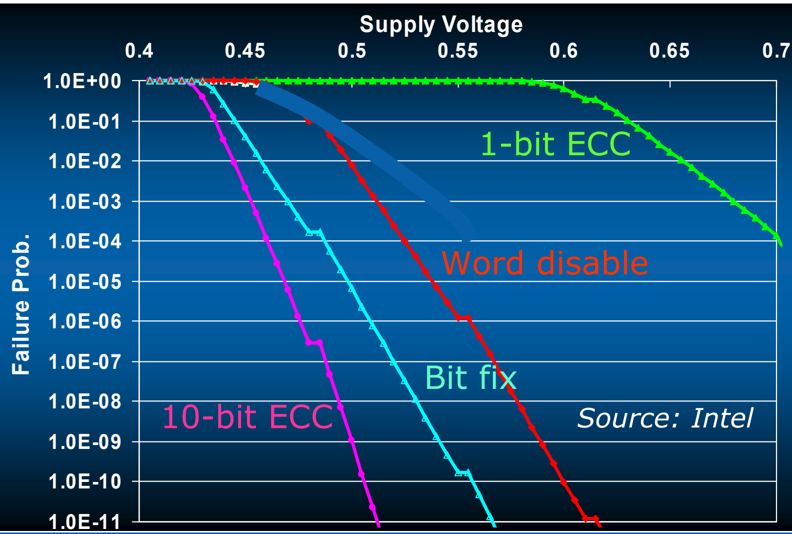
Reduce cache size @ low V/F by eliminating failing ***words/bits***

Word disable



Bit fix



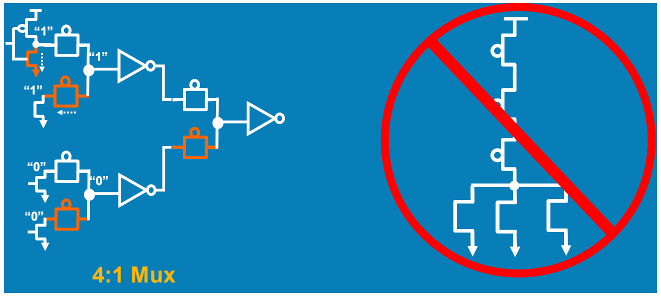


Source: Intel	Vmin (mV)	Density	Capacity	Latency (cycles)	IPC	EPI
Conventional	660	1*	1* (8-way)	L1: 3 L2: 20	1*	1*
32KB L1 Word disable	500	0.92	0.5 (4-way)	4	0.95	0.5
2MB L2 Bit fix	500	1	0.75 (6-way)	23	0.95	0.5

* Normalized reference value

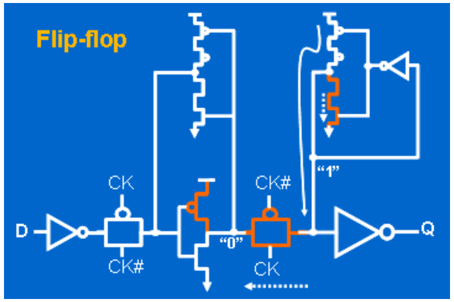
Low-voltage logic design

Narrow muxes

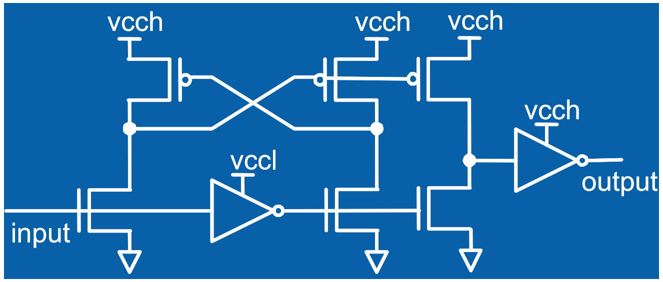


No stack height > 2

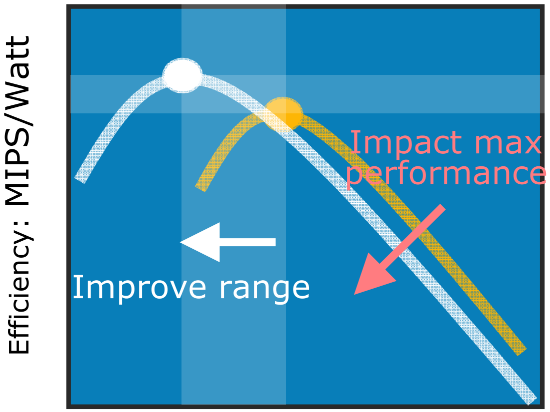
Robust flip-flops

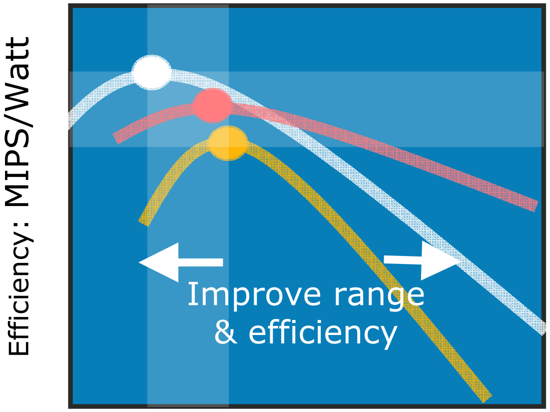


Robust level converters

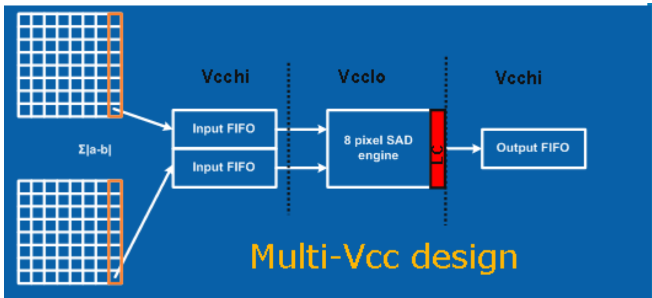


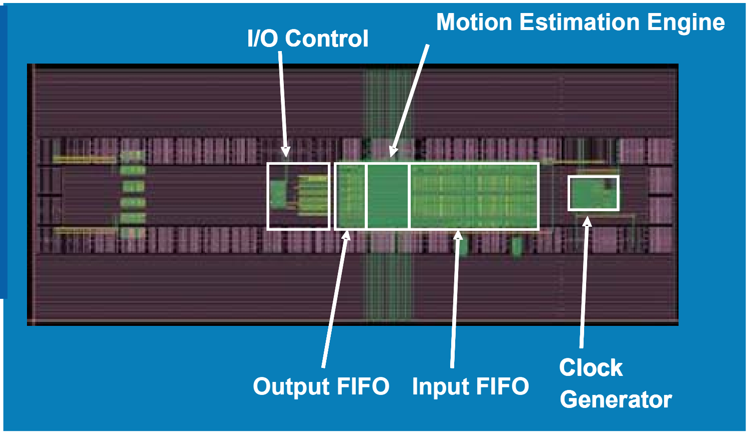
Design & technology optimizations to balance range, performance & efficiency





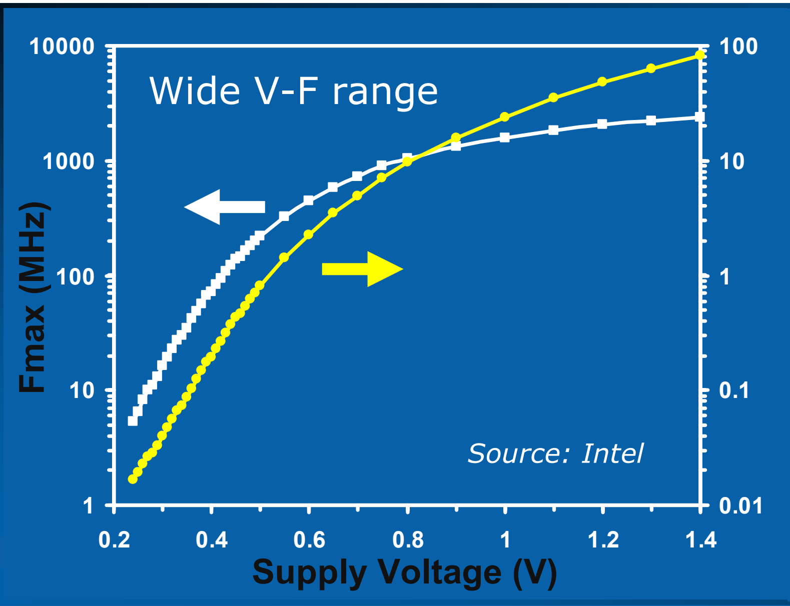
Low-voltage motion estimation engine

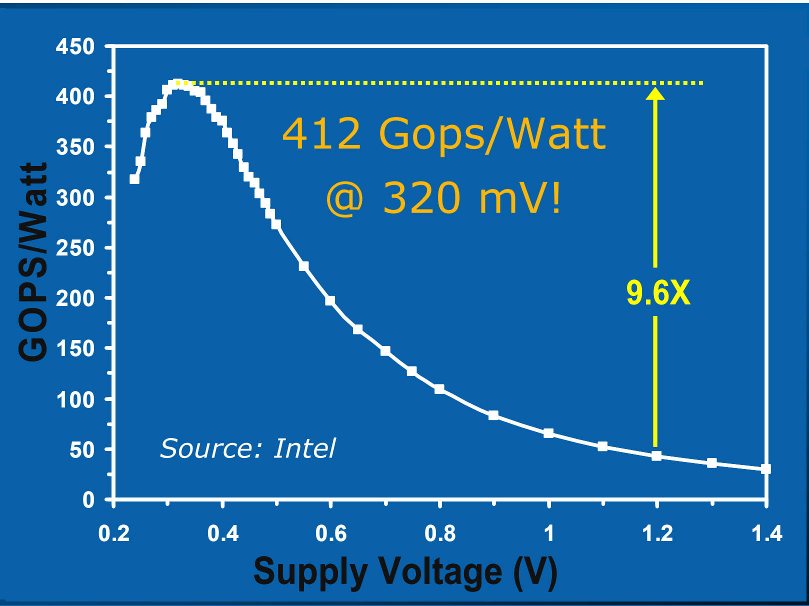




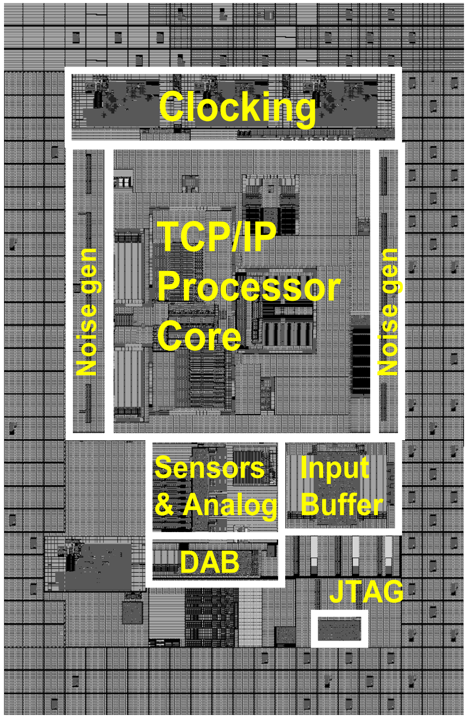
65nm CMOS
70K transistors
Die area ~1mm^2

Functional down to 240 mV!

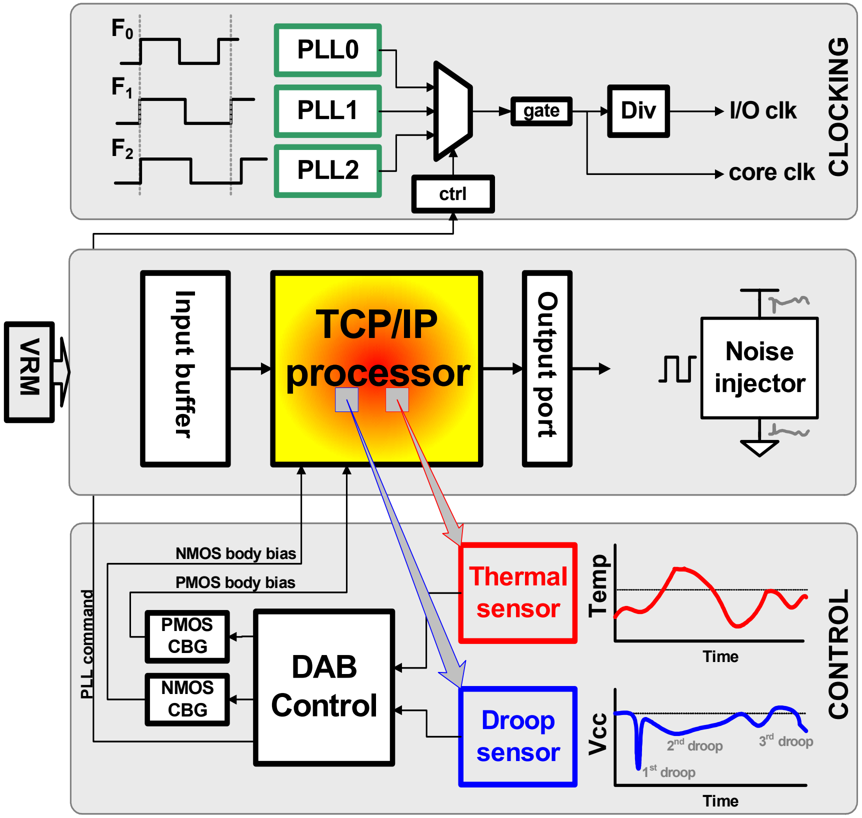


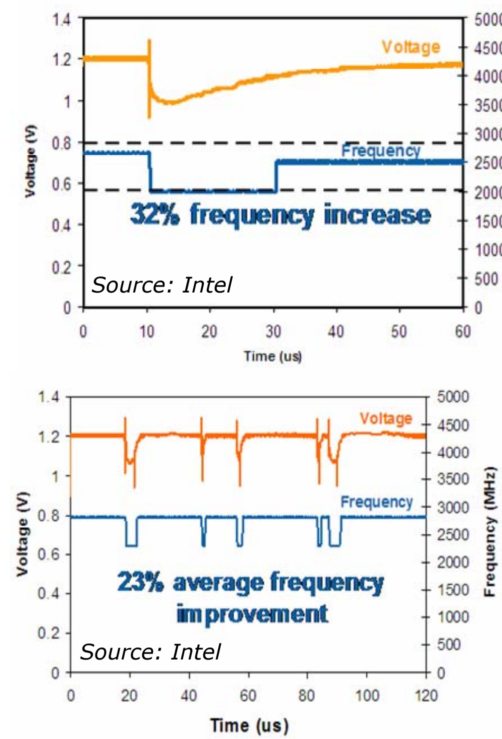


Dynamic V & F adaptation



Prototype chip in 90nm

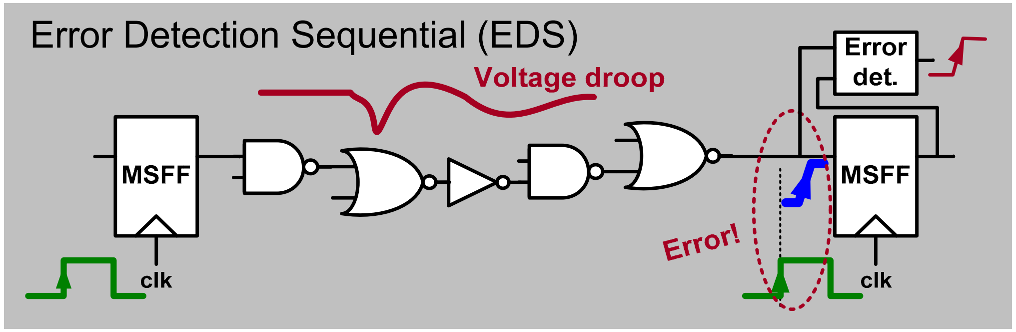




Environment-aware dynamic adaptation

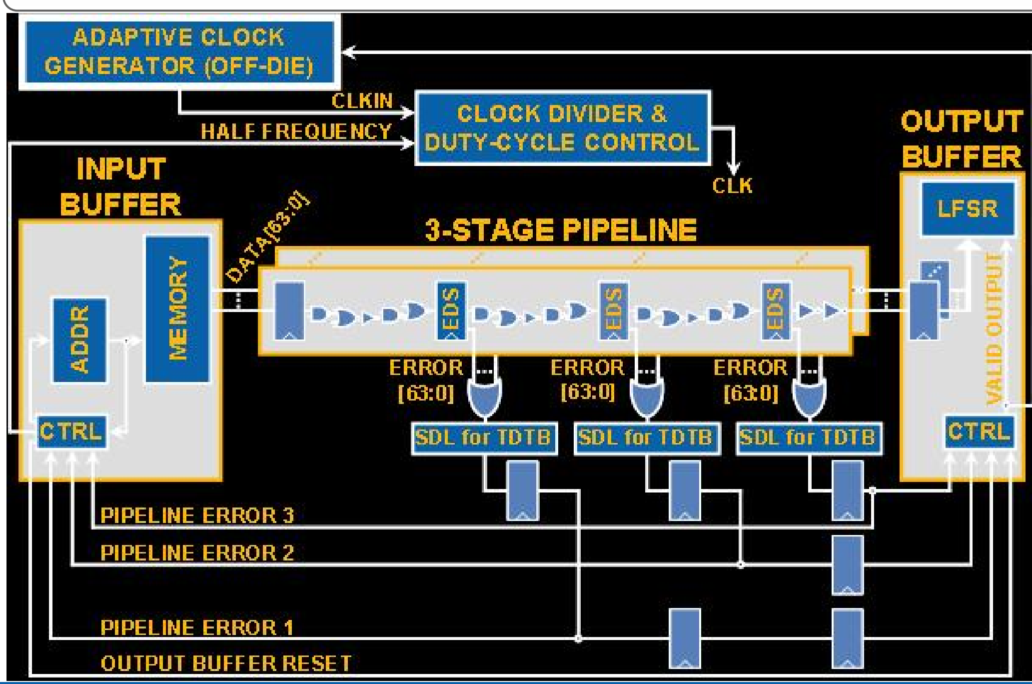
- Adapt F/V to V/T change → reduce V/T margin
- Adapt F/V to aging → reduce aging margin

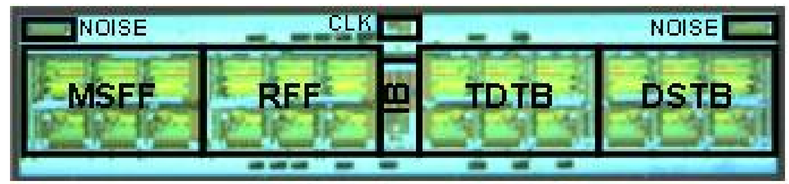
Resilient circuits

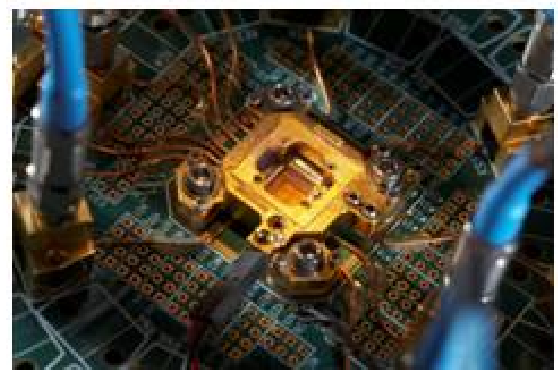


- Detect errors in critical path FFs
- Propagate error signals
- Correct errors by re-execution
- Feedback to adaptive V/F

65nm resilient circuits testchip

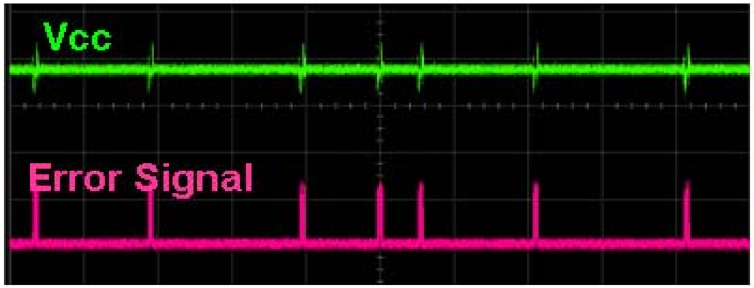


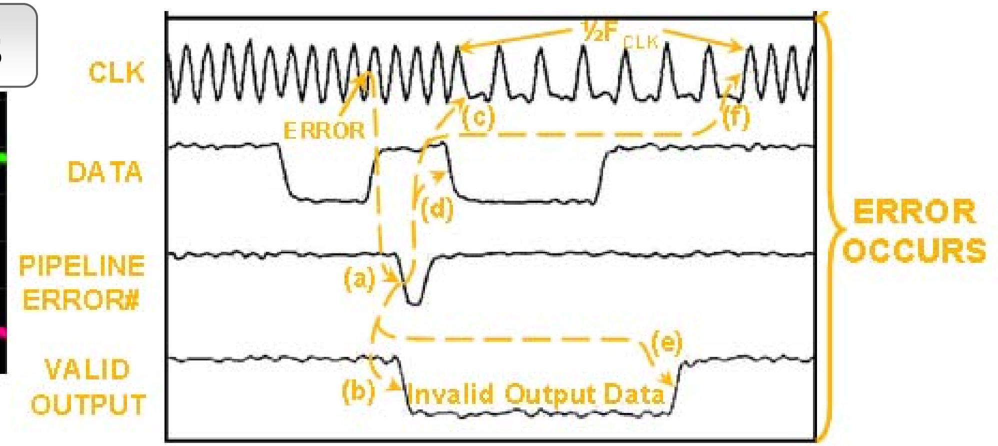


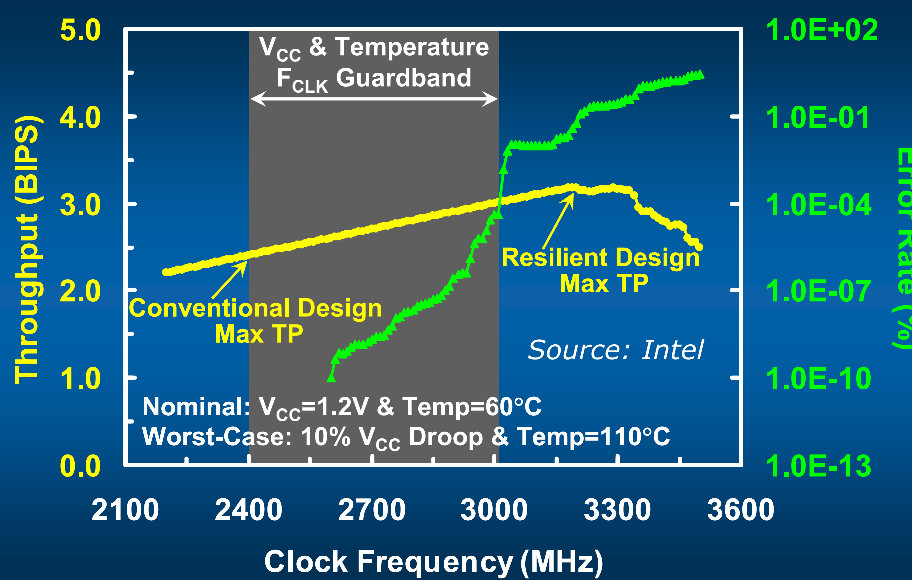


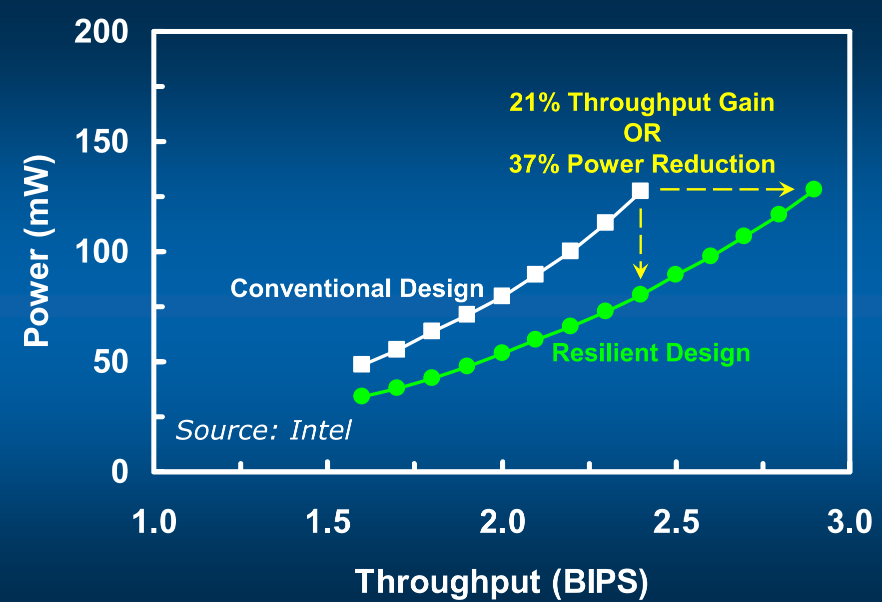
Resiliency experiments

Response to voltage droops









Summary

- Resilient platforms offer better performance, energy efficiency and reliability
- Resiliency, dynamic adaptation and reconfiguration will be critical in scaled CMOS
- Logic and memory design innovations will be needed to keep pushing the voltage scaling limits