ASP-DAC 2010

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  Authors: Naehyuck Chang, Jueun Seo, Donghwa Shin, and Younghyun Kim
  Affiliation of All Authors: Seoul National Univ., Republic of Korea
  Speaker: Naehyuck Chang

- **1D-2: Maximizing the Harvested Energy for Micro-Power Applications through Efficient MPPT and PMU Design**
  Authors: Hui Shao, Chi-Ying Tsui, Wing-Hung Ki
  Affiliation of All Authors: Hong Kong Univ. of Science and Technology, Hong Kong
  Speaker: Chi-Ying Tsui

- **1D-3: Dynamic Power Management in Environmentally Powered Systems**
  Authors: Clemens Moser, Jian-Jia Chen, and Lothar Thiele
  Affiliation of All Authors: ETH Zurich, Switzerland
  Speaker: Jian-Jia Chen

- **1D-4: Micro-scale energy harvesting: A system perspective**
  Authors: Lu Chao, Vijay Raghunathan, and Kaushik Roy
  Affiliation of All Authors: Purdue Univ., USA
  Speaker: Vijay Raghunathan

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- **2D-1: 3D Integration and Networks on Chips (Short Paper)**
  Authors: Srinivasan Murali (iNoCs/EPFL, Switzerland), Luca Benini (Univ. of Bologna, Italy), Giovanni De Micheli (EPFL, Switzerland)
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Recent Advancement in Post-Silicon Validation
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- **3D-1: Data Learning Based Diagnosis**
  Author: Li-C. Wang, Univ. of California, Santa Barbara, USA

- **3D-2: Using Introspective Software-Based Testing for Post-Silicon Debug and Repair**
  Author: Todd Austin, Univ. of Michigan, USA

- **3D-3: Post-Silicon Debugging for Multi-Core Designs**
  Author: Valeria Bertacco, Univ. of Michigan, USA

- **3D-4: Low-Cost Repair Techniques by Using Partitioning**
  Author: Kyungho Kim, Byungtae Kang, Dongyun Kim (Samsung Electronics Co., Republic of Korea), Sungchul Lee, Juyong Shin and Hyunchul Shin (Hanyang Univ., Republic of Korea)
  Speaker: Hyunchul Shin

- **3D-5: On Signal Tracing in Post-Silicon Validation**
  Author: Qiang Xu and Xiao Liu, Chinese Univ. of Hong Kong, Hong Kong
  Speaker: Qiang Xu

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Organizer & Moderator: Vincent Mooney, Georgia Tech/ Nanyang Technological Univ., USA

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  Authors: James Tschanz, Keith Bowman, Muhammad Khellah, Chris Wilkerson, Bibiche Geuskens, Dinesh Somasekhar, Arijit Raychowdhury, Jaydeep Kulkarni, Carlos Tokunaga, Shih-Lien Lu, Tanay Karnik, Vivek K. De
  Affiliation of All Authors: Intel Corp., USA
  Speaker: Vivek K. De

- **7D-2: Benefits and Barriers to Probabilistic Design**
  Author: Siva Narendra, Tyfone, Inc., USA

- **7D-3: A Probabilistic Boolean Logic for Energy Efficient Circuit and System Design**
  Author: Lakshmi N. B. Chakrapani (Rice Univ., USA), Krishna Palem (Rice Univ./Nanyang Technological Univ., USA)
  Speaker: Krishna Palem

- **7D-4: Panel Discussion: Dependable Silicon Design with Unreliable Components**
  Organizer & Moderator: Vincent Mooney, Georgia Tech/ Nanyang Technological Univ., USA
  Panelists: Vivek K. De, Intel Corp., USA
  Siva Narendra, Tyfone, Inc., USA
  Krishna Palem, Rice Univ./ Nanyang Technological Univ., USA

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  Author: Rainer Dömer, Univ. of California, Irvine, USA

- **8D-2: TLM Automation for Multi-Core Design**
  Author: Samar Abdi, Concordia Univ., Canada

- **8D-3: Platform Modeling for Exploration and Synthesis**
  Authors: Andreas Gerstlauer, Univ. of Texas at Austin, USA; Gunar Schirner, Northeastern Univ., USA
  Speaker: Andreas Gerstlauer

- **8D-4: Application of ESL Synthesis on GSM Edge Algorithm for Base Station**
  Author: Alan Su, Global Unichip Corp., Taiwan

Designers' Forum

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Ing-Jer Huang, National Sun Yat-Sen Univ., Taiwan

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An-Yeu (Andy) Wu, ITRI, Taiwan

- **5D-1: Overview of ITRI's Parallel Architecture Core (PAC) DSP Project: from VLIW DSP Processor to Android ready Multicore Computing Platform**
  An-Yeu (Andy) Wu, ITRI, Taiwan

- **5D-2: Design and Verification Methods of Toshiba's Wireless LAN Baseband SoC**
  Masanori Kuwahara, Toshiba, Japan

- **5D-3: Programmable Platform for Multimedia SoC**
  Bor-Sung Liang, Sunplus Core Technology, Taiwan

- **5D-4: SoC for Car Navigation Systems with a 53.3 GOPS Image Recognition Engine**
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Organizers: Cheng-Wen Wu, National Tsing Hua Univ./ITRI, Taiwan
Jin-Fu Li, National Central Univ./ITRI, Taiwan

- **6D-1: Tutorial: Is 3D Integration an Opportunity or Just a Hype?**
  Jin-Fu Li, National Central Univ./ITRI, Taiwan

- **6D-2: Panel Discussion: Is 3D Integration an Opportunity or Just a Hype?**
  Organizers & Moderators: Cheng-Wen Wu, National Tsing Hua Univ./ITRI, Taiwan
  Jin-Fu Li, National Central Univ./ITRI, Taiwan
  Panelists: Albert Li, GUC, Taiwan
  Erik Jan Marinissen, IMEC, Belgium
  Ding-Ming Kwai, ITRI, Taiwan
  Kyu-Myung Choi, Samsung, Republic of Korea
  Makoto Takahashi, Toshiba, Japan

Session 9D: Thursday, January 21, 13:30-15:10, Room 101D
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Organizers: Alan P. Su, Global Unichip Corp., Taiwan
Ing-Jer Huang, National Sun Yat-Sen Univ., Taiwan

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  Koichiro Yamashita, Fujitsu Laboratories Ltd., Japan

- **9D-2: Design of Complex Image Processing Systems in ESL**
  Benjamin Carrion Schafer (NEC Corp., Japan), Ashish Trambadia (NEC, Japan), Kazutoshi Wakabayashi (NEC Corp., Japan)
  Speaker: Kazutoshi Wakabayashi

- **9D-3: PAC Duo System Power Estimation at ESL**
  Wen-Tsan Hsieh, Jen-Chieh Yeh, Shi-Yu Huang (ITRI/ National Tsing Hua Univ., Taiwan)
  Speaker: Wen-Tsan Hsieh

- **9D-4: A Practice of ESL Verification Methodology from SystemC to FPGA -Using EPC Class-1 Generation-2 RFID Tag Design as an Example**
  William Young (TSMC, Taiwan), Chua-Huang Huang (Feng Chia Univ., Taiwan), Alan P. Su (Global Unichip Corp., Taiwan), C. P. Jou, Fu-Lung Hsueh (TSMC, Taiwan)
  Speaker: William Young

Session 10D: Thursday, January 21, 15:30-17:10, Room 101D
Oral Session: Embedded Software Development for Multi-Processor Systems-on-Chip
Organizers: Rainer Doemer, Univ. of California at Irvine, USA
Andreas Gerstlauer, Univ. of Texas at Austin, USA

Invited Talks:

- **10D-1: The Shrink Wrapped Myth: Cross Platform Software**
  Mike Olivarez (Freescale Semiconductor, Inc., USA)

- **10D-2: Using Software to Achieve Low Power Solutions**
  Albert Shiue (Alvaview Technologies, Taiwan)

- **10D-3: MPSoC Programming using the MAPS Compiler**
  Jeronimo Castrillon, Rainer Leupers (RWTH Aachen Univ., Germany)
  Speaker: Jeronimo Castrillon

- **10D-4: System-level Development of Embedded Software**
  Gunar Schirner (Northeastern Univ., USA)

Two Half-Day and Three Full-Day Tutorials

HALF-DAY Tutorials

Tutorial 1: Monday, January 18, 9:30-12:30, Room 101A
Embedded Software for System-on-Chip (SoC) Design
Organizer: Tie-Wei Kuo (National Taiwan Univ., Taiwan)
Speakers: Lothar Thiele (Swiss Federal Institute of Technology (ETH), Switzerland)
Tie-Wei Kuo (National Taiwan Univ., Taiwan)

Tutorial 2: Monday, January 18, 14:00 - 17:00, Room 101A
Analog and Mixed-Signal Circuit Design in Nanometer CMOS Technologies
Organizer & Speaker: Georges Gielen (Katholieke Universiteit Leuven, Belgium)

FULL-DAY Tutorials

Tutorial 3: Monday, January 18, 9:30-17:00, Room 101B
3D Integrated Circuit Design
Organizer: Sachin Sapatnekar (Univ. of Minnesota, USA)
Speakers: Paul Franzon (North Carolina State Univ., USA)
Ruchir Puri (IBM TJ Watson Research Center, USA)
Sachin Sapatnekar (Univ. of Minnesota, USA)
Yuan Xie (Pennsylvania State Univ., USA)

Tutorial 4: Monday, January 18, 9:30-17:00, Room 101C
Industrial Low-Power Circuit Design
Organizer: Pei-Hsin Ho (Synopsys Inc., USA)
Speakers: Louis Jiing-Yuan Lin (Global Unichip Corp., Taiwan)
Yoshio Inoue (Renesas Technology Corporation, Japan)
David Flynn (ARM Ltd., UK)
Pei-Hsin Ho (Synopsys Inc., USA)

Tutorial 5: Monday, January 18, 9:30-17:00, Room 101D
The Convergence and Inter-Relationship of Yield, Design for Manufacturability and Test
Organizer: Srikanth Venkataraman (Intel Corporation, USA)
Speakers: Srikanth Venkataraman (Intel Corporation, USA)
Robert C. Aitken (ARM Ltd., USA)

Welcome to ASP-DAC 2010

On behalf of the Organizing Committee, I would like to invite you to the 2010 Asia and South Pacific Design Automation Conference (ASP-DAC 2010) to be held on January 18-21, 2010 in Taipei, Taiwan. This is the first time that ASP-DAC comes to Taiwan. Taiwan is the place where many electronics systems and semiconductor devices are designed and manufactured. It has a very large community of academic researchers and industrial practitioners who are eager to interact with the world EDA community. In other words, Taiwan is a very good market for EDA ideas.

Taipei is the capital city of Taiwan. It is easily accessible by direct flight from major cities around the world. You will find many interesting places to visit. In addition to regular conference activity, the Organizing Committee will organize several social activities to enrich your trip.

Since 2006, in order to maintain quality and consistency of its technical program, ASP-DAC has established a rotation rule that includes the separation of the Technical Program Committee from the Organizing Committee. The 2010 Technical Program Committee under the leadership of Professor Shinji Kimura of Waseda University, Japan, has put together an excellent technical program. Keeping up with ASP-DAC tradition, the conference features five tutorials on leading-edge EDA challenges and opportunities, University LSI Design Contest, Ph.D. student forum, and designer's track. We are very grateful to have three excellent keynoters: Professor C. L. Liu of National Tsing Hua University, Dr. Wally Rhines of Mentor Graphics, and Mr. Jim Lai of Global Unichip Corp. They will give us very different views of EDA.

Local volunteers and conference management team have worked very hard over the past year for the conference's success. I sincerely welcome you all to Taipei for ASP-DAC 2010.

Youn-Long Lin
General Chair
ASP-DAC 2010, Taipei, Taiwan

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General Chair
Youn-Long Lin
Department of Computer Science
National Tsing Hua University
ylin@cs.nthu.edu.tw

Past Chair
Kazutoshi Wakabayashi
NEC Corporation
wakaba@bl.jp.nec.com

OC Secretary
Juinn-Dar Huang
National Chiao Tung University
jdhuang@mail.nctu.edu.tw

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ASP-DAC 2010 Secretariat
Rm. 200, Bldg. 9, 195, Sec. 4, Chung Hsing Rd.
Chutung, Hsinchu , Taiwan 310, R.O.C.
TEL: 886-3-5919039
FAX: 886-3-5820420
E-mail:aspdac2010@aspdac.com

Visit Our Web Site
http://www.aspdac.com

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Technical Program Chair
Shinji Kimura
Waseda Univ.,Japan
shinji_kimura@waseda.jp

Technical Program Vice Chairs
Hyunchul Shin
Hanyang Univ.,Korea
shin@hanyang.ac.kr

Jing-Jia Liou
National Tsing Hua Univ.,Taiwan
jjliou@ee.nthu.edu.tw

Secretaries
Nozomu Togawa
Waseda Univ.,Japan
ntogawa@waseda.jp

Shigetoshi Nakatake
Univ. of Kitakyushu.,Japan
nakatake@env.kitakyu-u.ac.jp

TPC Subcommittees

(* indicates the subcommittee chair.)

[1] System-Level Modeling and Simulation/Verification

***Sri Parameswaran** (Univ. of New South Wales, Australia)
Ing-Jer Huang (National Sun Yat-Sen Univ., Taiwan)
Chia-Lin Yang (National Taiwan Univ., Taiwan)
Nagisa Ishiura (Kwansei Gakuin Univ., Japan)
Joerg Henkel (Univ. of Karlsruhe., Germany)

[2] System-Level Synthesis and Optimization

***Yuichi Nakamura** (NEC Corp., Japan)
Li Shang (Univ. of Colorado, USA)
Danella Zhao (Univ. of Louisiana at Lafayette, USA)
Tsuyoshi Isshiki (Tokyo Institute of Tech., Japan)
Lovic Gauthier (Kyusyu Univ., Japan)
Jen-Chieh Yeh (ITRI, Taiwan)

[3] System-Level Memory/Communication Design and Networks on Chip

***Hiroyuki Tomiyama** (Nagoya Univ., Japan)
Samar Abdi (Univ. of California, Irvine, USA)
Preeti Ranjan Panda
(Indian Institute of Technology, Delhi, India)
Tulika Mitra (National Univ. of Singapore, Singapore)
Yoshinori Takeuchi (Osaka Univ., Japan)
Sungjoo Yoo (POSTECH, Korea)
Michihiro Koibuchi (NII, Japan)
Cheng-Yeh Wang (MediaTek Inc., Taiwan)
Yunheung Paek (Seoul National University, Korea)

[4] Embedded and Real-Time Systems

***Samarjit Chakraborty**
(Technical Univ. of Munich, Germany)
Naehyuck Chang (Seoul National. Univ., Korea)
Zonghua Gu (HKUST, Hong Kong)
Chi-Sheng Shih (National Taiwan Univ., Taiwan)
Prabhat Mishra (Univ. of Florida, USA)
Eli Bozorgzadeh (Univ. of California, Irvine, USA)
Zili Shao (Polytechnic Univ., Hong Kong,China)
Chun Jason Xue (City Univ. of Hong Kong, Hong Kong)
Tei-Wei Kuo (National Taiwan Univ., Taiwan)

[5] High-Level/Behavioral/Logic Synthesis and Optimization

***Deming Chen** (Univ. of Illinois at Urbana-Champaign, USA)
Ani Nahapetian (Univ. of California, Los Angeles, USA)
Hiroyuki Higuchi (Fujitsu Microelectronics Limited, Japan)
Ting-Ting Hwang (National Tsing Hua Univ., Taiwan)
Taewhan Kim (Seoul National Univ., Korea)
Yuan Xie (Pennsylvania State Univ., USA)
Shigeru Yamashita (Ritsumeikan Univ., Japan)

[6] Validation and Verification for Behavioral/Logic Design

***Shin'ichi Minato** (Hokkaido Univ., Japan)
Yirng-An Chen (Marvell Corp., USA)
Kiyoharu Hamaguchi (Osaka Univ., Japan)
Chung-Yang Huang (National Taiwan Univ., Taiwan)
Miroslav Velev (Aries Design Automation, USA)
Farn Wang (National Taiwan Univ., Taiwan)
Yoshinori Watanabe (Cadence, USA)

[7] Physical Design

***Yao-Wen Chang** (National Taiwan Univ., Taiwan)
Sheqin Dong (Tsinghua Univ., China)
Jeong-Tyng Li (SpringSoft, USA)
Yih-Lang Li (National Chiao Tung Univ., Taiwan)
Sherief Reda (Brown Univ., USA)
Cliff Sze (IBM Research, USA)
Yasuhiro Takashima (Univ. of Kitakyushu, Japan)
Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, USA)
Evangeline F.Y. Young
(The Chinese Univ. of Hong Kong, Hong Kong)

[8] Timing, Power Thermal Analysis and Optimization

***Youngsoo Shin** (KAIST, Korea)
Matthew Guthaus (Univ. of California, Santa Cruz, USA)
Shih-Hsu Huang (Chung Yuan Christian Univ., Taiwan)
Volkan Kursun
(Hong Kong Univ. of Science and Technology, Hong Kong)
Kimiyoshi Usami (Shibaura Institute of Technology , Japan)
Hongliang Chang (Cadence, USA)
Massimo Poncino (Politecnico di Torino, Italy)

[9] Signal/Power Integrity, Interconnect/Device/Circuit Modeling and Simulation

***Hideki Asai** (Shizuoka Univ., Japan)
Kimihiro Ogawa (STARC(Sony) Japan)
Yu-Min Roger Lee (National Chiao Tung Univ., Taiwan)
En-Xiao Liu
(Institute of High Performance Computing (IHPC), Singapore)
Zuochang Ye (Tsinghua Univ., China)
Sungroh Yoon (Korea Univ., Korea)
Kyu-won Ken Choi (Illinois Institute of Technology, USA)

[10] Design for Manufacturability/Yield and Statistical Design

***Toshiyuki Shibuya** (Fujitsu Labs. America, USA)
David Pan (The Univ. of Texas at Austin, USA)
Keh-Jeng Chang (National Tsing Hua Univ., Taiwan)
Puneet Gupta (Univ. of California, Los Angeles, USA)
Fedor G. Pikus (Mentor Graphics Corporation, USA)
Zeng Shi (Zhejiang University, China)

[11] Test and Design for Testability

***Seiji Kajihara** (Kyusyu Institute of Technology, Japan)
Shi-Yu Huang (National Tsing Hua Univ., Taiwan)
Wu-Tung Cheng (Menter Graphics, USA)
Ming-Der Shieh (National Cheng Kung Univ., Taiwan)
Tomokazu Yoneda (NAIST, Japan)

[12] Analog, RF and Mixed Signal Design and CAD

***Jaijeet Roychowdhury** (Univ. of California, Berkeley, USA)
Alper Demir (Koc Univ., Turkey)
Chin-Fong Chiu (National Chip Implementation Center, Taiwan)
Eric Keiter (Sandia National Labs, Albuquerque, NM, USA)
Woogeun Rhee (Tsinghua Univ., China)

[13] Emerging Technologies and Applications

***Chin-Long Wey** (National Central Univ., Taiwan)
Arfan Ghani (Univ. of Ulster, N. Ireland, UK)
In-Cheol Park (KAIST, Korea)
Mehdi Baradaran Tahoori (Northeastern University, USA)
Chun-Ming Huang (National Chip Implementation Center, Taiwan)
Xiaoyang Zeng (Fudan Univ., China)

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Chair

Jiun-In Guo
National Chung Cheng University, Taiwan
jiguo@cs.ccu.edu.tw

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Tohoku University, Japan
hariyama@ecei.tohoku.ac.jp

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Lih-Yih Chiou
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lihyih@mail.ncku.edu.tw

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yasuura@c.csce.kyushu-u.ac.jp

Vice Chair
Hidetoshi Onodera
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onodera@vlsi.kuee.kyoto-u.ac.jp

Secretaries
Toshihiro Hattori
RENESAS Technology Corporation
hattori.toshihiro@renesas.com

Atsushi Takahashi
Osaka University
atsushi@si.eei.eng.osaka-u.ac.jp

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University LSI Design Contest

The University LSI Design Contest was conceived as a unique program of ASP-DAC Conference. The purpose of the Contest is to encourage education and research in LSI design, and its realization on chips at universities, and other educational organizations by providing opportunities to present and discuss innovative and state-of- the-art designs at the conference. Application areas and types of circuits include:

(1) Analog, RF and Mixed-Signal Circuits,
(2) Digital Signal processing,
(3) Microprocessors, and
(4) Custom Application Specific Circuits and Memories.

Methods or technology used for implementation include:
(a) Full Custom and Cell-Based LSIs,
(b) Gate Arrays, and
(c) Field Programmable Devices, including FPGA/PLDs.

This year, 20 selected designs from six countries/areas will be disclosed in Session 4D with a short presentation followed by live discussions in front of posters with light meas. Submitted designs were reviewed by the members of the University Design Contest Committee. As a result, the 20 designs were selected. Also, we have instituted one outstanding design award from the selected designs.

It is with great pleasure that we acknowledge the contributions to the Design Contest, and it is our earnest belief that it will promote and enhance research and education in LSI design in academic organizations. It is also our hope that many people not only in academia but in industry will attend the contest and enjoy the stimulating dicussions.

- **Date:** Wednesday, January 20, 2010
- **Place:** Taipei International Convention Center, 1F
  1) Oral Presentation : Room 101D (10:30-12:10)
  2) Poster Presentation : Room 103
  [Food will be served] (12:10-13:30)

University LSI Design Contest Committee

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Jiun-In Guo

National Chung Cheng University, Taiwan

Co-Chair

Masanori Hariyama

Tohoku University, Japan

Designers' Forum

Designers' Forum is conceived as a unique program that shares the design experience and solutions of real product developments among hardware/software designers and EDA researchers/developers. This year it consists of four special sessions on the topics of SoC development, 3D IC integration, ESL design methodology and embedded software development.

Oral Sessions

5D : State-of-the-art SoCs
9D : ESL, the Road to Glory, or Is It Not? Real Stories about Using ESL Design Methodology in Product Development
10D: Embedded Software Development for Multi-Processor Systems-on-Chip

Tutorial and Panel Discussion:
6D : Is 3D Integration an Opportunity or Just a Hype?

Designs will be presented focusing mainly on the design styles, problems and ways to tackle these. Panel discussions will also be held concerning the latest design problems. The following gives detailed information of each session:

Session 5D: State-of-the-art SoCs
Wednesday, January 20, 13:30 - 15:10, Room 101D

For digital systems in today's digital-convergence era, various functions such as communication, security, audio, video, and recognition must be implemented by an SoC. Functional diversification will keep increasing, and demands for the improvement of the SoC's functionality and performance will thus continue. The latest SoCs must meet these requirements while considering cost, power consumption, reliability, and so on. Facing these challenges, new hardware/software technologies and design methodologies are indispensable. In light of our pursuit of advanced technologies for the SoCs, this session is devoted to an exploration of the latest advances in not only hardware/software implementations but also

design tools and methods for the developments. Four representatives are invited from both industry and academia, and the state-of-the-art technologies are presented and discussed in the session.

Session 6D: Is 3D Integration an Opportunity or Just a Hype?
Wednesday, January 20, 15:30-17:10, Room 101D

Three-dimensional (3D) integration using through-silicon via (TSV) provides numerous opportunities to designers looking for more cost-effective system chip solutions. In addition to stacking homogeneous memory dies, 3D integration technology supports heterogeneous integration of memories, logic,sensors, etc. It eases the interconnect performance limitation, provides higher functionality, results in small form factor, etc. On the other hand, there are challenges that should be overcome before volume production of TSV-based 3D ICs becomes possible, e.g., technological challenges, yield and test challenges, thermal and power challenges, infrastructure challenges, etc.

Foundries like IBM and Tezzaron have announced that they are ready for volume shipments of some special chips with 3D technology. Does this mean that 3D integration has a bright future? Or will we eventually see that 3D integration works only for some specific applications? This session first gives an embedded tutorial which introduces basics of 3D ICs. Then a panel of experts in this area will give position statements and elaborate their perspectives of opportunities and challenges on 3D ICs. Finally, the panel will be open for discussion between the audience and the panelists.

Session 9D: ESL, the Road to Glory, or Is It Not? Real Stories about Using ESL Design Methodology in Product Development
Thursday, January 21, 13:30 - 15:10, Room 101D

Electronic System Level design methodology (ESL) has been widely used in leading design houses for SoC designs. However still many designers have not adopted the technology. In this session

we invite ESL users to share ESL experiences, the road to glory, or not, to help designers to make wise decisions in moving into ESL. Designers talk about their experiences in using ESL to design real products. Benefit of using ESL, suggestions to adopt ESL design flow and tool package needed to use ESL are discussed. The first talk gives an insight into SW and HW co-design for multi-core SoC based embedded systems, one of the key focuses in ESL. The second talk discusses how ESL not only reduces the development time but also facilitates the communication between algorithm designers and hardware developers. The third talk shows a power estimation framework which uses the proposed power model interface to integrate the various power models in system level for a dual-core SoC. The fourth talk describes how ESL/FPGA co-emulation verification helps the design of a RFID tag chip.

Session 10D: Embedded Software Development for Multi-Processor Systems-on-Chip
Thursday, January 21, 15:30-17:10, Room 101D

While embedded system complexities continue to grow exponentially, the software content is constantly increasing, yet the productivity of developing such software is lagging behind that of hardware. In fact, software has become the most important part of the system. For most embedded systems today, it is the software that defines the overall speed, efficiency, power consumption, and capabilities of the system. However, the embedded software is typically only addressed as an afterthought and "shoe horned" into the device.

This session deals with the issues to cope with the ever increasing complexity of embedded systems software. It presents different views by both industry and academia representatives on the challenges and potential solutions for embeddd software development for multi-processor systems-on-chip (MPSoC). Two talks from the industrial perspective discuss the issues and challenges involved in developing commercial software for real-world embedded systems, followed by two talks from the academic community that

outline promising approaches to automate and overcome key issues in software development for the future.

The first presentation discusses the challenges in developing embedded software across multiple platforms and specifically addresses portability issues in supporting multiple OSes for cell phone applications. The second presentation addresses low power aspects in hardware-dependent software that can be optimized using advanced compilation techniques. The third presentation highlights the MAPS compiler, an integrated programming environment for multiple simultaneous applications on MPSoC. MAPS supports both sequential and parallel programming models and targets efficient code generation for predefined heterogeneous MPSoC platforms. The fourth presentation presents research results on system-level modeling of embedded software and automatic code generation for an efficient implementation. Issues including device driver generation and efficient multi-tasking are addressed as well.

Designers' Forum Chair
Ing-Jer Huang (National Sun Yat-Sen Univ., Taiwan)

Designers' Forum Vice Chairs
Rainer Doemer (Univ. of California, Irvine, USA)
Alan P. Su (Global Unichip Corp., Taiwan)
Kunio Uchiyama (Hitachi, Japan)
Cheng-Wen Wu (National Tsing Hua Univ/ITRI., Taiwan)

Student Forum at ASP-DAC 2010

A poster session for graduate students to present their research works is held during ASP-DAC 2010. This is a great opportunity for students to get feedback and have discussions with people from academia and industry.

Date and Time : 12:20-13:30, January 19, 2010
Location : Room 103 (Food will be served.)

I would like to thank the following committee members for their support and contribution to the Student Forum:

Poster Selection Committee:
Eui-Young Chung (Yonsei University, Korea)
Sung Woo Chung (Korea University, Korea)
Koji Hashimoto (Fukuoka University, Japan)
Yongsoo Joo (Pennsylvania State University, USA)
Hyung-Ock Kim (Samsung Electronics, Korea)
Hyung Gyu Lee (Samsung Electronics, Korea)
Yih-Lang Li (National Chiao Tung University, Taiwan)
Chien-Nan Jimmy Liu (National Central University, Taiwan)
Yung-Hsiang Lu (Purdue University, USA)
Kohei Miyase (Kyushu Institute of Technology, Japan)
Shinobu Nagayama (Hiroshima City University, Japan)
Hiroshi Saito (University of Aizu, Japan)
Dongwan Shin (Qualcomm, Korea)
Chun-Yao Wang (National Tsing Hua University, Taiwan)
Takayuki Watanabe (University of Shizuoka, Japan)
David Wu (Chinese University of Hong Kong, Hong Kong)
Chia-Lin Yang (National Taiwan University, Taiwan)

Advisory Committee:
Naehyuck Chang (Seoul National University, Korea)
Yasuhiro Takashima (University of Kitakyushu, Japan)
Special thanks go to ASP-DAC 2010 for sponsoring this forum.

Chair:
Ting-Chi Wang
National Tsing Hua University, Taiwan

Invitation to the ASP-DAC 2011

ASP-DAC 2011 will come back to its home town, Yokohama, Japan, again. On behalf of all the committee members of 2011, I would like to welcome you to Yokohama, one of the most attractive cities in Japan, where traditional and modern cultures are coexisting in harmony.

General Chair
Kunihiro Asada
University of Tokyo
asada@silicon.t.u-tokyo.ac.jp

Keynote Addresses

Keynote I

Tuesday, January 19, 9:00-10:00, Taipei International Convention Center, Room 101

"I Attended the Nineteenth Design Automation Conference"
Chung-Laung Liu
Chair Professor of National Tsing Hua University

I presented a technical paper at the Nineteenth Design Automation Conference in 1982. Twenty Eight years since then was a short time, a long time, and a wonderful time for the profession!

Keynote II

Tuesday, January 19, 10:20-11:20, Taipei International Convention Center, Room 101

"Delivering 10X Design Improvements"
Walden C. Rhines
Chairman and Chief Executive Officer of Mentor Graphics

Time and time again, escalating complexity has threatened to derail the IC industry from the extraordinary 35% annual reduction in transistor pricing it has enjoyed the past 40+ years. Fortunately, in each and every instance, creative engineers and companies have seen this as a challenge and opportunity to innovate. As a result, the electronic design automation industry has repeatedly delivered order of magnitude improvements in every aspect of the IC design cycle for over three decades.
.

Today, the exponential rise in complexity has quickened its pace as the industry moves toward adoption of 28 nm and below. Dr. Wally Rhines will discuss how in the next five years, 10X improvements in design methodologies are needed in four principal areas: high-level system design, verification, embedded software development, and back-end physical design and test. He will provide a roadmap for the next wave of changes needed to successfully negotiate rising complexity, highlighting where they will most likely occur.

Keynote III

Tuesday, January 19, 11:20-12:20, Taipei International Convention Center, Room 101

"IC Design for the Intuitive Life Style"
Jim Lai
President of Global Unichip Corp.

In the past two decades, computer, consumer and communication products remain the main driving force to push design technology further deep to advanced technolog node. The consumer market seems to run out of fuel in the past year. Will new innovation or convergence drive the next explosion in consumer applications? In this speech, Mr. Jim Lai will express how our lifestyle has been changed by technology and how human needs push the IC design to different applcations. From the close observation of the IC design industry, he will point out the challenges which IC design industry currently face, and draw the trend and potential solutions to support the continuous evolution of human life.

Technical Program

Tuesday, January 19, 13:30 - 15:10

Tuesday, January 19, 13:30 - 15:10 Room 101A
Session 1A: Embedded Systems Design Techniques

Chairs: ***Chun Jason Xue*** - City Univ. of Hong Kong, Hong Kong
Tei-Wei Kuo - National Taiwan Univ., Taiwan

1A-1 A PUF Design for Secure FPGA-Based Embedded Systems
Jason H. Anderson (Univ. of Toronto, Canada)

1A-2 Adaptive Power Management for Real-Time Event Streams
Kai Huang (ETH Zurich, Switzerland), Luca Santinelli (Scuola Superiore Sant'Anna of Pisa, Italy), Jian-Jia Chen, Lothar Thiele (ETH Zurich, Switzerland), Giorgio C. Buttazzo (Scuola Superiore Sant'Anna of Pisa,Italy)

1A-3 An Alternative Polychronous Model and Synthesis Methodology for Model-Driven Embedded Software
Bijoy Antony Jose, Sandeep Kumar Shukla (FERMAT Lab, Virginia Tech, U.S.A.)

1A-4 Trace-based Performance Analysis Framework for Heterogeneous Multicore Systems
Shih-Hao Hung, Chia-heng Tu, Thean-Siew Soon (National Taiwan Univ., Taiwan)

Tuesday, January 19, 13:30 - 15:10 Room 101B
Session 1B: Advanced Model Order Reduction Technique

Chairs: ***Hideki Asai*** - Shizuoka Univ., Japan
Sheldon Tan - Univ. of California, Riverside, U.S.A.

1B-1 Efficient Model Reduction of Interconnects Via Double Gramians Approximation
Boyuan Yan, Sheldon Tan (Univ. of California, Riverside, U.S.A.) ,Gengsheng Chen (Fudan Univ., China), Yici Cai (Tsinghua Univ., China)

1B-2 Wideband Reduced Modeling of Interconnect Circuits by Adaptive Complex-Valued Sampling Method
Hai Wang, Sheldon Tan (Univ. of California, Riverside, U.S.A.), Gengsheng Chen (Fudan Univ., China)

1B-3 VISA: Versatile Impulse Structure Approximation for Time-Domain Linear Macromodeling
Chi-Un Lei, Ngai Wong (Univ. of Hong Kong, Hong Kong)

1B-4 An Extension of the Generalized Hamiltonian Method to S-parameter Descriptor Systems
Zheng Zhang, Ngai Wong (Univ. of Hong Kong, Hong Kong)

Tuesday, January 19, 13:30 - 15:10 Room 101C
Session 1C: Logic Synthesis

Chairs: ***Yuan Xie*** - Pennsylvania State Univ., U.S.A.
Shih-Chieh Chang - National Tsing Hua Univ., Taiwan

1C-1 Simultaneous Slack Budgeting and Retiming for Synchronous Circuits Optimization
Shenghua Liu, Yuchun Ma, Xian-Long Hong, Yu Wang (Tsinghua Univ., China)

1C-2 A Fast SPFD-based Rewiring Technique
Pongstorn Maidee, Kia Bazargan(Univ. of Minnesota, U.S.A.)

1C-3 iRetILP: An Efficient Incremental Algorithm for Min-period Retiming under General Delay Model
Debasish Das (Northwestern Univ., U.S.A.), Jia Wang (Illinois Inst. of Tech., U.S.A.), Hai Zhou (Northwestern Univ., U.S.A.)

Tuesday, January 19, 13:30 - 15:10 Room 101D
Session 1D: Special Session: Techniques for Efficient Energy Harvesting and Generation for Portable and Embedded Systems

Organizer &Chair: ***Pai Chou*** - Univ. of California, Irvine/National Tsing Hua Univ., U.S.A.

1D-1 Room-Temperature Fuel Cells and their Integration into Portable and Embedded Systems
Naehyuck Chang, Jueun Seo, Donghwa Shin, Younghyun Kim (Seoul National Univ., Republic of Korea)

1D-2 Maximizing the Harvested Energy for Micro-power Applications through Efficient MPPT and PMU Design
Hui Shao, Chi-ying Tsui, Wing-Hung Ki (Hong Kong Univ. of Science and Tech., Hong Kong)

1D-3 Dynamic Power Management in Environmentally Powered Systems
Clemens Moser, Jian-Jia Chen, Lothar Thiele (ETH Zurich, Switzerland)

1D-4 Micro-scale Energy Harvesting: A System Perspective
Lu Chao, Vijay Raghunathan, Kaushik Roy (Purdue Univ., U.S.A.)

Tuesday, January 19, 15:30 - 17:10

Tuesday, January 19, 15:30 - 17:10 Room 101A
Session 2A: Memory Management and Compiler Techniques

Chairs: ***Zili Shao*** - Hong Kong Polytechnic Univ.,China
Jian-Jia Chen - ETH Zurich, Switzerland

2A-1 Co-Optimization of Memory Access and Task Scheduling on MPSoC Architectures with Multi-Level Memory
Yi He (Univ. of Texas, Dallas, U.S.A.), Chun Jason Xue (City Univ. of Hong Kong, Hong Kong), Cathy Qun Xu, Edwin Sha (Univ. of Texas, Dallas, U.S.A.)

2A-2 A New Compilation Technique for SIMD Code Generation across Basic Block Boundaries
Hiroaki Tanaka, Yutaka Ota, Nobu Matsumoto (Toshiba Corp., Japan), Takuji Hieda, Yoshinori Takeuchi, Masaharu Imai (Osaka Univ., Japan)

2A-3 LibGALS: A Library for GALS Systems Design and Modeling
Wei-Tsun Sun, Zoran Salcic, Avinash Malik (Univ. of Auckland, New Zealand)

2A-4 Joint Variable Partitioning and Bank Selection Instruction Optimization on Embedded Systems with Multiple Memory Banks
Tiantian Liu, Minming Li, Chun Jason Xue (City Univ. of Hong Kong, Hong Kong)

Tuesday, January 19, 15:30 - 17:10 Room 101B
Session 2B: Power and Signal Integrity

Chairs: ***Yu-Min Roger Lee*** - National Chiao Tung Univ., Taiwan
Hsin-Po Wang - SpringSoft, Taiwan

2B-1 On-Chip Power Network Optimization with Decoupling Capacitors and Controlled-ESRs
Wanping Zhang (Qualcomm Inc./UCSD, U.S.A.), Ling Zhang, Amirali Shayan (UCSD, U.S.A.), Wenjian Yu (Tsinghua Univ.,U.S.A.), Xiang Hu (UCSD, U.S.A.), Zhi Zhu (Qualcomm Inc.,U.S.A.), Ege Engin (SDSU,U.S.A.), Chung-Kuan Cheng (UCSD, U.S.A.)

2B-2 An Adaptive Parallel Flow for Power Distribution Network Simulation Using Discrete Fourier Transform
Xiang Hu, Wenbo Zhao, Peng Du, Amirali Shayan, Chung-Kuan Cheng (Univ. of California, San Diego,U.S.A.)

2B-3 Technique for Controlling Power-Mode Transition Noise in Distributed Sleep Transistor Network
Yongho Lee, Taewhan Kim (Seoul National Univ., Republic of Korea)

2B-4 A Novel FDTD Algorithm Based on Alternating-Direction Explicit Method with PML Absorbing Boundary Condition
Shuichi Aono (SESAME Technology Inc., Japan), Masaki Unno, Hideki Asai (Shizuoka Univ., Japan)

Tuesday, January 19, 15:30 - 17:10 Room 101C
Session 2C: System-level Simulation

Chair: ***Chia-Lin Yang*** **-** National Taiwan Univ., Taiwan

2C-1 Speeding Up SoC Virtual Platform Simulation by Data-Dependency-Aware Synchronization and Scheduling
Kuen-Huei Lin, Siao-Jie Cai, Chung-Yang (Ric) Huang (National Taiwan Univ., Taiwan)

2C-2 SCGPSim: A Fast SystemC Simulator on GPUs
Mahesh Nanjundappa (Virginia Polytechnic Inst. and State Univ., U.S.A.), Hiren D Patel (Univ. of Waterloo, Canada), Bijoy A Jose, Sandeep K Shukla (Virginia Polytechnic Inst. and State Univ., U.S.A.)

2C-3 A Flexible Hybrid Simulation Platform Targeting Multiple Configurable Processors SoC
Hao Shen, Frédéric Pétrot (TIMA Laboratory, INP Grenoble, France)

2C-4 A Fast Heuristic Scheduling Algorithm for Periodic ConcurrenC Models
Weiwei Chen, Rainer Doemer (Univ. of California, Irvine, U.S.A.)

Tuesday, January 19, 15:30 - 17:10 Room 101D
Session 2D: Special Session: 3D Integration and Networks on Chips

Organizer & Moderator:
Srinivasan Murali **-** iNoCs/EPFL, Switzerland

2D-1 3D Integration and Networks on Chips (Short Paper)
Srinivasan Murali (iNoCs/EPFL, Switzerland), Luca Benini (Univ. of Bologna, Italy), Giovanni De Micheli(EPFL, Switzerland)

2D-2 3D Integration and Networks on Chips (Panel)
Organizer & Moderator:
Srinivasan Murali **-** iNoCs/EPFL, Switzerland

Panelists: ***Ruchir Puri*** **-** IBM, U.S.A.
Paull Marchal **-** IMEC, Belgium
Yuan Xie **-** Pennsylvania State Univ.,U.S.A.
Ahmed Jerraya **-** LETI, France
Nobuaki Miyakawa **-** Honda Research, Japan

Wednesday, January 20, 8:30 - 10:10

Wednesday, January 20, 8:30 - 10:10 Room 101A
Session 3A: Emerging Memories and 3D ICs

Chairs: ***Mehdi Baradaran Tahoori*** **-** Northeastern Univ., U.S.A.
Chin-Long Wey **-** National Central Univ., Taiwan

3A-1 Three Dimensional Integrated Circuit (3D IC) Floorplan and Power/Ground Network Cosynthesis
Paul Falkerstern, Yuan Xie (Pennsylvania State Univ., U.S.A.), Yao-wen Chang (National Taiwan Univ., Taiwan), Yu Wang (Tsinghua Univ., China)

3A-2 Power and Slew-aware Clock Network Design for Through-Silicon-Via (TSV) Based 3D ICs
Xin Zhao, Sung Kyu Lim (Georgia Tech, U.S.A.)

3A-3 A Novel Si-Tunnel FET based SRAM Design for Ultra Low-Power 0.3V V_{DD} Applications
Jawar Singh (Univ. of Bristol, U.K.), Ramakrishnan Krishnan, Saurabh Mookerjea, Suman Datta, Vijaykrishnan Narayanan (Pennsylvania State Univ., U.S.A.), Dhiraj Pradhan (Univ. of Bristol, U.K.)

3A-4s CAD Reference Flow for 3D Via-Last Integrated Circuits
Chang-Tzu Lin, Ding-Ming Kwai, Yung-Fa Chou, Ting-Sheng Chen, Wen-Ching Wu (ITRI, Taiwan)

3A-5s Energy and Performance Driven Circuit Design for Emerging Phase-Change Memory
Dimin Niu, Yibo Chen, Xiangyu Dong, Yuan Xie (Pennsylvania State Univ., U.S.A.)

Wednesday, January 20, 8:30 - 10:10 Room 101B
Session 3B: Macromodeling and Verification of Analog Systems

Chairs: ***Chin-Fong Chiu-*** National Chip Implementation Center, Taiwan
Eric Keiter- Sandia National Labs, U.S.A.

3B-1 Current Source Modeling in the Presence of Body Bias
Saket Gupta, Sachin S. Sapatnekar (Univ. of Minnesota, U.S.A.)

3B-2 Manifold Construction and Parameterization for Nonlinear Manifold-Based Model Reduction
Chenjie Gu, Jaijeet Roychowdhury (Univ. of California, Berkeley, U.S.A.)

3B-3 A Fast Analog Mismatch Analysis by an Incremental and Stochastic Trajectory Piecewise Linear Macromodel
Hao Yu (Berkeley Design Automation, U.S.A.), Xuexin Liu, Hai Wang, Sheldon Tan (UC Riverside, U.S.A.)

3B-4 Formal Verification of Tunnel Diode Oscillator with Temperature Variations
Kusum Lata, Jamadagni H S (CEDT,Indian Institute of Science, Bangalore, India)

Wednesday, January 20, 8:30 - 10:10 Room 101C
Session 3C: System-level Modeling and Analysis

Chairs: ***Soonhoi Ha*** **-** Seoul National Univ., Republic of Korea
Nagisa Ishiura **-** Kwansei Gakuin Univ., Japan

3C-1 Constrained Global Scheduling of Streaming Applications on MPSoCs
Jun Zhu, Ingo Sander, Axel Jantsch (Royal Inst. of Tech., Sweden)

3C-2 Analyzing Impact of Multiple ABB and AVS Domains on Throughput of Power and Thermal Constrained Multi-Core Processors
Jungseob Lee, Shi-Ting Zhou, Nam Sung Kim (Univ. of Wisconsin - Madison, U.S.A.)

3C-3 Source-Level Timing Annotation for Fast and Accurate TLM Computation Model Generation
Kai-Li Lin, Chen-Kang Lo, Ren-Song Tsay (National Tsing Hua Univ., Taiwan)

3C-4 Improved On-Chip Router Analytical Power and Area Modeling
Andrew B. Kahng, Bill Lin, Kambiz Samadi (UC San Diego, U.S.A.)

Wednesday, January 20, 8:30 - 10:10 Room 101D
Session 3D: Special Session: Recent Advancement in Post-silicon Validation

Chair: ***Ing-Jer Huang*** **-** National Sun Yat-Sen Univ.,Taiwan

3D-1 Data Learning Based Diagnosis
Li-C. Wang (Univ. of California, Santa Barbara, U.S.A.)

3D-2 Using Introspective Software-based Testing for Post-silicon Debug and Repair
Todd Austin (Univ. of Michigan, U.S.A.)

3D-3 Post-silicon Debugging for Multi-core Designs
Valeria Bertacco (Univ. of Michigan, U.S.A.)

3D-4 Low-cost Repair Techniques by Using Partitioning
Kyungho Kim, Byungtae Kang, Dongyun Kim (Samsung Electronics Co., Republic of Korea), Sungchul Lee, Juyong Shin, Hyunchul Shin (Hanyang Univ., Republic of Korea)

3D-5 On Signal Tracing in Post-silicon Validation
Qiang Xu, Xiao Liu (Chinese Univ. of Hong Kong, Hong Kong)

Wednesday, January 20, 10:30 - 12:10

Wednesday, January 20, 10:30 - 12:10 Room 101A
Session 4A: New Techniques for Beyond-die Routing

Chairs: ***Yasuhiro Takashima*** **-** Univ. of Kitakyushu, Japan
Yih-Lang Li **-** National Chiao Tung Univ., Taiwan

4A-1 CrossRouter: A Droplet Router for Cross-Referencing Digital Microfluidic Biochips
Zigang Xiao, Evangeline F.Y. Young (Chinese Univ. of Hong Kong, Hong Kong)

4A-2 Optimal Simultaneous Pin Assignment and Escape Routing for Dense PCBs
Hui Kong, Tan Yan, Martin D.F Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.)

4A-3 CAFE router: A Fast Connectivity Aware Multiple Nets Routing Algorithm for Routing Grid with Obstacles
Yukihide Kohira (Univ. of Aizu, Japan), Atsushi Takahashi (Osaka Univ., Japan)

4A-4 Obstacle-Aware Longest Path using Rectangular Pattern Detouring in Routing Grids
Jin-Tai Yan, Ming-Ching Jhong, Zhi-Wei Chen (Chung Hua Univ., Taiwan)

Wednesday, January 20, 10:30 - 12:10 Room 101B
Session 4B: Analog Layout and Testing

Chairs: ***Sachin Sapatnkar*** **-** Univ. of Minnesota, U.S.A.
Jeong-Tyng Li **-** SpringSoft, U.S.A.

4B-1 A Performance-Constrained Template-Based Layout Retargeting Algorithm for Analog Integrated Circuits
Zheng Liu, Lihong Zhang (Memorial Univ. of Newfoundland, Canada)

4B-2 Symmetry-Aware TCG-Based Placement Design under Complex Multi-Group Constraints for Analog Circuit Layouts
Rui He, Lihong Zhang (Memorial Univ. of Newfoundland, Canada)

4B-3 Regularity-Oriented Analog Placement with Diffusion Sharing and Well Island Generation
Shigetoshi Nakatake (Univ. of Kitakyushu, Japan), Masahiro Kawakita, Takao Ito (Toshiba Corp., Japan), Masahiro Kojima, Michiko Kojima, Kenji Izumi, Tadayuki Habasaki (NEC, Japan)

4B-4 A Novel Characterization Technique for High Speed I/O Mixed Signal Circuit Components Using Random Jitter Injection
Ji Hwan (Paul) Chun (Intel Corp., U.S.A.), Jae Wook Lee, Jacob A. Abraham (Univ. of Texas, Austin,U.S.A.)

Wednesday, January 20, 10:30 - 12:10 Room 101C
Session 4C: New Techniques in Technology Mapping

Chairs: ***Ting-Ting Hwang*** **-** National Tsing Hua Univ.,Taiwan
Yuchun Ma **-** Tsinghua Univ., China

4C-1 Technology Mapping with Crosstalk Noise Avoidance
Fang-Yu Fan (TSMC, Taiwan), Hung-Ming Chen (NCTU, Taiwan), I-Min Liu (Atoptech, U.S.A.)

4C-2 Fault-Tolerant Resynthesis with Dual-Output LUTs
Ju-Yueh Lee (UCLA, U.S.A.), Yu Hu (Univ. of Alberta, Canada), Rupak Majumdar, Lei He (UCLA, U.S.A.), Minming Li (City Univ. of Hong Kong, Hong Kong)

4C-3 TRECO: Dynamic Technology Remapping for Timing Engineering Change Orders
Kuan-Hsien Ho, Jie-Hong Roland Jiang, Yao-Wen Chang (National Taiwan Univ., Taiwan)

4C-4 Multi-Operand Adder Synthesis on FPGAs Using Generalized Parallel Counters
Taeko Matsunaga, Shinji Kimura (Waseda Univ., Japan), Yusuke Matsunaga (Kyushu Univ., Japan)

Wednesday, January 20, 10:30 - 12:10 Room 101D
Session 4D: University LSI Design Contest

Organizer: ***Jiun-In Guo*** - National Chung Cheng Univ., Taiwan
Masanori Hariyama - Tohoku Univ., Japan

4D-1 Checker-Pattern and Shared Two Pixels LOFIC CMOS Image Sensors
Yoshiaki Tashiro, Shun Kawada, Shin Sakai, Shigetoshi Sugawa (Tohoku Univ., Japan)

4D-2 A CMOS Image Sensor With 2.0-e- Random Noise and 110-ke- Full Well Capacity Using Column Source Follower Readout Circuits
Takahiro Kohara, Wonghee Lee (Tohoku Univ., Japan), Koichi Mizobuchi (Texas Instruments Japan, Japan), Shigetoshi Sugawa (Tohoku Univ., Japan)

4D-3 Checkered White-RGB Color LOFIC CMOS Image Sensor
Shun Kawada, Shin Sakai, Yoshiaki Tashiro, Shigetoshi Sugawa (Tohoku Univ., Japan)

4D-4 A Versatile Recognition Processor for Sensor Network Applications
Risako Takashima, Hanai Yuya, Yuichi Hori, Tadahiro Kuroda (Keio Univ., Japan)

4D-5 A 2-6 GHz Fully Integradted Tunable CMOS Power Amplifier for Multi-Standard Transmitters
Daisuke Imanishi, JeeYoung Hong, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan)

4D-6 An Embedded Debugging/Performance Monitoring Engine for a Tile-based 3D Graphics SoC Development
Liang-Bi Chen, Tsung-Yu Ho, Jiun-Cheng Ju, Cheng-Lung Chiang, Chung-Nan Lee, Ing-Jer Huang (National Sun Yat-Sen Univ., Taiwan)

4D-7 Cascaded Time Difference Amplifier using Differential Logic Delay Cell
Shingo Mandai, Toru Nakura, Makoto Ikeda, Kunihiro Asada (Univ. of Tokyo, Japan)

4D-8 Built-in Self At-Speed Delay Binning and Calibration Mechanism in Wireless Test Platform
Chen-I Chung, Jyun-Sian Jhou, Ching-Hwa Cheng (Feng Chia Univ., Taiwan)

4D-9 Dynamic Voltage Domain Assignment Technique for Low Power Performance Manageable Cell Based Design
Elone Lee, Feng-Tso Chien, Ching Hwa Cheng (Feng Chia Univ., Taiwan), Jiun-In Guo (National Chung Cheng Univ., Taiwan)

4D-10 Adaptive Performance Control with Embedded Timing Error Predictive Sensors for Subthreshold Circuits
Hiroshi Fuketa, Masanori Hashimoto, Yukio Mitsuyama, Takao Onoye (Osaka Univ., Japan)

4D-12 A 60GHz Direct-Conversion Transmitter in 65nm CMOS Technology
Naoki Takayama, Kouta Matsushita, Shogo Ito, Ning Li, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan)

4D-13 An Electrically Adjustable 3-Terminal Regulator with Post-Fabrication Level-Trimming Function
Hiroyuki Morimoto, Hiroki Koike, Kazuyuki Nakamura (Kyushu Inst. of Tech., Japan)

4D-14 Fine Resolution Double Edge Clipping with Calibration Technique for Built-In At-Speed Delay Testing
Chen-I Chung, Shuo-Wen Chang, Feng-Tso Chien, Ching Hwa Cheng (Feng Chia Univ., Taiwan)

4D-15 Geyser-1: A MIPS R3000 CPU core with finegrained run-time Power Gating
Diasuke Ikebuchi, Naomi Seki, Yuu Kojima, Masahiro Kamata, Zhao Lei, Hideharu Amano (Keio Univ., Japan), Toshiki Shirai, Satoshi Koyama, Tatsunori Hashida, Yusuke Umahashi, Hiroki Masuda, Kimiyoshi Usami (Shibaura Inst. of Tech., Japan), Seidai Takeda, Hiroshi Nakamura (Univ. of Tokyo, Japan), Mitaro Namiki (Univ. of Agri. and Tech., Japan), Masaaki Kondo (Univ. of Electro-Communications, Japan)

4D-16 A WiMAX Turbo Decoder with Tailbiting BIP Architecture
Hiroaki Arai, Naoto Miyamoto, Koji Kotani (Tohoku Univ., Japan), Hisanori Fujisawa (Fujitsu Laboratories Ltd., Japan), Takashi Ito (Tohoku Univ., Japan)

4D-17 Temporal Circuit Partitioning for a 90nm CMOS Multi-Context FPGA and its Delay Measurement
Naoto Miyamoto, Tadahiro Ohmi (Tohoku Univ., Japan)

4D-18 Design and Chip Implementation of an Instruction Scheduling Free Ubiquitous Processor
Masa-aki Fukase, Ryosuke Murakami, Tomoaki Sato (Hirosaki Univ., Japan)

4D-19 MUCCRA-3: A Low Power Dynamically Reconfigurable Processor Array
Yoshiki Saito, Toru Sano, Masaru Kato, Vasutan Tunbunheng, Yoshihiro Yasuda, Masayuki Kimura, Hideharu Amano (Keio Univ., Japan)

4D-20 Rapid Prototyping on a Structured ASIC Fabric
Steve C.L. Yuen, Yan-Qing Ai, Brian P.W. Chan, Thomas C.P. Chau, Sam M.H. Ho, Oscar K.L. Lau, Kong-Pang Pun (Chinese Univ. of Hong Kong, Hong Kong), Philip H.W. Leong (Univ. of Sydney, Australia), Oliver C.S. Choy (Chinese Univ. of Hong Kong, Hong Kong)

4D-21 A High Performance Low Complexity Joint Transceiver for Closed-Loop MIMO Applications
Jian-Lung Tzeng, Chien-Jen Huang, Yu-Han Yuan, Hsi-Pin Ma (National Tsing Hua Univ., Taiwan)

Wednesday, January 20, 13:30 - 15:10

Wednesday, January 20, 13:30 - 15:10 Room 101A
Session 5A: Clock Network Analysis and Optimization

Chairs: ***Kimihiro Ogawa*** - STARC/Sony, Japan
Rachid Salik - Cadence Design Systems Inc.,U.S.A.

5A-1 A Fast Symbolic Computation Approach to Statistical Analysis of Mesh Networks with Multiple Sources
Zhigang Hao, Guoyong Shi (Shanghai Jiaotong Univ., China)

5A-2 Minimizing Clock Latency Range in Robust Clock Tree Synthesis
Wen-Hao Liu, Yih-Lang Li, Hui-chi Chen (National Chiao Tung Univ., Taiwan)

5A-3 Blockage-Avoiding Buffered Clock-Tree Synthesis for Clock Latency-Range and Skew Minimization
Xin-Wei Shih, Chung-Chun Cheng, Yuan-Kai Ho, Yao-Wen Chang (National Taiwan Univ., Taiwan)

5A-4 Improved Clock-Gating Control Scheme for Transparent Pipeline
Jung Hwan Choi (Samsung Electronics, Republic of Korea), Byung Guk Kim (Purdue Univ., U.S.A.), Aurobindo Dasgupta (Intel Corp., U.S.A.), Kaushik Roy (Purdue Univ., U.S.A.)

Wednesday, January 20, 13:30 - 15:10 Room 101B
Session 5B: Test Solutions for Emerging Applications

Chairs: ***Wu-Tung Cheng*** - Mentor Graphics, U.S.A.
Ming-Der Shieh - National Cheng Kung Univ., Taiwan

5B-1 Scan-Based Attack against Elliptic Curve Cryptosystems
Ryuta Nara, Nozomu Togawa, Masao Yanagisawa, Tatsuo Ohtsuki (Waseda Univ., Japan)

5B-2 Secure and Testable Scan Design Using Extended de Bruijn Graphs
Hideo Fujiwara, Marie Engelene J. Obien (NAIST, Japan)

5B-3 Correlating System Test Fmax with Structural Test Fmax and Process Monitoring Measurements
Chia-Ying (Janine) Chen (Univ. of California, Santa Barbara, U.S.A.), Jing Zeng (Advanced Micro Devices, Inc, U.S.A.), Li-C Wang (Univ. of California, Santa Barbara, U.S.A.), Michael Mateja (Advanced Micro Devices, Inc, U.S.A.)

5B-4 Guided Gate-level ATPG for Sequential Circuits using a High-level Test Generation Approach
Bijan Alizadeh, Masahiro Fujita (Univ. of Tokyo, Japan)

Wednesday, January 20, 13:30 - 15:10 Room 101C
Session 5C: Power, Performance and Reliability in SoC Design

Chairs: ***Yoshinori Takeuchi*** - Osaka Univ., Japan

5C-1 Optimizing Power and Performance for Reliable On-Chip Networks
Aditya Yanamandra, Soumya Eachempati, Niranjan Soundararajan, Vijaykrishnan Narayanan, Mary Jane Irwin, Ramakrishnan Krishnan (Pennsylvania State Univ., U.S.A.)

5C-2 A Low Latency Wormhole Router for Asynchronous On-chip Networks
Wei Song, Doug Edwards (Univ. of Manchester, U.K.)

5C-3 Combined Use of Rising and Falling Edge Triggered Clocks for Peak Current Reduction in IP-Based SoC Designs
Tsung-Yi Wu (National Changhua Univ. of Education, Taiwan), How-Rern Lin (Providence Univ., Taiwan), Tzi-Wei Kao, Shi-Yi Huang, Tai-Lun Li (National Changhua Univ. of Education, Taiwan)

5C-4 Workload Capacity Considering NBTI Degradation in Multi-core Systems
Jin Sun, Roman Lysecky, Karthik Shankar (Univ. of Arizona, U.S.A.), Avinash Kodi (Ohio Univ., U.S.A.), Ahmed Louri, Janet M. Wang (Univ. of Arizona, U.S.A.)

Wednesday, January 20, 13:30 - 15:10 Room 101D
Session 5D: Designers' Forum: State-of-the-art SoCs

Chairs: ***Kunio Uchiyama*** - Hitachi, Japan
Ing-Jer Huang - National Sun Yat-Sen Univ., Taiwan

5D-1 Overview of ITRI's Parallel Architecture Core (PAC) DSP Project: from VLIW DSP Processor to Android ready Multicore Computing Platform
An-Yeu (Andy) Wu (ITRI, Taiwan)

5D-2 Design and Verification Methods of Toshiba's Wireless LAN Baseband SoC
Masanori Kuwahara (Toshiba, Japan)

5D-3 Programmable Platform for Multimedia SoC
Bor-Sung Liang (Sunplus Core Technology, Taiwan)

5D-4 SoC for Car Navigation Systems with a 53.3 GOPS Image Recognition Engine
Hiroyuki Hamasaki (Renesas Technology, Japan)

Wednesday, January 20, 15:30 - 17:10

Wednesday, January 20, 15:30 - 17:10 Room 101A
Session 6A: Advances in Modern Clock Tree Routing

Chairs: ***Martin D. F. Wong*** - Univ. of Illinois, Urbana-Champaign, U.S.A.
Tsung-Yi Ho - National Cheng Kung Univ., Taiwan

6A-1 A Dual-MST Approach for Clock Network Synthesis
Jingwei Lu, Wing-Kai Chow, Chiu-Wing Sham (Hong Kong Polytechnic Univ., Hong Kong), Fung-Yu Young (Chinese Univ. of Hong Kong, Hong Kong)

6A-2 Buffered Clock Tree Sizing for Skew Minimization Under Power and Thermal Budgets
Krit Athikulwongse, Xin Zhao, Sung Kyu Lim (Georgia Tech, U.S.A.)

6A-3 Critical-PMOS-Aware Clock Tree Design Methodology for Anti-Aging Zero Skew Clock Gating
Shih-Hsu Huang, Chia-Ming Chang, Wen-Pin Tu, Song-Bin Pan (Chung Yuan Christian Univ., Taiwan)

6A-4 Clock Tree Embedding for 3D ICs
Tak-Yung Kim, Taewhan Kim (Seoul National Univ., Republic of Korea)

Wednesday, January 20, 15:30 - 17:10 Room 101B
Session 6B: Timing-related Testing and Diagnosis

Chairs: ***Shi-Yu Huang*** - National Tsing Hua Univ., Taiwan
Hideo Fujiwara - NAIST, Japan

6B-1 Improved Weight Assignment for Logic Switching Activity During At-Speed Test Pattern Generation
Meng-Fan Wu, Hsin-Chieh Pan, Teng-Han Wang, Jiun-Lang Huang (National Taiwan Univ., Taiwan), Kun-Han Tsai, Wu-Tung Cheng (Mentor Graphics Corp., U.S.A.)

6B-2 Graph Partition Based Path Selection for Testing of Small Delay Defects
Zijian He, Tao Lv, Huawei Li, Xiaowei Li (Institute of Computing Technology, CAS, China)

6B-3 Functional and Partially-Functional Skewed-Load Tests
Irith Pomeranz (Purdue Univ., U.S.A.), Sudhakar M. Reddy (Univ. of Iowa, U.S.A.)

6B-4 Emulating and Diagnosing IR-drop by Using Dynamic SDF
Ke Peng (Univ. of Connecticut, U.S.A.), Yu Huang, Ruifeng Guo, Wu-Tung Cheng (Mentor Graphics, U.S.A.), Mohammad Tehranipoor (Univ. of Connecticut,U.S.A.)

Wednesday, January 20, 15:30 - 17:10 Room 101C
Session 6C: Application-specific NoC Design

Chairs: ***Michihiro Koibuchi*** - NII, Japan
Samar Abdi - Concordia Univ., Canada

6C-1 Application-Specific 3D Network-on-Chip Design Using Simulated Allocation
Pingqiang Zhou (Univ. of Minnesota, U.S.A.), Ping-Hung Yuh (National Taiwan Univ., Taiwan), Sachin S. Sapatnekar (Univ. of Minnesota, U.S.A.)

6C-2 A3MAP: Architecture-Aware Analytic Mapping for Networks-on-Chip
Wooyoung Jang, David Z. Pan (Univ. of Texas, Austin, U.S.A.)

6C-3 Efficient Throughput-Guarantees for Latency-Sensitive Networks-On-Chip
Jonas Diemer, Rolf Ernst (Institute of Computer and Network Engineering, TU Braunschweig, Germany), Michael Kauschke (Intel, Germany)

6C-4 Floorplanning and Topology Generation for Application-Specific Network-on-Chip
Bei Yu, Sheqin Dong (Tsinghua Univ., China), Song Chen, Satoshi Goto (Waseda Univ., Japan)

Wednesday, January 20, 15:30 - 17:10 Room 101D
Session 6D: Designers' Forum: Is 3D Integration an Opportunity or Just a Hype?

Chairs: ***Cheng-Wen Wu*** - National Tsing Hua Univ./ITRI, Taiwan
Jin-Fu Li - National Central Univ./ITRI, Taiwan

6D-1 Tutorial: Is 3D Integration an Opportunity or Just a Hype?
Jin-Fu Li (National Central Univ./ITRI, Taiwan)

6D-2 Panel Discussion: Is 3D Integration an Opportunity or Just a Hype?

Organizers & Moderators: **Cheng-Wen Wu** - National Tsing Hua Univ./ITRI, Taiwan
Jin-Fu Li - National Central Univ./ITRI, Taiwan

Panelists: **Albert Li** (GUC, Taiwan)
Erik Jan Marinissen (IMEC, Belgium)
Ding-Ming Kwai, (ITRI, Taiwan)
Kyu-Myung Choi (Samsung, Republic of Korea)
Makoto Takahashi (Toshiba, Japan)

Thursday, January 21, 8:30 - 10:10

Thursday, January 21, 8:30 - 10:10 Room 101A
Session 7A: Modern Floorplanning and Placement Techniques

Chairs: ***David Pan*** - Univ. of Texas, Austin, U.S.A.
Hung-Ming Chen - National Chiao Tung Univ., Taiwan

7A-1 Configurable Multi-product Floorplanning
Qiang Ma, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.), Kai-Yuan Chao (Intel Corp., U.S.A.)

7A-2 UFO: Unified Convex Optimization Algorithms for Fixed-Outline Floorplanning
Jai-Ming Lin, Hsi Hung (National Cheng Kung Univ., Taiwan)

7A-3 Fixed-outline Thermal-aware 3D Floorplanning
Linfu Xiao (Chinese Univ. of Hong Kong, Hong Kong), Subarna Sinha (Synopsys, U.S.A.), Jingyu Xu (Synopsys, China), Evangeline F.Y. Young (Chinese Univ. of Hong Kong, Hong Kong)

7A-4 A Hierarchical Bin-Based Legalizer for Standard-Cell Designs with Minimal Disturbance
Yu-Min Lee, Tsung-You Wu, Po-Yi Chiang (National Chiao Tung Univ., Taiwan)

Thursday, January 21, 8:30 - 10:10 Room 101B
Session 7B: Power Optimization and Estimation in the DSM Era

Chairs: ***Kimiyoshi Usami*** - Shibaura Inst. of Tech., Japan
Masanori Hashimoto - Osaka Univ., Japan

7B-1 An Analytical Dynamic Scaling of Supply Voltage and Body Bias Exploiting Memory Stall Time Variation

Jungsoo Kim, Younghoon Lee (KAIST, Republic of Korea), Sungjoo Yoo (POSTECH, Republic of Korea), Chong-Min Kyung (KAIST, Republic of Korea)

7B-2 Bounded Potential Slack: Enabling Time Budgeting for Dual-Vt Allocation of Hierarchical Design
Jun Seomun, Seungwhun Paik, Youngsoo Shin (KAIST, Republic of Korea)

7B-3 Dynamic Power Estimation for Deep Submicron Circuits with Process Variation
Quang Dinh, Deming Chen, Martin Wong (UIUC,U.S.A.)

7B-4 Runtime Temperature-Based Power Estimation for Optimizing Throughput of Thermal-Constrained Multi-Core Processors
Dongkeun Oh, Nam Sung Kim, Yu Hen Hu (Univ. of Wisconsin, U.S.A.), Charlie Chung Ping Chen (National Taiwan Univ., Taiwan), Azadeh Davoodi (Univ. of Wisconsin, U.S.A.)

Thursday, January 21, 8:30 - 10:10 Room 101C
Session 7C: Design Verification and Debugging

Chairs: ***Yirng-An Chen*** - Marvell Corp., U.S.A.
Jie-Hong (Roland) Jiang - National Taiwan Univ., Taiwan

7C-1 Managing Verification Error Traces with Bounded Model Debugging
Sean Safarpour (Vennsa Technologies, Canada), Andreas Veneris, Farid Najm (Univ. of Toronto, Canada)

7C-2 Automatic Assertion Extraction via Sequential Data Mining of Simulation Traces
Po-Hsien Chang, Li.-C Wang (Univ. of California, Santa Barbara, U.S.A.)

7C-3 Automatic Constraint Generation for Guided Random Simulation
Hu-Hsi Yeh, Chung-Yang(Ric) Huang (National Taiwan Univ., Taiwan)

7C-4 A Method for Debugging of Pipelined Processors in Formal Verification by Correspondence Checking
Miroslav Velev, Ping Gao (Aries Design Automation, U.S.A.)

Thursday, January 21, 8:30 - 10:10 Room 101D

Session 7D: Special Session: Dependable Silicon Design with Unreliable Components

Organizer & Moderator: ***Vincent Mooney*** -Georgia Tech/ Nanyang Technological Univ., U.S.A.

7D-1 Resilient Design in Scaled CMOS for Energy Efficiency
James Tschanz, Keith Bowman, Muhammad Khellah, Chris Wilkerson, Bibiche Geuskens, Dinesh Somasekhar, Arijit Raychowdhury, Jaydeep Kulkarni, Carlos Tokunaga, Shih-Lien Lu, Tanay Karnik, Vivek K. De (Intel Corp., U.S.A.)

7D-2 Benefits and Barriers to Probabilistic Design
Siva Narendra (Tyfone, Inc., U.S.A.)

7D-3 A Probabilistic Boolean Logic for Energy Efficient Circuit and System Design
Lakshmi N. B. Chakrapani (Rice Univ., U.S.A.), Krishna Palem (Rice Univ./Nanyang Technological Univ., U.S.A.)

7D-4 Panel Discussion: Dependable Silicon Design with Unreliable Components
Organizer & Moderator: **Vincent Mooney** - Georgia Tech/ Nanyang Technological Univ., U.S.A.
Panelists: **Vivek K. De** (Intel Corp., U.S.A.)
Siva Narendra (Tyfone, Inc., U.S.A.)
Krishna Palem (Rice Univ./ Nanyang Technological Univ., U.S.A.)

Thursday, January 21, 10:30 - 12:10

Thursday, January 21, 10:30 - 12:10 Room 101A

Session 8A: DFM1: Patterning and Physical Design

Chairs: ***Fedor G. Pikus*** - Mentor Graphics Corp., U.S.A.
Masanori Hashimoto - Osaka Univ., Japan

8A-1 A Multi-Objective Min-Cut Based Layout Decomposition Framework for Double Patterning Lithography
Jae-Seok Yang (Univ. of Texas, Austin, U.S.A.), Katrina Lu (Intel, U.S.A.), MinSik Cho (IBM Research, U.S.A.), Kun Yuan, David Z. Pan (Univ. of Texas, Austin, U.S.A.)

8A-2 A Robust Pixel-Based RET Optimization Algorithm Independent of Initial Conditions
Jinyu Zhang (Tsinghua Univ., China), Min-Chun Tsai (Brion Technology, U.S.A.), Wei Xiong, Yan Wang, Zhiping Yu (Tsinghua Univ., China)

8A-3 A New Method to Improve Accuracy of Parasitics Extraction Considering Sub-wavelength Lithography Effects
Kuen-Yu Tsai, Wei-Jhih Hsieh, Yuan-Ching Lu, Bo-Sen Chang, Sheng-Wei Chien, Yi-Chang Lu (National Taiwan Univ., Taiwan)

8A-4 Dead Via Minimization by Simultaneous Routing and Redundant Via Insertion
Chih-Ta Lin, Yen-Hung Lin, Guan-Chan Su, Yih-Lang Li (National Chiao Tung Univ., Taiwan)

Thursday, January 21, 10:30 - 12:10 Room 101B

Session 8B: Design and Verification for Process Variation Issues

Chairs: ***Shih-Hsu Huang*** - Chung Yuan Christian Univ., Taiwan
Atsushi Takahashi - Osaka Univ., Japan

8B-1 Statistical Timing Verification for Transparently Latched Circuits through Structural Graph Traversal
Xingliang Yuan, Jia Wang (Illinois Inst. of Tech., U.S.A.)

8B-2 A Unified Multi-Corner Multi-Mode Static Timing Analysis Engine
Jing Jia Nian, Shih Heng Tsai, Chung Yang (Ric) Huang (National Taiwan Univ., Taiwan)

8B-3 Statistical Time Borrowing for Pulsed-Latch Circuit Designs
Seungwhun Paik, Lee-eun Yu, Youngsoo Shin (KAIST, Republic of Korea)

8B-4 Design Time Body Bias Selection for Parametric Yield Improvement
Cheng Zhuo, Yung-Hsu Chang, Dennis Sylvester, David Blaauw (Univ. of Michigan, Ann Arbor, U.S.A.)

Thursday, January 21, 10:30 - 12:10 Room 101C

Session 8C: New Advances in High-level Synthesis

Chairs: ***Taewhan Kim*** - Seoul National Univ., Republic of Korea
Yusuke Matsunaga - Kyushu Univ., Japan

8C-1 Minimizing Leakage Power in Aging-Bounded High-level Synthesis with Design Time Multi-Vth Assignment
Yibo Chen (Penn State Univ., U.S.A.), Yu Wang (Tsinghua Univ., China), Yuan Xie (Penn State Univ.,U.S.A.), Andres Takach (Mentor Graphics Corp.,U.S.A.)

8C-2 A Global Interconnect Reduction Technique during High Level Synthesis
Taemin Kim (Univ. of California, Los Angeles, U.S.A.), Xun Liu (North Carolina State Univ., U.S.A.)

8C-3 Incremental High-Level Synthesis
Luciano Lavagno (Cadence Design Systems, U.S.A.), Mototsugu Fujii (Renesas Technology Corp., Japan), Alex Kondratyev (Cadence Design Systems, U.S.A.), Noriyasu Nakayama (Fujitsu Advanced Technologies, Japan), Mitsuru Tatesawa (Renesas Technology Corp., Japan), Yosinori Watanabe (Cadence Design Systems, U.S.A.), Qiang Zhu (Cadence Design Systems, Japan)

8C-4 A High-Level Synthesis Flow for Custom Instruction Set Extensions for Application-Specific Processors
Nagaraju Pothineni (Google, India, India), Philip Brisk, Paolo Ienne (EPFL, Switzerland), Anshul Kumar, Kolin Paul (Indian Inst. of Tech., Delhi, India)

Thursday, January 21, 10:30 - 12:10 Room 101D

Session 8D: Special Session: ESL: Analysis and Synthesis of Multi-core Systems

Organizer & Chair: ***Daniel D. Gajski*** - Univ. of California,Irvine, U.S.A.

8D-1 Computer-aided Recoding for Multi-core Systems
Rainer Doemer (Univ. of California, Irvine, U.S.A.)

8D-2 TLM Automation for Multi-core Design
Samar Abdi (Concordia Univ., Canada)

8D-3 Platform Modeling for Exploration and Synthesis
Andreas Gerstlauer (Univ. of Texas, Austin, U.S.A.), Gunar Schirner (Northeastern Univ., Boston, U.S.A.)

8D-4 Application of ESL Synthesis on GSM Edge Algorithm for Base Station
Alan Su (Global Unichip, Taiwan)

Thursday, January 21, 13:30 - 15:10

Thursday, January 21, 13:30 - 15:10 Room 101A
Session 9A: DFM2: Variation Modeling

Chairs: ***Keh-Jeng Chang*** - National Tsing Hua Univ., Taiwan
Jing-Jou Tang - Southern Taiwan Univ., Taiwan

9A-1 Analyzing Electrical Effects of RTA-driven Local Anneal Temperature Variation
Vivek Joshi (Univ. of Michigan, U.S.A.), Kanak Agarwal (IBM, U.S.A.), Dennis Sylvester, David Blaauw (Univ. of Michigan, U.S.A.)

9A-2 Physical Design Techniques for Optimizing RTA-induced Variations
Yaoguang Wei (Univ. of Minnesota, U.S.A.), Jiang Hu (Texas A&M Univ., U.S.A.), Frank Liu (IBM, U.S.A.), Sachin Sapatnekar (Univ. of Minnesota, U.S.A.)

9A-3 On Confidence in Characterization and Application of Variation Models
Lerong Cheng, Puneet Gupta, Lei He (UCLA, U.S.A.)

Thursday, January 21, 13:30 - 15:10 Room 101B
Session 9B: Power Grid Analysis

Chairs: ***Youngsoo Shin*** - KAIST, Republic of Korea
Nam Sung Kim - Univ. of Wisconsin-Madison, U.S.A.

9B-1 Incremental Solution of Power Grids using Random Walks
Baktash Boghrati, Sachin S. Sapatnekar (Univ. of Minnesota, U.S.A.)

9B-2 Efficient Power Grid Integrity Analysis Using On-the-Fly Error Check and Reduction
Duo Li, Sheldon Tan, Ning Mi (Univ. of California, Riverside, U.S.A.), Yici Cai (Tsinghua Univ., China)

9B-3 PS-FPG: Pattern Selection based co-design of Floorplan and Power/Ground Network with Wiring Resource Optimization
Li Li (WuHan Univ. of Tech., China), Yuchun Ma (Tsinghua Univ., China), Ning Xu (WuHan Univ. of Tech., China), Yu Wang, Xianlong Hong (Tsinghua Univ., China)

9B-4 Gate Delay Estimation in STA under Dynamic Power Supply Noise
Takaaki Okumura, Fumihiro Minami, Kenji Shimazaki,

Kimihiko Kuwada (STARC, Japan), Masanori Hashimoto (Osaka Univ., Japan)

Thursday, January 21, 13:30 - 15:10 Room 101C
Session 9C: High-level Synthesis and Optimization for Performance and Power

Chairs: ***Lih-Yih Chiou*** - National Cheng Kung Univ., Taiwan
Jen-Chieh Yeh - ITRI, Taiwan

9C-1 Parametric Yield Driven Resource Binding in Behavioral Synthesis with Multi-Vth/Vdd Library
Yibo Chen (Penn State Univ., U.S.A.), Yu Wang (Tsinghua Univ., China), Yuan Xie (Penn State Univ., U.S.A.), Andres Takach (Mentor Graphics Corp., U.S.A.)

9C-2 Optimizing Blocks in an SoC Using Symbolic Code-Statement Reachability Analysis
Hong-Zu Chou (National Taiwan Univ., Taiwan), Kai-Hui Chang (Avery Design Systems, U.S.A.), Sy-Yen Kuo (National Taiwan Univ., Taiwan)

9C-3 High Level Event Driven Thermal Estimation for Thermal Aware Task Allocation and Scheduling
Jin Cui, Douglas L. Maskell (Nanyang Technological Univ., Singapore)

9C-4 Mapping and Scheduling of Parallel C Applications with Ant Colony Optimization onto Heterogeneous Reconfigurable MPSoCs
Fabrizio Ferrandi, Christian Pilato, Donatella Sciuto, Antonino Tumeo (Politecnico di Milano, Italy)

Thursday, January 21, 13:30 - 15:10 Room 101D
Session 9D: Designers' Forum: ESL, The Road to Glory, Or Is It Not? Real Stories about Using ESL Design Methodology in Product Development

Chairs: ***Alan P. Su*** - Global Unichip Corp., Taiwan
Ing-Jer Huang - National Sun Yat-Sen Univ., Taiwan

9D-1 Possibility of ESL- A Software Centric System Design for Multicore SoC in the Upstream Phase
Koichiro Yamashita (Fujitsu Laboratories Ltd., Japan)

9D-2 Design of Complex Image Processing Systems in ESL
Benjamin Carrion Schafer (NEC Corp., Japan), Ashish

Trambadia (NEC, Japan), Kazutoshi Wakabayashi (NEC Corp., Japan)
Speaker: Kazutoshi Wakabayashi

9D-3 PAC Duo System Power Estimation at ESL
Wen-Tsan Hsieh, Jen-Chieh Yeh, Shi-Yu Huang (ITRI/ National Tsing Hua Univ., Taiwan)

9D-4 A Practice of ESL Verification Methodology from SystemC to FPGA -Using EPC Class-1 Generation-2 RFID Tag Design as an Example
William Young (TSMC, Taiwan), Chua-Huang Huang (Feng Chia Univ., Taiwan), Alan P. Su (Global Unichip Corp., Taiwan), C. P. Jou, Fu-Lung Hsueh (TSMC, Taiwan)

Thursday, January 21, 15:30 - 17:10

Thursday, January 21, 15:30 - 17:10 Room 101A
Session 10A: DFM3: Robust Design

Chairs: ***Toshiyuki Shibuya*** - Fujitsu Laboratories of America, Inc, U.S.A.
Yi Chang Lu - National Taiwan Univ., Taiwan

10A-1 Slack Redistribution for Graceful Degradation Under Voltage Overscaling
Andrew B. Kahng, Seokhyeong Kang (UC San Diego, U.S.A.), Rakesh Kumar, John Sartori (UIUC, U.S.A.)

10A-2 A Decoder-Based Switch Box to Mitigate Soft Errors in SRAM-Based FPGAs
Hassan Ebrahimi, Morteza Zamani, HamidReza Zarandi (Amirkabir, Iran)

10A-3s On Process-Aware 1-D Standard Cell Design
Hongbo Zhang, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.),Kai-Yuan Chao (Intel Corp., U.S.A.)

10A-4s D-A Converter Based Variation Analysis for Analog Layout Design
Bo Liu, Toru Fujimura, Bo Yang, Shigetoshi Nakatake (Univ. of Kitakyushu, Japan)

Thursday, January 21, 15:30 - 17:10 Room 101B
Session 10B: Emerging Circuits and Architectures

Chairs: ***Xiaoyang Zeng*** - Fudan Univ., China
Chun-Ming Huang - National Chip Implementation Center, Taiwan

10B-1 Rule-Based Optimization of Reversible Circuits
Mona Arabzadeh, Mehdi Saeedi, Morteza Saheb Zamani (Amirkabir Univ. of Tech., Iran)

10B-2 Variation Tolerant Logic Mapping for Crossbar Array Nano Architectures
Cihan Tunc (Northeastern Univ., U.S.A.), Mehdi Tahoori (Northeastern Univ./Karlsruhe Inst. of Tech., U.S.A.)

10B-3 Generalised Threshold Gate Synthesis based on AND, OR, NOT Representation of Boolean Function
Marek Arkadiusz Bawiec, Maciej Nikodem (Wrocław Univ. of Tech., Poland)

10B-4 Novel Dual-vth Independent-gate FinFET Circuits
Masoud Rostami, Kartik Mohanram (Rice Univ., U.S.A.)

Thursday, January 21, 15:30 - 17:10 Room 101C
Session 10C: System-level MPSoC Analysis and Optimization

Chairs: ***Yuichi Nakamura*** - NEC Corp., Japan
Lovic Gauthier - Kyusyu Univ., Japan

10C-1 Hybrid Dynamic Energy and Thermal Management in Heterogeneous Embedded Multiprocessor SoC
Shervin Sharifi, Ayse Kivilcim Coskun, Tajana Simunic Rosing (Univ. of California, San Diego, U.S.A.)

10C-2 Energy Efficient Joint Scheduling and Multi-core Interconnect Design
Cathy qun Xu (Univ. of Texas, Dallas, U.S.A.), Chun Jason Xue (City Univ. of Hong Kong, China), Yi He (Univeristy of Texas at Dallas, U.S.A.), Edwin H.M. Sha (Univ. of Texas, Dallas, U.S.A.)

10C-3 Dynamic and Adaptive Allocation of Applications on MPSoC Platforms
Andreas Schranzhofer, Jian-Jia Chen (Swiss Federal Inst. of Tech. (ETH), Zürich, Switzerland), Luca Santinelli (Scuola Superiore Sant'Anna, Pisa, Italy), Lothar Thiele (Swiss Federal Inst. of Tech. (ETH), Zürich, Switzerland)

10C-4 Cool and Save: Cooling Aware DynamicWorkload Scheduling in Multi-socket CPU Systems
Raid Ayoub, Tajana Rosing (Univ. of California, San Diego, U.S.A.)

Thursday, January 21, 15:30 - 17:10 Room 101D
Session 10D: Designers' Forum: Embedded Software Development for Multi-Processor Systems-on-Chip

Chairs: ***Rainer Doemer*** - Univ. of California, Irvine, U.S.A.
Andreas Gerstlauer - Univ. of Texas, Austin, U.S.A.

10D-1 The Shrink Wrapped Myth: Cross Platform Software
Mike Olivarez (Freescale Semiconductor, Inc., USA)

10D-2 Using Software to Achieve Low Power Solutions
Albert Shiue (Alvaview Technologies, Taiwan)

10D-3 MPSoC Programming using the MAPS Compiler
Jeronimo Castrillon, Rainer Leupers (RWTH Aachen Univ., Germany)

10D-4 System-level Development of Embedded Software
Gunar Schirner (Northeastern Univ., USA)

Tutorials

Tutorial 1 (Half Day)
Monday, January 18, 9:30 - 12:30, Room 101A
Embedded Software for System-on-Chip (SoC) Design

Organizer:
Tie-Wei Kuo (National Taiwan University, Taiwan)

Speakers:
Lothar Thiele (Swiss Federal Institute of Technology (ETH) , Switserland)
Tie-Wei Kuo (National Taiwan University, Taiwan)

Tutorial Summary:

1. Embedded Software Design for Multiprocessor System-on-Chip (MPSoC)

For many emerging embedded applications, high performance is required: High-quality multimedia processing in consumer electronics, software defined radio in communications systems, or real-time diagnostics in medical systems are typical examples. A frequent choice for digital signal processing systems will be heterogeneous multiprocessor system-on-chip (MPSoCs) because of their computational power, programmability, and low power dissipation.

Software development plays a central role in handling the increasing complexity of applications implemented on MPSoCs. Productively programming heterogeneous MPSoCs requires support for concurrency, timing, heterogeneity, scalability, and hardware/software system integration. This support is only provided to a very limited degree by the traditional practice of using C/C++ and a board support package to program single and multiprocessor signal processing systems.

Recognizing this challenge, a variety of techniques and complete software design flows have been proposed that shift the software development for MPSoCs to higher levels of abstraction. In those design flows, applications are developed using a high-level application programming interface (API), or a model of computation. These approaches attempt to assist software developers in the necessary high-level design decisions and allow automating certain steps in the design flow.

A particular challenge is the performance analysis of MPSoCs which is required for early design space explorat on and final system verification. Simulation-based methods are not well suited for this purpose due to long run-times and missing corner-case coverage. To overcome these limitations, formal performance analysis methods that scale to large systems and provide guarantees for meeting real-time constraints have been developed. Embedding formal performance analysis into the MPSoC design cycle requires the generation of a faithful analysis model and its calibration with the system-specific parameters.

The tutorial will provide an overview about the major challenges in multiprocessor software development.We will present a taxonomy of software design flows based on this analysis, review current MPSoC software design flows and classify them based on the associated challenges. As an example, a design flow is presented that integrates a modular performance analysis method into the MPSoC programming environment. The result is an MPSoC software design flow that allows to automatically generate the system implementation together with an analysis model for system verification.

2. The Design and Implementation Issues of Flash-Memory Storage Systems

While flash memory has been widely adopted in the implementations of various storage systems, it recently receives a lot of attention in various system-component designs. With the unique characteristics of flash memory, it is highly challenging in the designs of management software, especially when reliability and performance become major concerns. In this tutorial, we will summarize popular implementations of the management software, and the behavior analysis of flash-memory storage systems will also be addressed.Challenge issues for current and future implementations, especially on reliability and file-system considerations, and some potential solutions will be presented.

Tutorial 2 (Half Day)
Monday, January 18, 14:00 - 17:00, Room 101A
Analog and Mixed-signal Circuit Design in Nanometer CMOS Technologies

Organizer & Speaker:

Georges Gielen (Katholieke Universiteit Leuven, Belgium)

Tutorial Summary:

Nanometer CMOS technologies pose particular challenges to the design of analog and mixed-signal integrated circuits. This tutorial will discuss design techniques to overcome these challenges and will illustrate this with several practical design examples.Examples given include ultra-low-power design, design for reliability, reconfigurable designs, etc.

Tutorial 3 (Full Day)
Monday, January 18, 9:30 - 17:00, Room 101B
3D Integrated Circuit Design

Organizer:

Sachin Sapatnekar (ECE Dept., University of Minnesota , USA)

Speakers:

Paul Franzon (ECE Dept., North Carolina State University, USA)
Ruchir Puri (IBM TJ Watson Research Center, USA)
Sachin Sapatnekar (ECE Dept., University of Minnesota , USA)
Yuan Xie (CSE Dept., Pennsylvania State University, USA)

Tutorial Summary:

Despite generation upon generation of technology scaling, computer chips have remained essentially two-dimensional (2D). Improvements in the on-chip wire delay, and in the maximum number of inputs and outputs per chip have not been able to keep up with transistor performance growth, and it has become progressively harder to hide the discrepancy. In contrast with these conventional 2D circuits, 3D integrated circuits offer a new paradigm that builds multiple tiers of active devices stacked above each other.Recent advances in process technology have brought 3D technology to the point where it is feasible and practical, and it has raised widespread interest in the chip industry. The move to 3D allows numerous benefits over 2D, such as reduced

interconnect lengths, improved computation per unit volume, and the possibility of integrating heterogeneous systems. However, the paradigm requires a significant change from contemporary design methodologies, since an optimal 3D chip design has very different characteristics from an optimal 2D chip design. The goal of this tutorial is to provide an overview of the technology, the corresponding design challenges, and existing solutions to overcome these challenges.

3D chip technologies come in a number of flavors that are expected to enable the extension of CMOS performance. Designing in 3D forces the industry to look at formerly-two-dimensional integration issues quite differently, and requires the re-fitting of multiple existing EDA capabilities. We begin with an overview of the motivation for 3D, process steps, and delve into the design issues in detail.

We then address how the technology can be used to provide significant performance benefits: up to now 3DIC technologies, through silicon vias (TSV), and bonding techniques, have mainly been exploited in view of their potential for miniaturization. However, the open question is how to exploit 3DIC for reasons beyond just size and weight. It is becoming clear that if the system is re-architected to explicitly account for 3D IC technology, advantages can be gained in performance, power consumption, and cost. However, complicating factors that must be dealt with include partitioning, design management, thermal design, and manufacturing test.

A key part of the 3D solution lies in the development of EDA solutions to address such 3D-specific issues,and the next part of the tutorial overviews the specific role for new computer-aided design (CAD) tools that can solve problems related to building designs in 3D: specifically, 3D physical design, thermal management,and power delivery. We will also discuss how one can extend the existing 2D design flows to adapt to 3D as opposed to inventing new flows. Design flow steps unique to 3D will also be described.

Finally, the tutorial will address architectural issues in 3D design. Design space exploration at the architectural level

technologies and to build high performance microprocessors. In this tutorial, we will discuss fine-granularity and coarse-granularity processor design options, and present various novel architecture designs enabled by 3D integration, leveraging the benefits of faster and high-bandwidth communication to stacked layer, as well as the heterogeneous integration capability.

Tutorial 4(Full Day)
Monday, January 18, 9:30 - 17:00, Room 101C
Industrial Low-Power Circuit Design

Organizer:

Pei-Hsin Ho (Synopsys Inc., USA)

Speakers:

Louis Jiing-Yuan Lin (Global Unichip Corporation, Taiwan)
Yoshio Inoue (Renesas Technology Corporation, Japan)
David Flynn (ARM Ltd., UK)
Pei-Hsin Ho (Synopsys Inc., USA)

Tutorial Summary:

Power consumption is the primary concern for almost all IC designs --- whether they target consumer electronics or high-performance computers. In this tutorial, world-class experts will illustrate state-of-the-art low-power design techniques and share silicon-proven design experiences that practitioners as well as researchers in low-power design may find useful and insightful. In particular, the tutorial will cover details of leakage power minimization through power gating, including discussions of (1) in-rush current and dynamic IR drop analysis, (2) power switch placement and stitching, (3) state retention overhead minimization and reliability analysis, (4) power-gating testability and (5) implementing low-power SoCs using EDA tools that support UPF or CPF. The tutorial will also cover details of dynamic power minimization through multiple power domain design and advanced low-power System, RTL and physical design, including discussions of (1) multi-Vdd designs, (2) DVFS (Dynamic Voltage and Frequency Scaling) implementation and verification, (3) multi-depth sleep mode, (4) low-power clock-tree synthesis and (5) low-power asynchronous design.

The speakers will also discuss their hands-on experiences in 65nm technologies, large low-power SoCs, designs with 50 power modes, power gating using PMK (power management kits) and ARM1176JZF-S processor.

Tutorial 5 (Full Day)
Monday, January 18, 9:30 - 17:00, Room 101D
The Convergence and Inter-relationship of Yield, Design for Manufacturability and Test

Organizer:

Srikanth Venkataraman (Intel Corporation , USA)

Speakers:

Srikanth Venkataraman (Intel Corporation , USA)
Robert C. Aitken (ARM Ltd., USA)

Tutorial Summary:

The tutorial goal is to how design for yield (DFY) and design for manufacturability (DFM) aretightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. As feature sizes reduced to 90 nm micron and below, systematic mechanism-limited yield loss began to appear as a substantial component in yield loss due to the interaction between design and manufacturing. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. In DFM/DFY circles, it is common to speak of defect limited yield, but it is less common to think of test-limited yield, yet this concept is common in DFT (e.g. IDDQ testing, delay testing). Test techniques to close the loop by crafting test patterns to expose the defect prone feature and circuit marginality through ATPG, and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact are covered.This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area,and to apply these concepts in their jobs.

Section 1: Introduction and background (30 mins)

- Introduction
- Tutorial goal
- What is Yield?
- What is DFX? Interaction of manufacturability, yield, variability, and test

Section 2: Yield and Fab Metrology (60 mins)

- Manufacturability versus yield
- Sources of Yield loss – Random, Systematic and Parametric, Defect versus design-related
- Yield models and metrics: Poisson, negative binomial, Murphy,
- Economics of yield
- Redundancy/Repair: Memory and logic
- How does a Fab improve defectivity and manage yield? Fab Metrology, In-line inspections,Process control, Test chips and test structures,SRAM-based, feature-based, ring oscillators,Yield management systems (YMS)

Section 3: DFM - Design for Manufacturability(90 mins)

- What is DFM?
- Lithography: DRC rules, recommendations, shape-based effects, process window, simulation
- Resolution Enhancement Techniques (RET): Optical proximity correction (OPC), Phase shift mask (PSM), Sub resolution assist features (SRAF), Off axis illumination (OAI)
- Chemical Mechanical Polishing (CMP): CMP modeling and analysis, density rules, dummy metal fill, systematic versus random components
- Random defects and Critical Area Analysis (CAA): Shorts / opens / vias / contacts, inductive fault analysis, tradeoffs, optimization,

ASP-DAC 2010 at a Glance

Monday, January 18, 2010

HALF-DAY Tutorials	
9:30 - 12:30	**Room 101A**
Tutorial 1 Embedded Software for System-on-Chip (SoC) Design	
14:00 - 17:00	**Room 101A**
Tutorial 2 Analog and Mixed-signal Circuit Design in Nanometer CMOS Technologies	

FULL-DAY Tutorials	
9:30 - 17:00	**Room 101B**
Tutorial 3 3D Integrated Circuit Design	
9:30 - 17:00	**Room 101C**
Tutorial 4 Industrial Low-Power Circuit Design	
9:30 - 17:00	**Room 101D**
Tutorial 5 The Convergence and Inter-relationship of Yield, Design for Manufacturability and Test	

Tuesday, January 19, 2010

Room 101A	Room 101B	Room 101C	Room 101D
Op (Room 101) Opening 8:30 - 9:00			
1K (Room 101) Keynote Session I 9:00 - 10:00			
2K (Room 101) Keynote Session II 10:20 - 11:20			
3K (Room 101) Keynote Session III 11:20 - 12:20			
1A Embedded Systems Design Techniques 13:30 - 15:10	1B Advanced Model Order Reduction Technique 13:30 - 15:10	1C Logic Synthesis 13:30 - 15:10	1D Special Session: Techniques for Efficient Energy Harvesting and Generation for Portable and Embedded Systems 13:30 - 15:10
2A Memory Management and Compiler Techniques 15:30 - 17:10	2B Power and Signal Integrity 15:30 - 17:10	2C System-level Simulation 15:30 - 17:10	2D Special Session: 3D Integration and Networks on Chips 15:30 - 17:10

Wednesday, January 20, 2010

Room 101A	Room 101B	Room 101C	Room 101D
3A Emerging Memories and 3D ICs 8:30 - 10:10	3B Macromodeling and Verification of Analog Systems 8:30 - 10:10	3C System-level Modelling and Analysis 8:30 - 10:10	3D Special Session: Recent Advancement in Post-silicon Validation 8:30 - 10:10
4A New Techniques for Beyond-die Routing 10:30 - 12:10	4B Analog Layout and Testing 10:30 - 12:10	4C New Techniques in Technology Mapping 10:30 - 12:10	4D University LSI Design Contest 10:30 - 12:10
5A Clock Network Analysis and Optimization 13:30 - 15:10	5B Test Solutions for Emerging Applications 13:30 - 15:10	5C Power, Performance and Reliability in SoC Design 13:30 - 15:10	5D Designers' Forum: State-of-the-art SoCs 13:30-15:10
6A Advances in Modern Clock Tree Routing 15:30 - 17:10	6B Timing-related Testing and Diagnosis 15:30 - 17:10	6C Application-specific NoC Design 15:30 - 17:10	6D Designers' Forum: Is 3D Integration an Opportunity or Just a Hype? 15:30-17:10

Thursday, January 21, 2010

Room 101A	Room 101B	Room 101C	Room 101D
7A Modern Floorplanning and Placement Techniques 8:30 - 10:10	7B Power Optimization and Estimation in the DSM Era 8:30 - 10:10	7C Design Verification and Debugging 8:30 - 10:10	7D Special Session: Dependable Silicon Design with Unreliable Components 8:30 - 10:10
8A DFM1: Patterning and Physical Design 10:30 - 12:10	8B Design and Verification for Process Variation Issues 10:30 - 12:10	8C New Advance in High-level Synthesis 10:30 - 12:10	8D Special Session: ESL: Analysis and Synthesis of Multi-core Systems 10:30 - 12:10
9A DFM2: Variation Modeling 13:30 - 15:10	9B Power Grid Analysis 13:30 - 15:10	9C High-level Synthesis and Optimization for Performance and Power 13:30 - 15:10	9D Designers' Forum: ESL, The Road to Glory, Or Is It Not? Real Stories about Using ESL Design Methodology in Product Development 13:30 - 15:10
10A DFM3: Robust Design 15:30 - 17:10	10B Emerging Circuits and Architectures 15:30 - 17:10	10C System-level MPSoC Analysis and Optimization 15:30 - 17:10	10D Designers' Forum: Embedded Software Development for Multi-Processor Systems-on-Chip 15:30 - 17:10

Registration

Advance Registration Deadline: Dec. 20, 2009, Taiwan Time (GMT+8)

Online registration is recommended. If the web-based registration is inconvenient to you, please complete the **registration form** and fax it to :

Conference Registration

Ms. Yvonne Chen / Ms. Lylia Chu
TEL: +886-3-591-3003 or 591-2673
FAX: +886-3-5820303
E-Mail: YvonneChen@itri.org.tw
Room 100, Bldg. 21, 195 Sec. 4 Chung-Hsing Rd.
Chutung, Hsinchu, Taiwan 310, R.O.C.

◎Registration Fee (currency exchange rate in December 2009 is around US$1 to NT$32.5)

Category	By Dec. 20, 2009	After Dec. 21, 2009
【Conference】		
*Member	NT$17,300	NT$19,000
Non-member	NT$20,700	NT$22,200
Full-time Student	NT$10,800	NT$12,400
【Designers' Forum】		
*Member	NT$7,400	NT$9,100
Non-member	NT$7,400	NT$9,100
Full-time Student	NT$7,400	NT$9,100
【Tutorial - Full Day】		
*Member	NT$10,500	NT$12,000
Non-member	NT$12,400	NT$13,700
Full-time Student	NT$7,100	NT$8,100
**Student Group	NT$2,100	N/A
【Tutorial - Half Day】		
*Member	NT$7,100	NT$8,500
Non-member	NT$8,500	NT$9,800
Full-time Student	NT$4,500	NT$5,200
**Student Group	NT$1,300	N/A

* Member of IEEE, ACM SIGDA, TICD
**A group of 5 or more full-time students from same institute for early registration only.

Additional Options	
CD-ROM version proceedings	NT$600
Tutorial handout	NT$300
Banquet ticket	NT$1,500

The conference fee includes:

- Admission to all sessions (including keynote speeches and designers' forum) without tutorials
- Cocktail Reception
- Banquet (excluding Full-time students)
- One refreshment per break
- Conference kit (with a final program and one CD-ROM of conference proceedings).

The designers' forum fee includes:

- Admission to Keynote Speech and Designers' Forum
- One CD-ROM of conference proceedings
- One refreshment per break
- Cocktail Reception

The tutorial fee includes:

- Admission to full-day or half-day tutorial(s)
- One copy of all tutorial texts
- One lunch coupon
- One refreshment per break

*Presenters registering as Full-time students will receive a banquet ticket.

*Student Group: Limited seats of tutorials are provided to student group registration of 5 or more full-time students from same institute. Please register online with group registration before Dec. 20, 2009.

*Proceedings: ASP-DAC 2010 will be producing CD-ROM version Proceedings only. All papers will be included in the CD-ROM version Proceedings. Additional CD-ROM version Proceedings will be available for purchase at the conference. The price is NT$600.

*The CD-ROM version Proceedings will also be available for purchase after the conference; please contact IEEE and ACM SIGDA for the CD-ROM version.

*Banquet: The banquet will be held from 18:00 to 20:00 on January 20, 2010 at the fourth floor of conference venue. Designers' Forum-only ,Tutorial-only and non-presenter Full-time Student conference registrants wishing to attend the banquet can purchase banquet tickets online or pay NT$1,500 for a ticket when they register on site

REGISTRATION DETAILS

- All participants (including speakers) are requested to register ON-LINE.
- The Registration fee may be paid by bank draft or credit card. Please make check/bank draft payable to “Industrial Technology Research Institute”. Credit card payment is only accepted on line. All of your information will be secured by SSL.
- A registration confirmation will be sent once the payment has been completed.
- Each registrant must register individually.
- If you could not register successfully through the internet, please download the Registration Form and fill it out; then send it by E-mail or fax to Conference Registrar.

CANCELLATION AND REFUND

If written notice of cancellation reaches the Conference Registrar:

- Before 23:59 GMT+0800, December 20, 2009, USD$40 (TWD1, 300) cancellation fee will be deducted from the refund.
- After 23:59 GMT+0800, December 20, 2009, no refund will be given. Yet, a copy of CD-ROM Proceedings will be sent to the registrant after the Conference.
- For any further query, please contact the Conference Registrar.

ASP-DAC 2010 Registration Form (1/2)

Advance Registration Deadline: Dec. 20, 2009, Taiwan Time (GMT+8)

Family Name		**First Name**	
Title	☐ Mr. ☐ Prof. ☐ Dr. ☐ Mrs. ☐ Ms.		
Affiliation	☐ Industrial ☐ Research ☐ Academia ☐ Professor ☐ Student		
Name of Company/School			
Speaker	☐ Yes ☐ No	**Session No.**	
Address			
City		**State/Country**	**Zip Code**
Telephone	( )	**Fax**	( )
E-mail	(*REQUIRED* for registration confirmation)		
Membership	☐ IEEE ☐ ACM SIGDA ☐ TICD ☐ Non-member		
IEEE Number		**Student ID**	

Tutorial (Please choose one Full-Day topic or **one/two** Half-Day topics.)

☐	**Tutorial 1** (Half Day)	Embedded Software Design for Multiprocessor System-on-Chip (MPSoC)
☐	**Tutorial 2** (Half Day)	Analog and Mixed-signal Circuit Design in Nanometer CMOS Technologies
☐	**Tutorial 3** (Full Day)	3D Integrated Circuit Design
☐	**Tutorial 4** (Full Day)	Industrial Low-Power Circuit Design
☐	**Tutorial 5** (Full Day)	The Convergence and Inter-relationship of Yield, Design for Mnufacturability and Test

Registration Fee (currency exchange rate in December 2009 is around US$1 to NT$32.5)

Category	By Dec. 20, 2009	After Dec. 21, 2009
[Conference]		
☐ *Member	NT$17,300	NT$19,000
☐ Non-member	NT$20,700	NT$22,200
☐ Full-time Student	NT$10,800	NT$12,400
[Designers' Forum]		
☐ *Member	NT$7,400	NT$9,100
☐ Non-member	NT$7,400	NT$9,100
☐ Full-time Student	NT$7,400	NT$9,100
[Tutorial - Full-Day]		
☐ *Member	NT$10,500	NT$12,000
☐ Non-member	NT$12,400	NT$13,700
☐ Full-time Student	NT$7,100	NT$8,100
☐ **Student Group	NT$2,100	N/A
[Tutorial - Half-Day]		
☐ *Member	NT$7,100	NT$8,500
☐ Non-member	NT$8,500	NT$9,800
☐ Full-time Student	NT$4,500	NT$5,200
☐ **Student Group	NT$1,300	N/A
[Additional Options]		
☐ CD-ROM version proceedings	NT$600	X ( ) copy(ies)
☐ Tutorial handout	NT$300	X ( ) copy(ies)
☐ Banquet ticket	NT$1,500	X ( ) copy(ies)
Total Payment Due	**NT$**	

**Member of IEEE, ACM SIGDA, TICD*

***A group of 5 or more full-time students from same institute for early registration only.*

ASP-DAC 2010 Registration Form (2/2)

Payment Method			
☐ **Check/Bank Draft** Make check/bank drafts payable to: ***Industrial Technology Research Institute***			
☐ **Credit Card** (Only TWD will be charged by credit card.)			
Issue Bank		☐ Master ☐ Visa ☐ JCB	
Card Number		Exp.Date (month/year)	
The last three digits on the signature panel (the reverse side of the card)			
Signature			

***The conference fee includes:** Admission to all sessions (including keynote speeches and designers' forum) without tutorials, Cocktail Reception, Banquet (excluding Full-time students), one refreshment per break and conference kit (with a final program and one CD-ROM of conference proceedings).

*Presenters registering as Full-time students will receive a banquet ticket.

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Information

Visa for Arriving Taiwan

Foreign nationals may obtain visas from embassies consulates or representative offices of the Republic of China.

Visa Exempt Entry : 30 days (no extension is permitted)

Thirty-day visa-free privileges are afforded to citizens of the Australia, Austria, Belgium, Canada, Costa Rica, Denmark, Finland, France, Germany, Greece, Ireland, Iceland, Italy, Japan, Republic of Korea, Liechtenstein, Luxembourg, Malaysia, Malta, Monaco, the Netherlands, New Zealand, Norway, Portugal, Singapore, Spain, Sweden, Switzerland, U.K. and U.S.A. Requirements for the entry are:

1. A passport valid for at least six months.
2. A confirmed return air ticket or an air ticket and a visa for the next destination, and a confirmation air seat reservation for his (her) departure.
3. No criminal record of law violation.

Landing Visa: 14 days (no extension is permitted)

Fourteen-day landing visas can be obtained upon arrival at Taoyuan airport. Passengers with passports of the above listed countries plus the Czech Republic, Hungary, Poland and Switzerland are to apply for landing visa. Requirements for the entry are:

1. A passport valid for at least six months.
2. A confirmed return air ticket or an air ticket and a visa for the next destination, and a confirmation air seat reservation for his (her) departure.
3. An application form with one photo.
4. Visa fee NT$ 1,500. (Approximately 45 US dollars)
5. No criminal record of law violation.

Visa for People Holding Passport of Mainland China

Please read this guideline (PDF Format) for detailed information, fill in the application form (PDF Format), and then air-mail (preferably express mail) "Filled Application Form", "Xerox Copy of Identification Card", "Two 2 inch Self-photo" and "Job Certificate" before January 1, 2007 to: The Secretariat of TS2007, ME

Department, National Taiwan University of Science and Technology, 43, Keelung Road, Section 4, Taipei, Taiwan, ROC. The necessary application form and further information can be found on the web site: http://www.boca.gov.tw/

Currency

The Republic of China's unit of currency is the New Taiwan Dollar (NT$). Bill denominations are NT$2000, NT$1000, NT$500, NT$200, and NT$100. Coin denominations are NT$1, NT$5, NT$10 and NT$50. As of December 2009, the exchange rate was quoted around NT$32.5 to one US Dollar. Foreign currencies can be exchanged at the airport upon arrival, or at government-authorized banks, tourist hotels, and large department stores. Receipts are given when currency is exchanged, and must be presented in order to exchange unused NT Dollars before departure. Traveler's checks in major currencies may be cashed at some tourist-oriented businesses and at most international tourist hotels.

Credit Cards

Hotels, department stores, airlines, large stores and restaurants accept major credit cards. Cash is generally preferred elsewhere.

Banking Hours

Banks are open from 9 a.m. to 3:30 p.m., Monday to Friday.

Electricity Supply

Taiwan uses electric current of 110 volts at 60 cycles, appliances from Europe, Australia or South-East Asia will need an adaptor or transformer. Many buildings have sockets with 220 volts especially for the use of air conditioners.

Accommodation

Due to the hot season in Taipei, the hotel room availability is not guaranteed by hotels even though a block of rooms has been reserved for ASP-DAC participants at the following hotels near the TICC: Grand Hyatt Taipei, The Tango Hotel, Taipei Fullerton Hotel East, United Hotel, Agora Garden, Pacific Business Center-Taipei and Charming Hotel. Please make your hotel reservation **NO LATER THAN DECEMBER 31st, 2009** to qualify for a room under the conference special rates.

The Conference sessions will be held at the Taipei International Convention Center (TICC). Please notice the distance from the hotels to the TICC. Please check the hotel information below and fax the reservation form back to the hotel you choose for reservation.

Hotel	Room Rate (NTD; Tax Included)		Charges including
1. Grand Hyatt Taipei http://www.grandhyatttaipei.com.tw/ Fax : +886-2-2720-1111	Grand Room (Single Occupancy)	4,500	Breakfast
	Grand Room (Double Occupancy)	5,100	
2. The Tango Hotel http://www.tango-hotels.com Fax: +886-2- 2528-7676	Junior Suite	4,550	Breakfast
	Executive King	4,200	
3. United Hotel http://www.unitedhotel.com.tw/ Fax No.: +886-2-2741-2789	Superior Single	3,700	Breakfast
	Superior Twin	3,900	
4. Agora Garden http://www.agoragdn.com.tw/mainpage.asp Fax: +886-2-8780-5608	Studio Single Room	3,600	Breakfast
	Agora Suite Twin	3,900	
5. Taipei Fullerton Hotel East http://www.taipeifullerton.com.tw/east_32/ Fax : +886-2-2720-1111	Deluxe Single Room	3,200	Breakfast
	Deluxe Twin Room	3,600	
6. Pacific Business Center-Taipei http://www.businesscenter.com.tw/ Fax: +886-2-8780-5000	Superior Single Room	2,900	Breakfast
	Business Twin Room	3,500	
7. Charming Hotel http://charming.hotel.com.tw/ Fax : +886-2-2765-7092/ +886-2-2762-5931	Standard Single	1,880	Breakfast
	Superior Single(Twin)	2,480	

* Currency exchange rate in December 2009 is around USD1 to NT$32.5).
* Please check with the hotel for payment method.

For more information about accommodations and room reservations for each hotel, please contact:

Grand Hyatt Taipei
Tel : +886-2-2720-1200 Ext : 3158
Fax : +886-2-2720-1111
Address: 2, Song Shou Road, Taipei, Taiwan
e-mail : taipei.grand@hyatt.com
Website : http://www.grandhyatttaipei.com.tw/
Transportation:
1. Airport pickup service cost NT$2,200 (Mercedes-Benz 320)
2. Taxi from Taoyuan Airport terminal taxi stop to hotel costs around NT$1,500
3. Takes 3-5 minutes from the Grand Hyatt Taipei to the conference site by walk.

The Tango Hotel
Tel : +886-2-2528-8000
Contact Window: Erica Chen
Fax : +886-2-2528-7676
Address: 297, ZhongXiao East Road, Section 5, Taipei 110, Taiwan
e-mail : rsvn.xy@tango-hotels.com
ericachen@tango-hotels.com
Website : http://www.tango-hotels.com
Transportation:
1. Airport pickup service cost NT$1,600 (Mercedes-Benz 320)
2. Taxi from Taoyuan Airport terminal taxi stop to hotel costs around NT$1,500
3. Takes 10-15 minutes from the Tango Hotel to the conference site by walk.

United Hotel
Tel : +886- 2-2773-1515
Fax : +886- 2-2741-2789
Address: No. 200, Kwang Fu S. Road, Taipei, Taiwan
E-mail : reservation@unitedhotel.com.tw
Website : http://www.unitedhotel.com.tw/index.php
Transportation:
1. Airport pickup service costs NT$1,600 (Mercedes-Benz 320)
2. Taxi from Taoyuan Airport terminal taxi stop to hotel costs around NT$1,500
3. Takes 20 minutes from the United Hotel to the conference site by walk.

Agora Garden
Tel : +886-2-8780-5168
Fax : +886-2-8780-5608
Address: No. 68, Sung-Kao, Road, Taipei, Taiwan
e-mail : owen@agoragdn.com.tw
rsv@agoragdn.com.tw
Website : http://www.agoragdn.com.tw/mainpage.asp
Transportation:
1. Airport pickup service costs NT$2,000 (Lexus 430)
2. Taxi from Taoyuan Airport terminal taxi stop to hotel costs around NT$1,500
3. Takes 15 minutes from the Agora Garden to the conference site by walk.

Taipei Fullerton Hotel East
Tel : +886- 2-2763-5656
Fax : +886- 2-2767-9347
Address: 32 Nanking East Road, Section 5 , Taipei, Taiwan
E-mail : service3@taipeifullerton.com.tw
Website : http://www.taipeifullerton.com.tw/east_32/html/eng_south/about_us.htm
Transportation :
1. Airport pickup service costs NT$1,700 (Mercedes-Benz 320)
2. Taxi from Taoyuan Airport terminal taxi stop to hotel costs around NT$1,500
3. Takes 30 minutes from the Taipei Fullerton Hotel East to the conference site by walk.

Pacific Business Center-Taipei
Tel : +886-2-8780-8000
Fax : +886-2-8780-5000
Address: 11F 495 Guang-Fu S. Road , Taipei, Taiwan
E-mail : pbc.taipei@msa.hinet.net
Website: http://www.businesscenter.com.tw/
Transportation :
1. Airport pickup service costs NT$ 1,600 (Mercedes-Benz 320)
2. Taxi from Taoyuan Airport terminal taxi stop to hotel costs around NT$1,500
3. Takes 10 minutes from the Pacific Business Center-Taipei to the conference site by walk.

Charming Hotel
Tel : +886-2-2763-0555
Fax : +886-2-2762-5931
+886-2-2765-7092
Address: 16, Sec.4,Pa-Teh Road, Taipei, Taiwan
e-mail : charmin.hotel@msa.hinet.net
Website : http://charming.hotel.com.tw/about.asp
Transportation :
1. Airport pickup service costs NT$1,300 (Toyota Wish)
2. Taxi from Taoyuan Airport terminal taxi stop to hotel costs around NT$1,500
3. Takes about 30 minutes from the Charming Hotel to the conference site by walk.

ASP-DAC 2010 Hotel Reservation Form

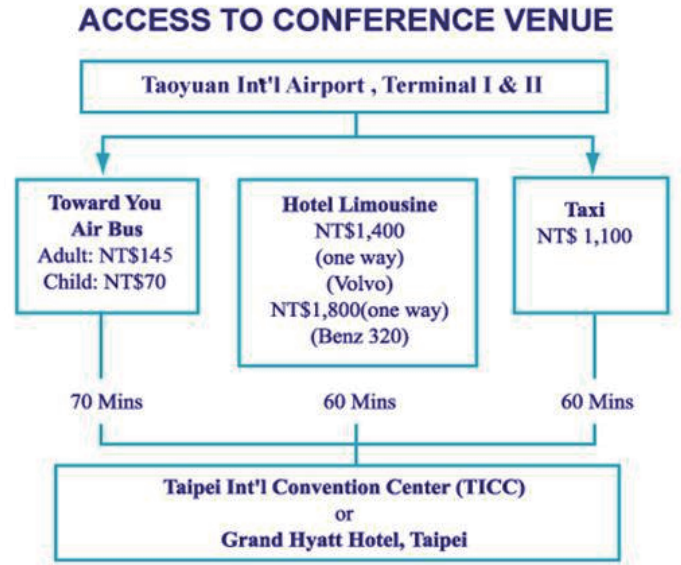
To secure the conference rates, please fill out and forward the form to the appropriate hotel. Mark room type on the following brackets and your preferences and **FAX it back to that Hotel you prefer NO LATER THAN DECEMBER 31st, 2009.** The availability is limited so please make the reservation as soon as possible and be sure to follow up on your reservation wih the hotel you have chosen.

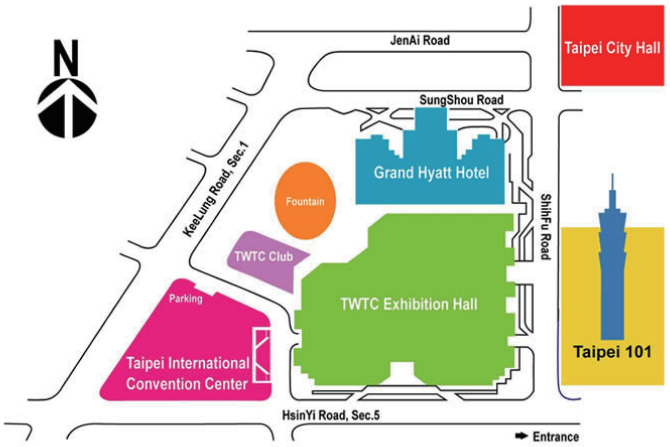
Hotel	Room Rate (NTD; Tax Included)		No. of Rooms Requested
1. Grand Hyatt Taipei http://www.grandhyatttaipei.com.tw/ Fax : +886-2-2720-1111 *Please refer to the hotel reservation form at the conference website.	Grand Room (Single Occupancy)	4,500	
	Grand Room (Double Occupancy)	5,100	
2. The Tango Hotel http://www.tango-hotels.com Fax: +886-2- 2528-7676	☐ Junior Suite	4,550	
	☐ Executive King	4,200	
3. United Hotel http://www.unitedhotel.com.tw/ Fax No.: +886-2-2741-2789	☐ Superior Single	3,700	
	☐ Superior Twin	3,900	
4. Agora Garden http://www.agoragdn.com.tw/mainpage.asp Fax: +886-2-8780-5608	☐ Studio Single Room	3,600	
	☐ Agora Suite Twin	3,900	
5. Taipei Fullerton Hotel East http://www.taipeifullerton.com.tw/east_32/ Fax : +886-2-2720-1111	☐ Deluxe Single Room	3,200	
	☐ Deluxe Twin Room	3,600	
6. Pacific Business Center-Taipei http://www.businesscenter.com.tw/ Fax: +886-2-8780-5000	☐ Superior Single Room	2,900	
	☐ Business Twin Room	3,500	
7. Charming Hotel http://charming.hotel.com.tw/ Fax : +886-2-2765-7092 / +886-2-2762-5931	☐ Standard Single	1,880	
	☐ Superior Single(Twin)	2,480	

Arrival Dates	(mm/dd)	**Departure Dates**	(mm/dd)
Arrival Time		**Arrival Flight No.**	
Last Name		**First Name**	
Title		**Company Name**	
Telephone		**Fax**	
Address			
State/City		**Country**	
E-mail		**Zip Code**	
Hotel Car Service	☐ Not required ☐ Yes, Taoyuan airport to hotel ☐ Yes, Hotel to Taoyuan Airport		
HOTELS REQUIRE GUARANTEE BY CREDIT CARD			
Credit Card	☐ American Express ☐ Master ☐ Visa ☐ JCB		
Credit Card No.	☐☐☐☐-☐☐☐☐-☐☐☐☐-☐☐☐☐		
EXP. Date	☐☐/☐☐ (mm/yy)		
Signature			

【Please confirm rules with hotels upon confirmation for guarantee and cancellation.】

Access to Taipei International Convention Center (TICC)



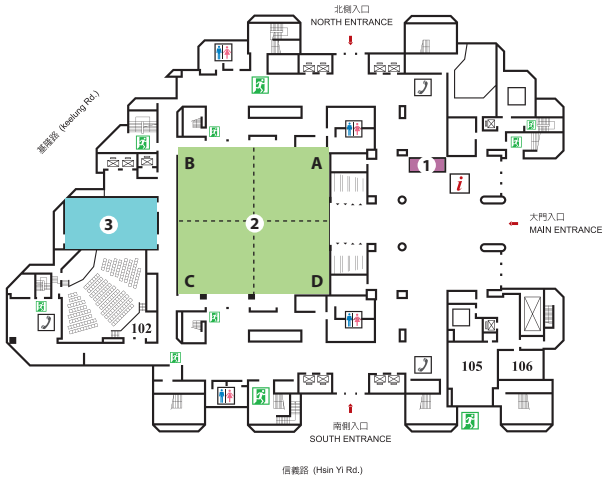


*Approximate price quote and traveling time.

Venue Map/ Room Assignment

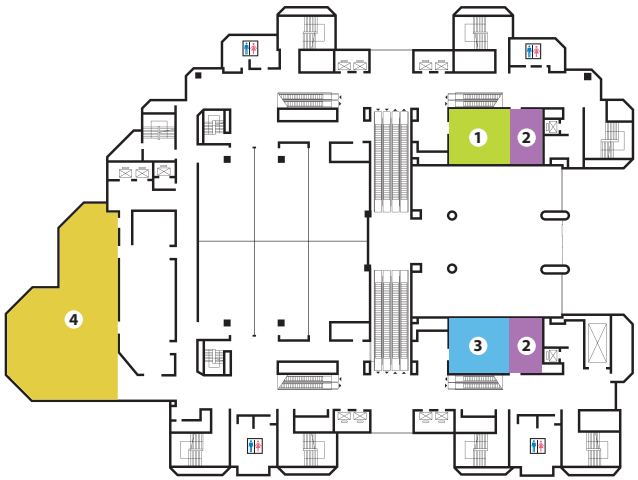
1st Floor

1. Main Entrance - Registration & Information
2. Room 101 – Opening, Keynote
   Room 101 A, B, C, D – Tutorial, Oral Sessions
3. Room 103 – Student Forum, University LSI Design Contest, Internet Lounge



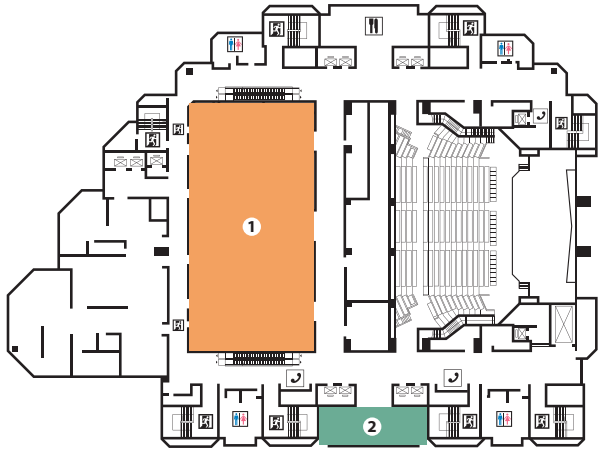
2nd Floor

1. Room 203A - Secretariat
2. Room 202B, 203B – Rehearsal Room
3. Room 202A – Meeting Room
4. International Lounge - Reception



3rd Floor

1. Banquet Hall – Tutorial's Lunch
2. South Lounge - Speakers' Breakfast



4th Floor

1. VIP Room - Banquet