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1855

AdaMS: Adaptive MLC/SLC Phase-Change Memory Design for File Storage

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Current Storage Technology

- Hard-Disk Drive

Slow

- Flash Drive

Small capacity

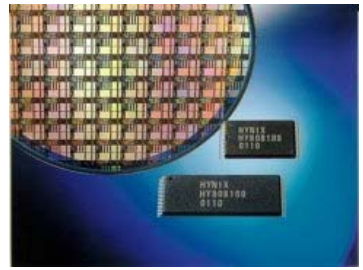
- Solid-State Drive

Based on the NAND flash technology

Expensive
Not large enough, not fast enough

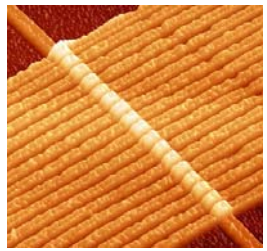
Non-volatile RAM "Revolution"

- FeRAM (Ferroelectric RAM)
- MRAM (Magnetic RAM)
- ReRAM (e.g. Memristor)
- PCRAM (Phase-Change RAM)



Toshiba
FeRAM(2009)

EverSpin
MRAM(2008)

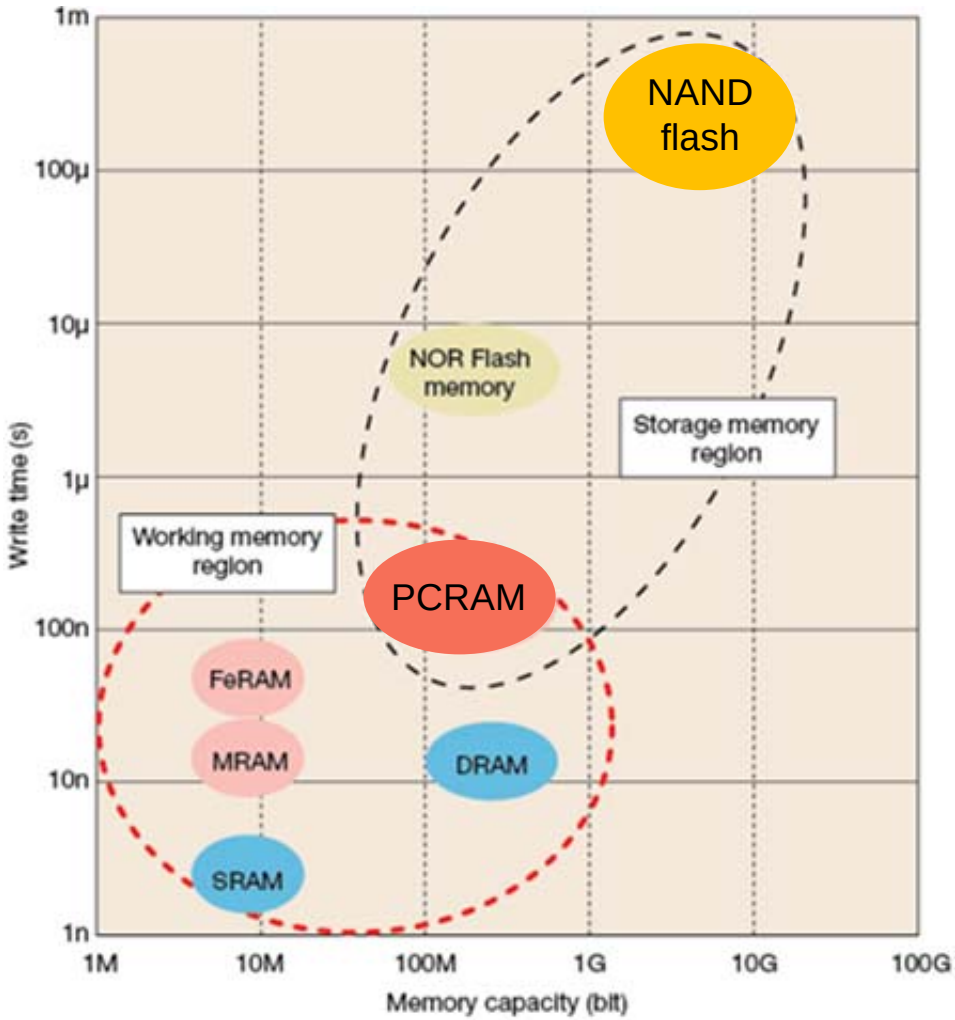


HP Labs
Memristor (2009)

Samsung
PCRAM (2008)

Why PCRAM is better than NAND flash?

- Speed:
  - PCRAM is 2-3 orders faster than NAND flash
- Endurance:
  - PCRAM has 3 orders higher endurance than flash
- Scalability:
  - NAND flash is hard to scale beyond 20nm, but PCRAM is projected to sub-10nm
- Byte-accessibility
  - PCRAM does not have the erase operation, and can be accessed under any granularity

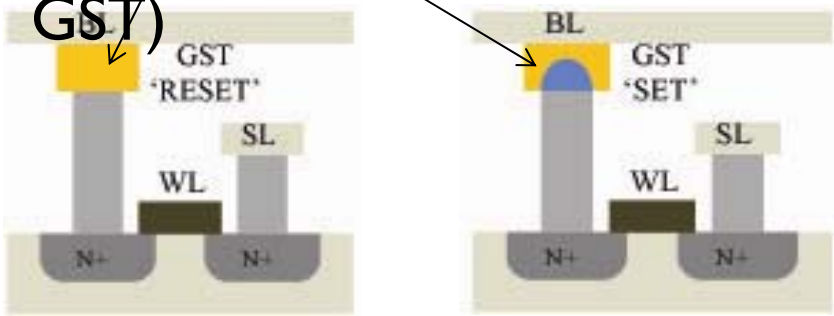


Courtesy: Motoyuki Ooishi

PCRAM Introduction

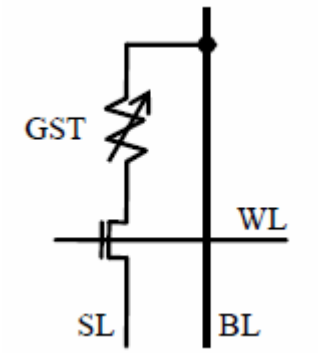
- First explored in 1966
- Mass production starts in 2009
- Use Chalcogenide to store '0' and '1's
  - Same as CD-RW and DVD-RW

Chalcogenide (GeSbTe, or GST)



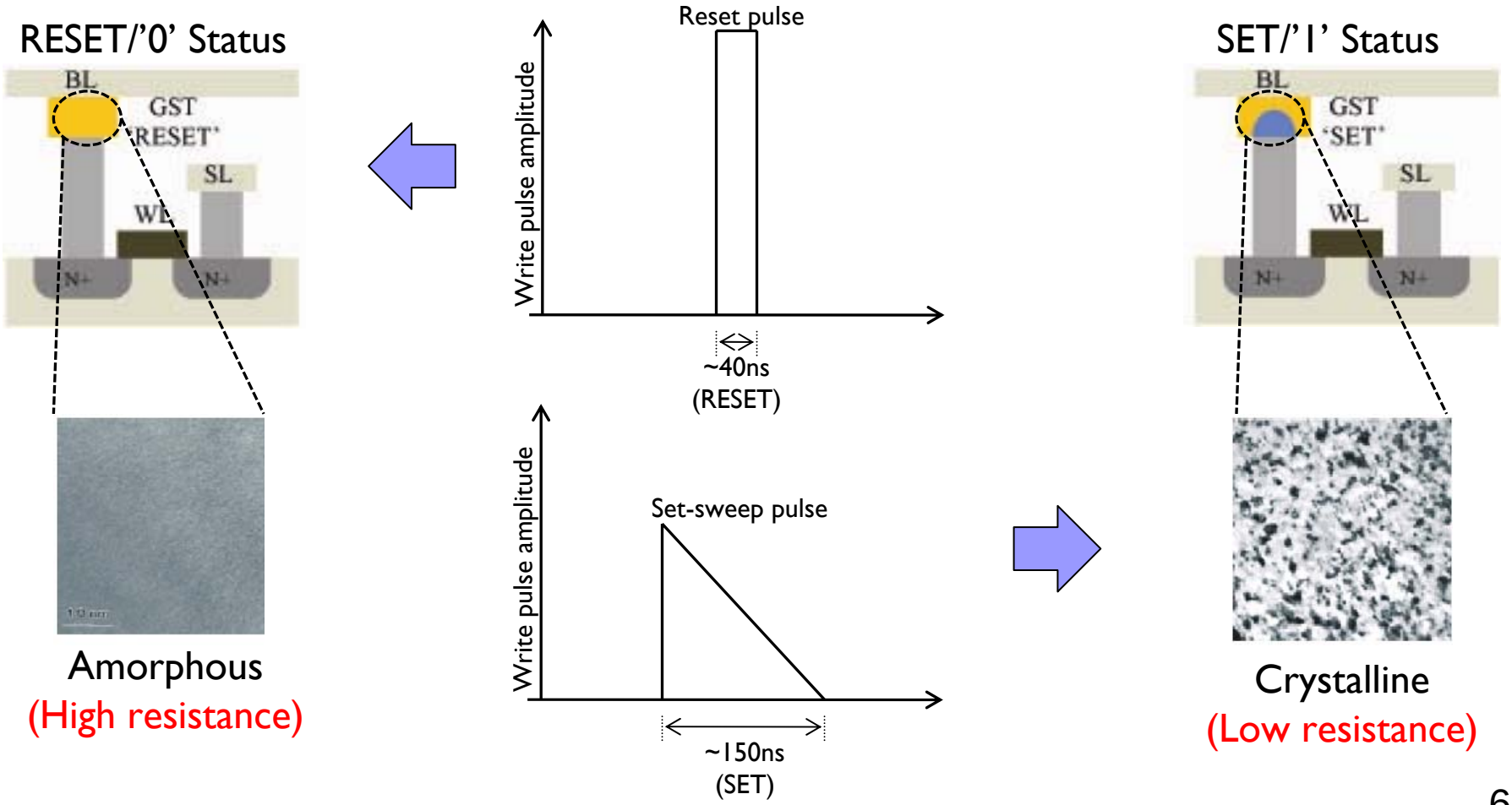
RESET/'0' Status SET/'1' Status

Equivalent circuit



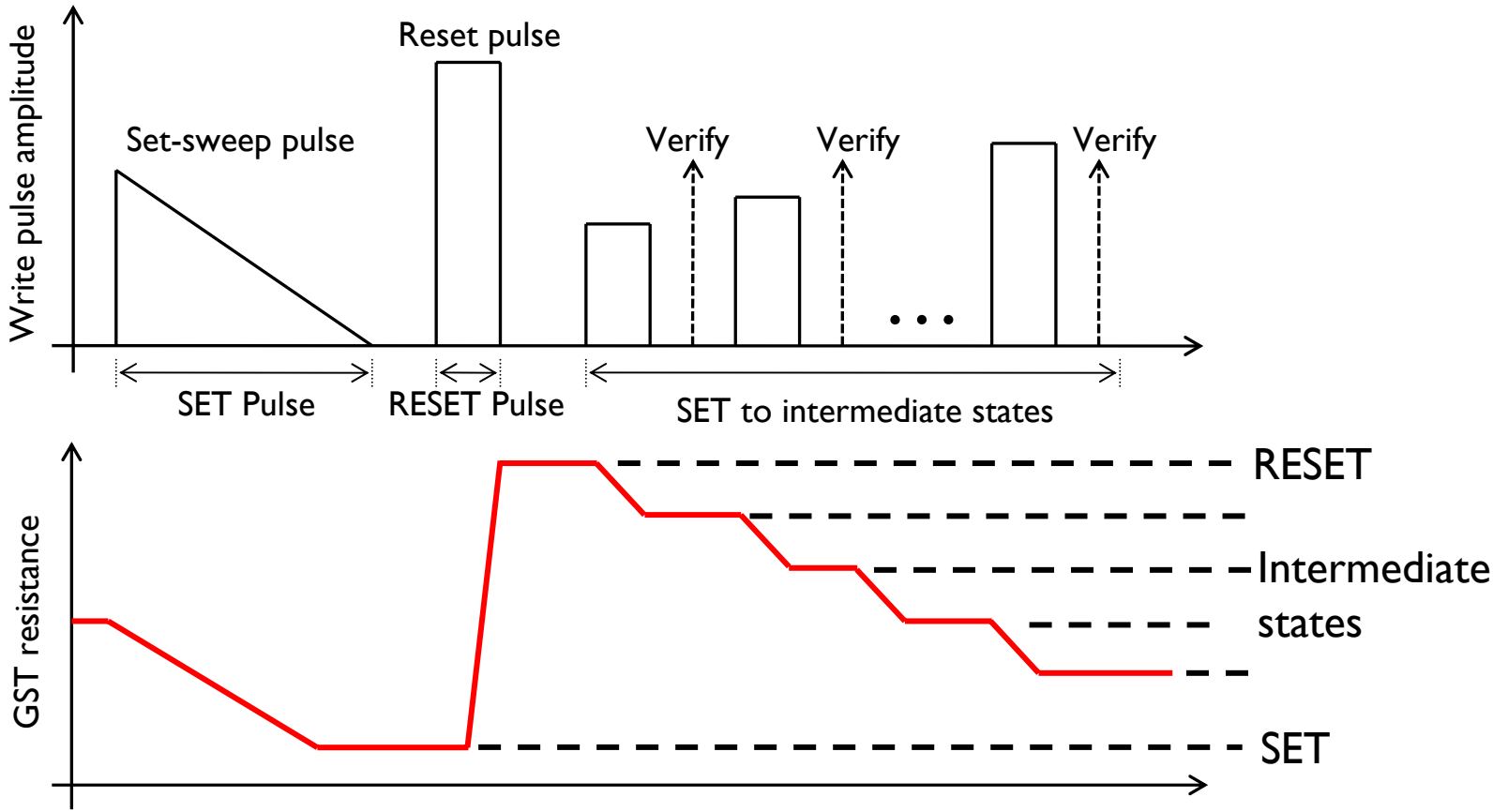
RESET/SET Operations of PCRAM

- Change status by applying heat (voltage, Joule heat)



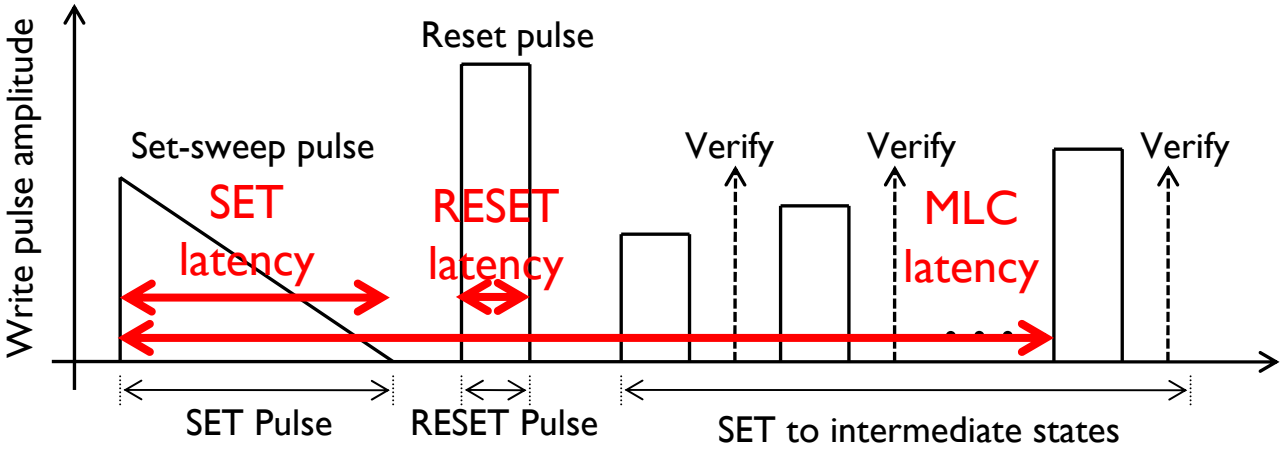
Multi-Level Cell

- Similar to NAND flash, PCRAM has the MLC capability
- Intermediate states between RESET and SET can be achieved by applying partial SET pulses.

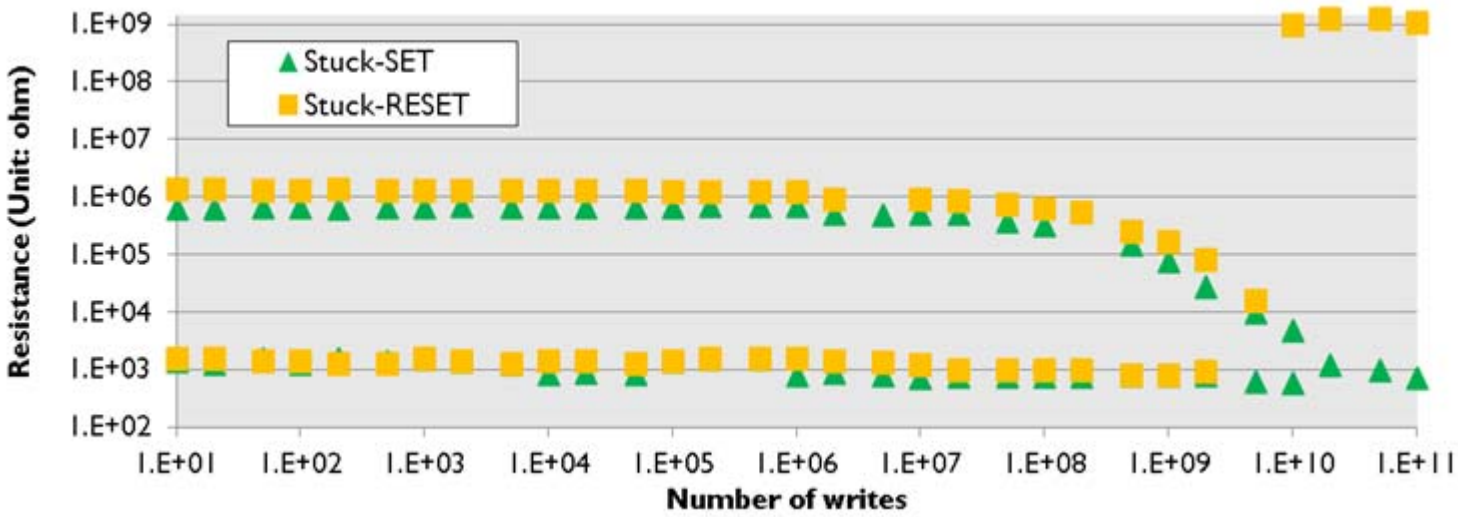


Multi-Level Cell

- MLC has performance overhead

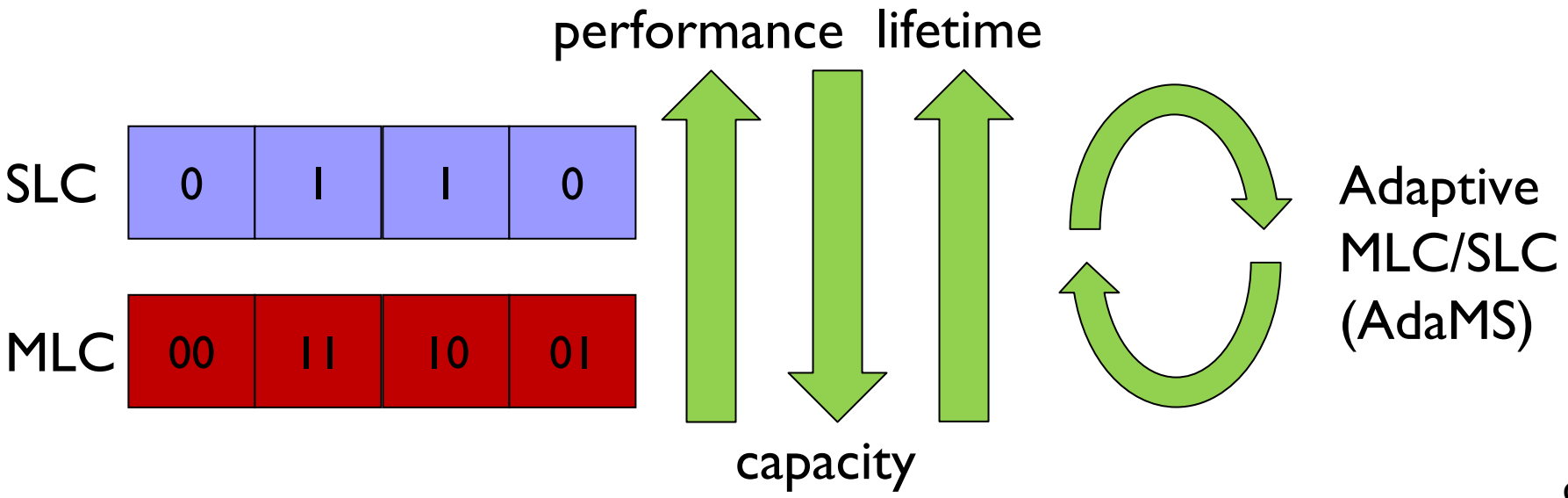


- MLC reduces PCRAM lifetime

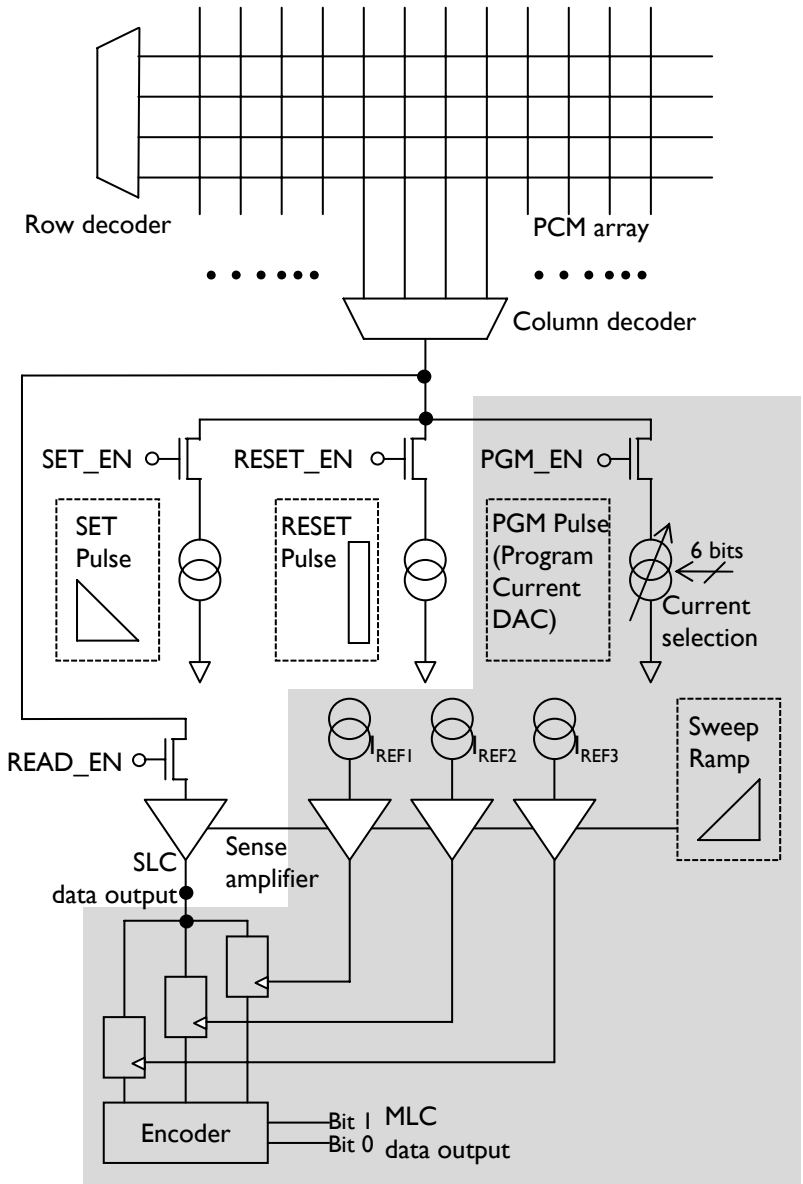


MLC Pros and Cons

- Pros
  - Increase capacity
- Cons
  - Increase write latency (multiple partial-RESET pulses)
  - Increase read latency (non-trivial sense amplifier)
  - Reduced lifetime



AdaMS: Hardware

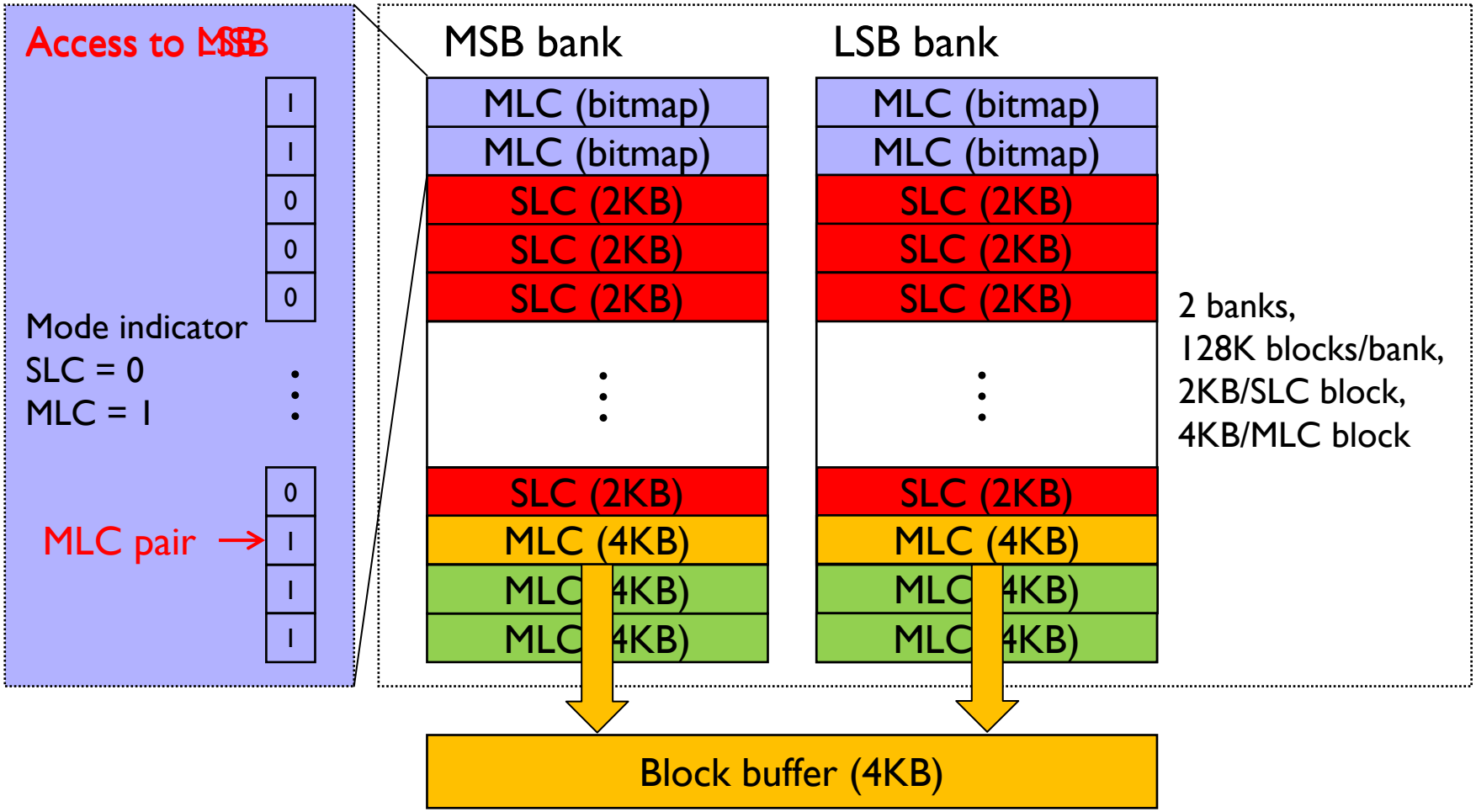


- No special hardware is needed to support AdaMS
- A MLC-aware PCRAM peripheral circuitry has the ability to access SLC

Shaded components are only used for MLC

AdaMS: Architecture

- AdaMS dynamically change PCRAM cells between MLC and SLC
- The total PCRAM capacity is a variable



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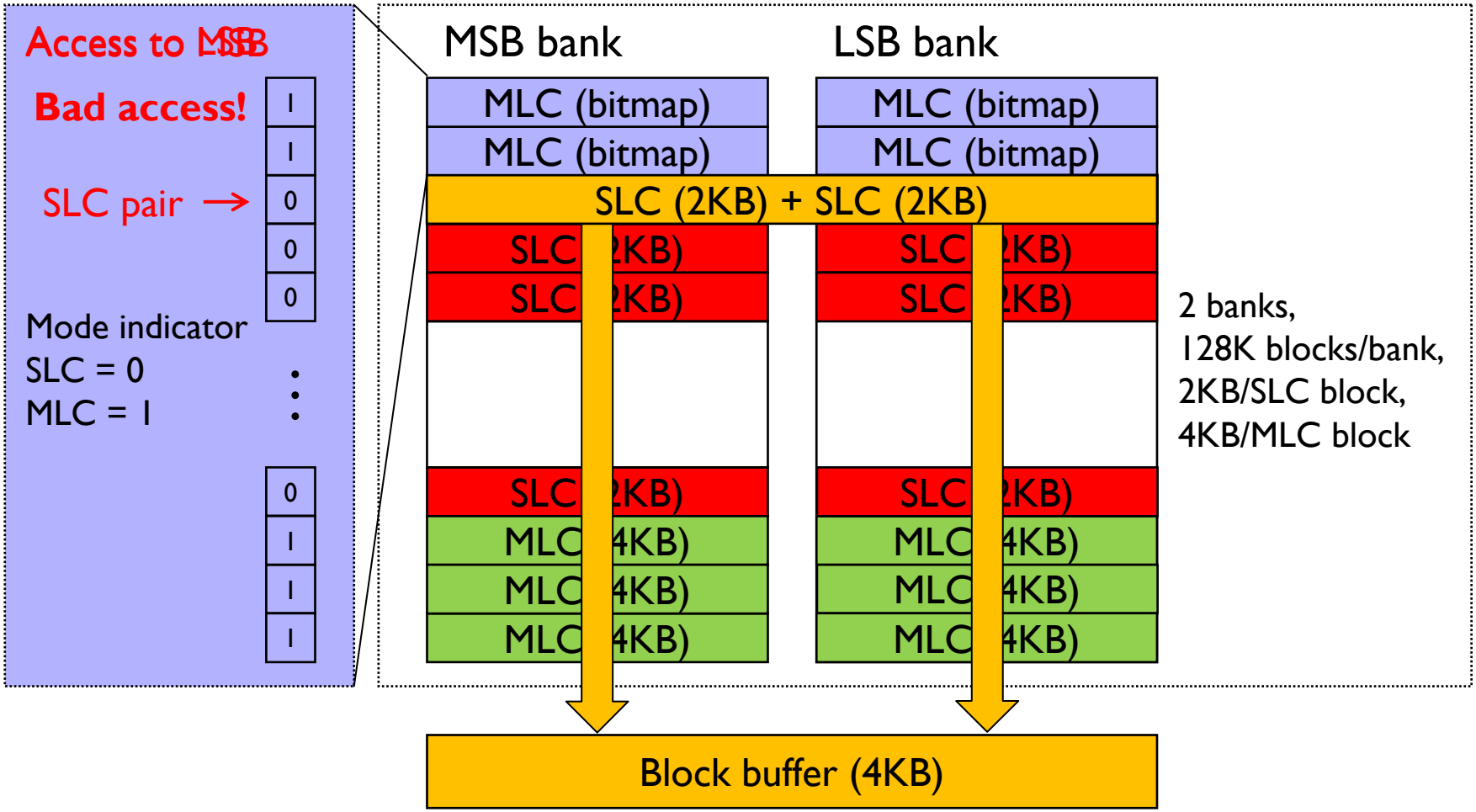
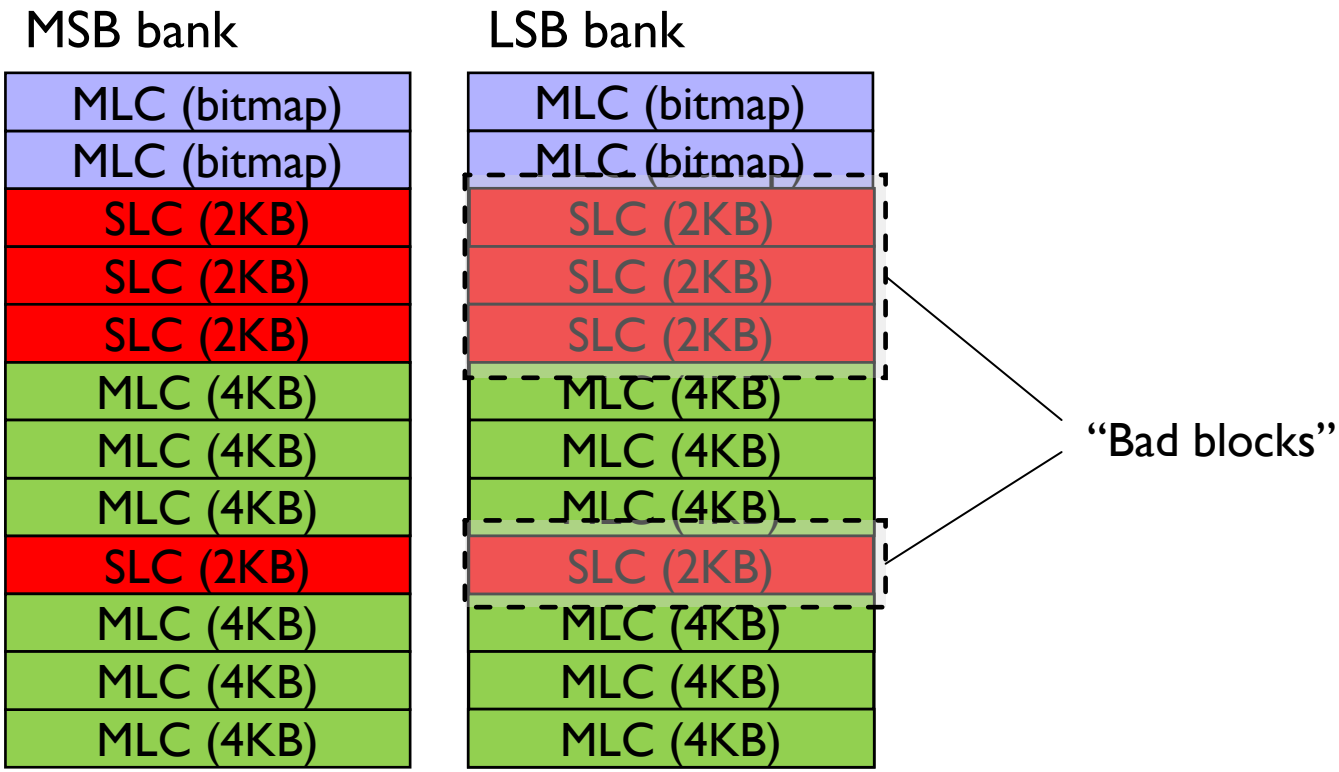


LSB Access in SLC Mode

- In SLC mode, all the LSB accesses are invalid and end up with a "bad block" signal
- File system (i.e. Ext2) uses "hidden file" to implement the "bad block list"
- When switching to MLC mode, those blocks are removed from the "bad block list"



Simulation Analysis

- Trace-based simulation
- 4 I/O traces
  - Synthetic
  - Financial 1
  - Financial 2
  - WebSearch
- PCRAM MLC and SLC parameters are from NVSim*

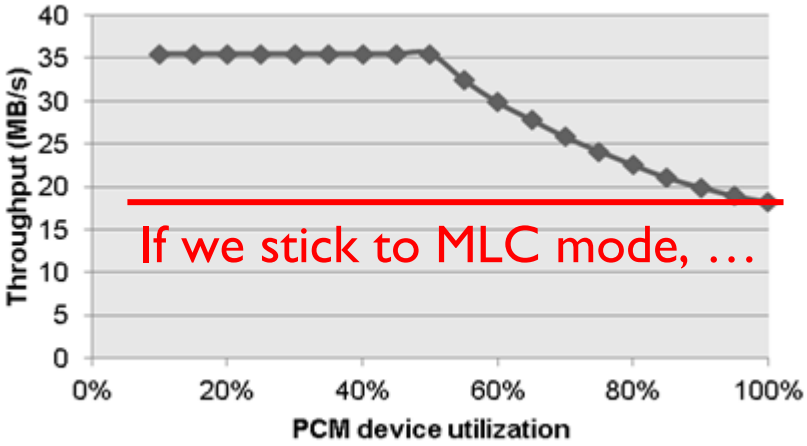
*NVSim is an ongoing project under the collaboration between PennState and HP Labs, which simulates the performance, energy, and area parameters of various non-volatile memory technologies.

Basic Assumptions

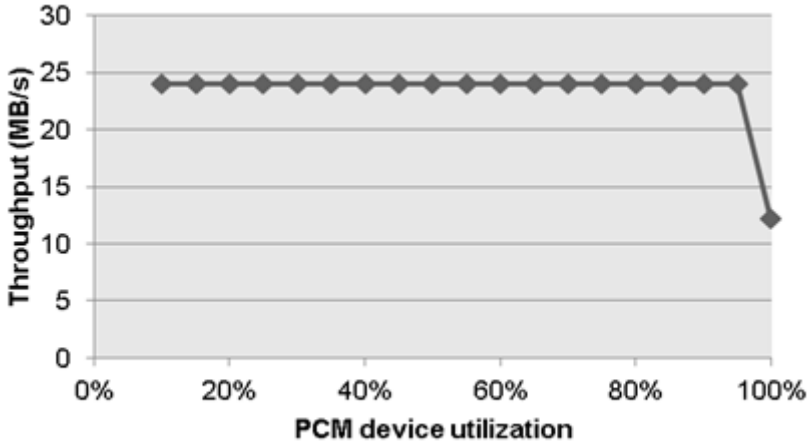
- 1. Assume our workload has peak storage capacity requirement of M
- 2. Our MLC PCRAM is 2-bit-per-cell
- 3. Our PCRAM chip array has M/2 cells in total
  - So, the total capacity is M, which meets the peak requirement
  - When it works in SLC mode, the capacity is M/2

- It means,
  - When the utilization is below 50%, we always use SLC mode because of its better performance
  - When the utilization is 100%, we have to use MLC mode

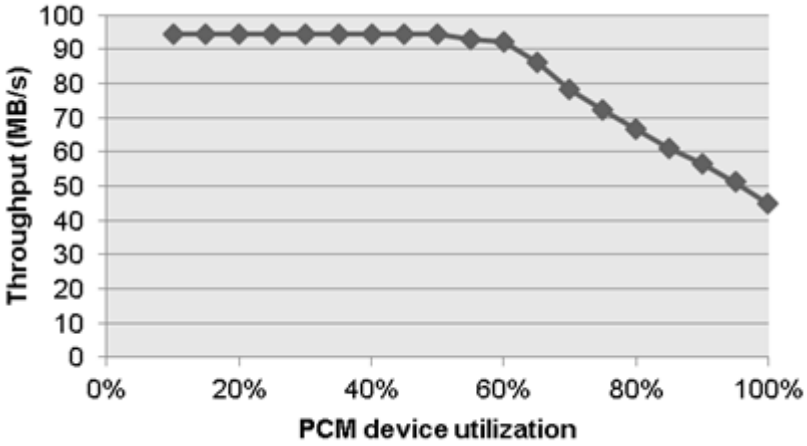
Utilization between 50% and 100%



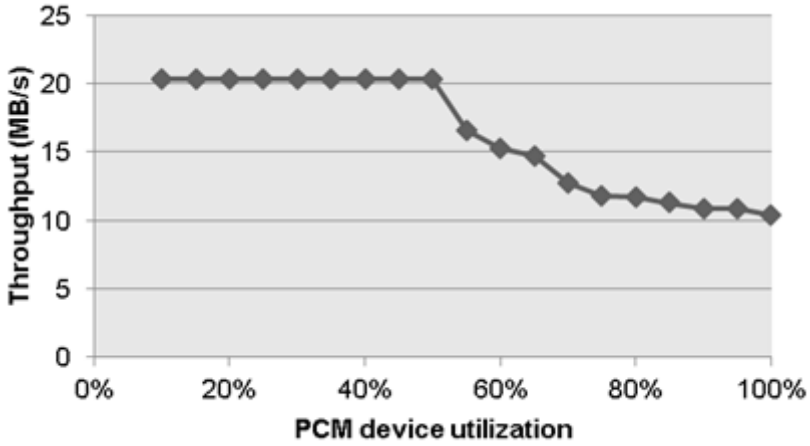
(a) Synthetic



(b) Financial 1



(c) Financial 2



(d) WebSearch

Conclusion

- AdaMS is easy to implement
  - Adaptive MLC/SLC control only needs minimal hardware change and a modified device software driver.
- AdaMS is useful
  - It improves the PCRAM performance when the storage utilization is below 100%, which is always true.

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Q&A