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1D-1

A H.264/MPEG-2 Dual Mode Video Decoder Chip Supporting Temporal/Spatial Scalable Video

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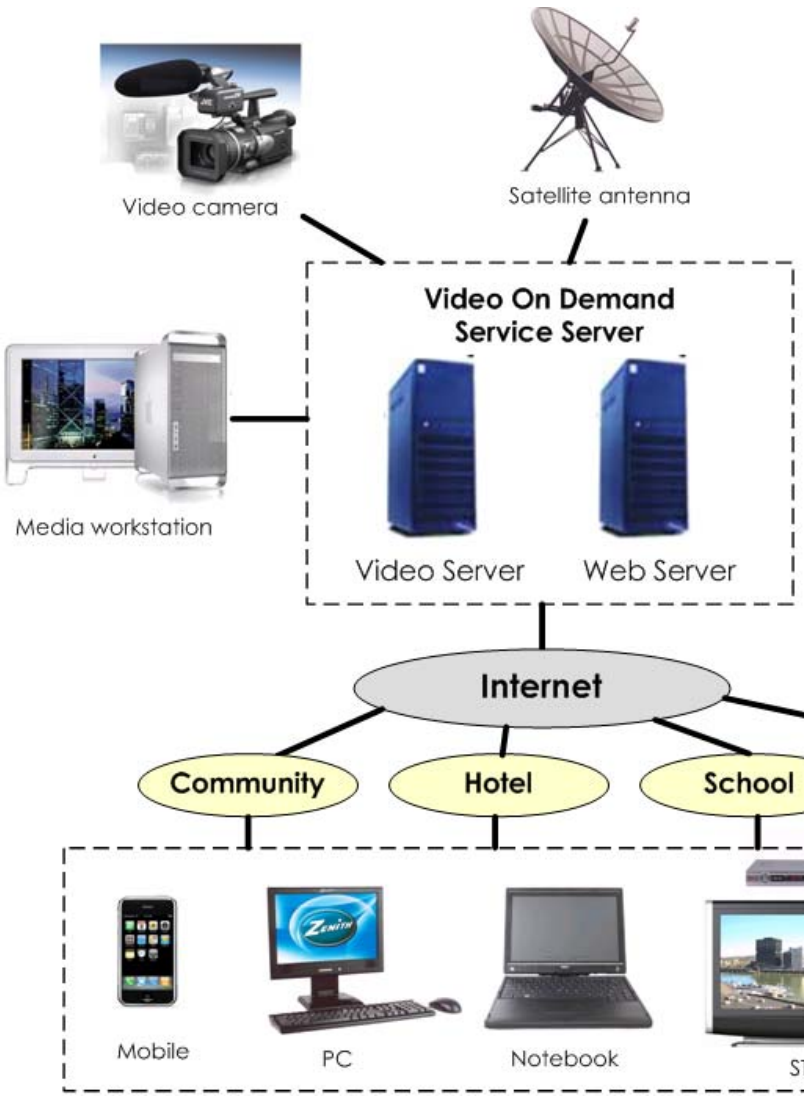
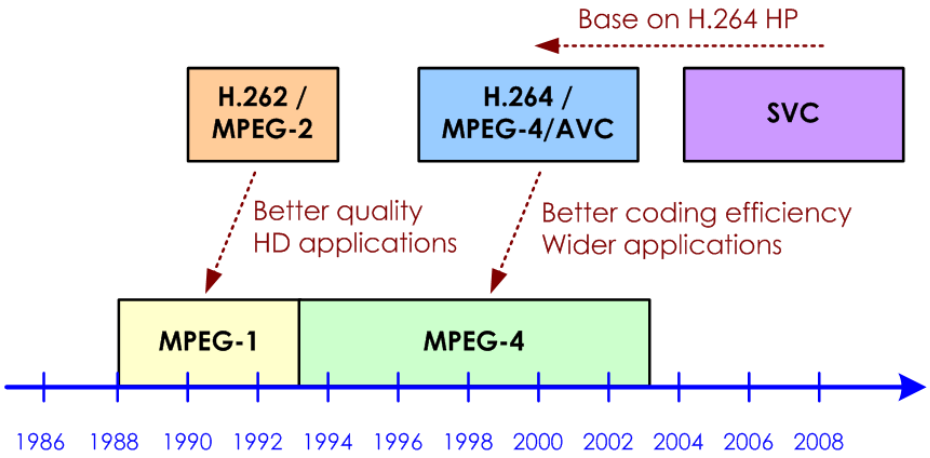
Introduction – Motivation

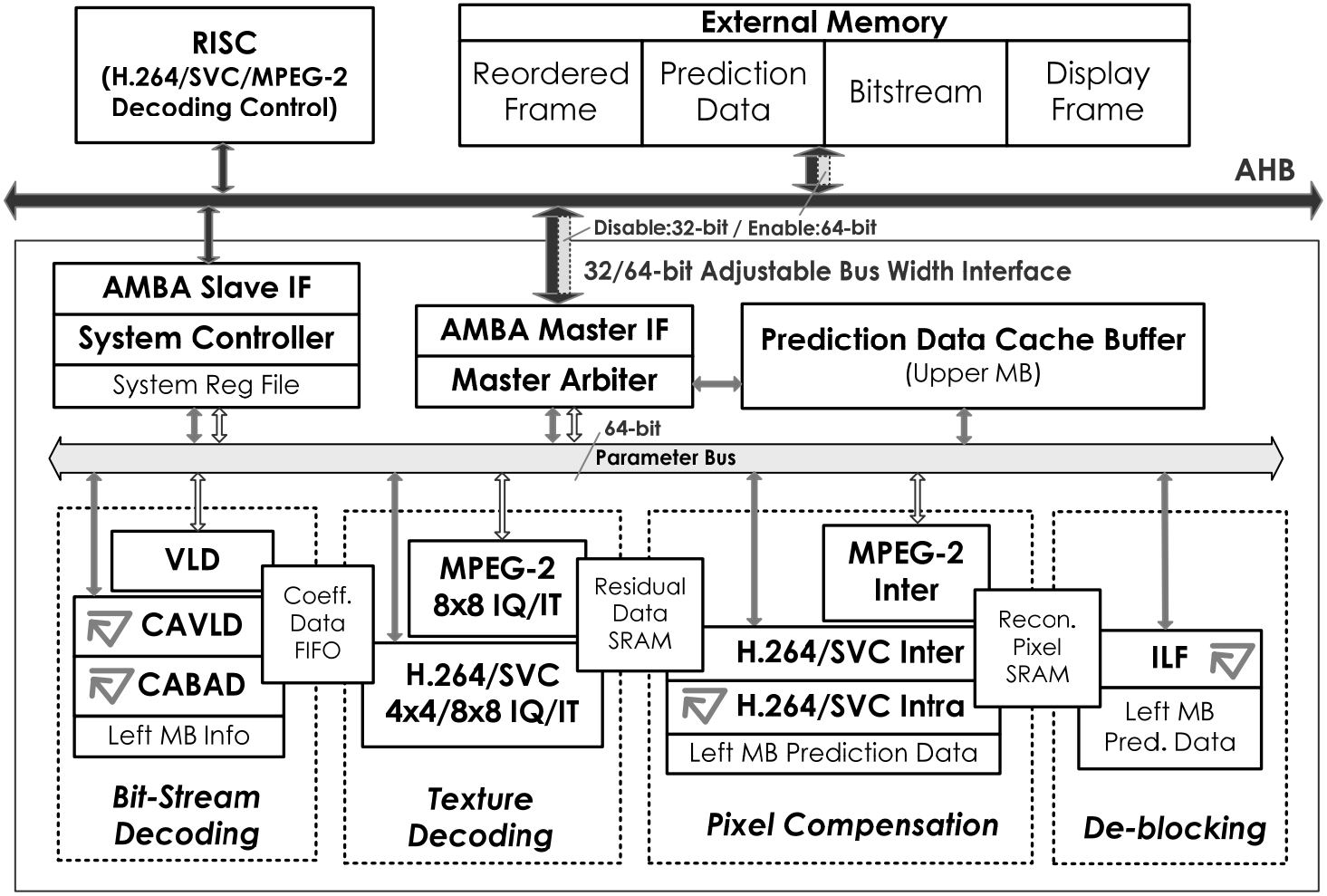




Video coding development history

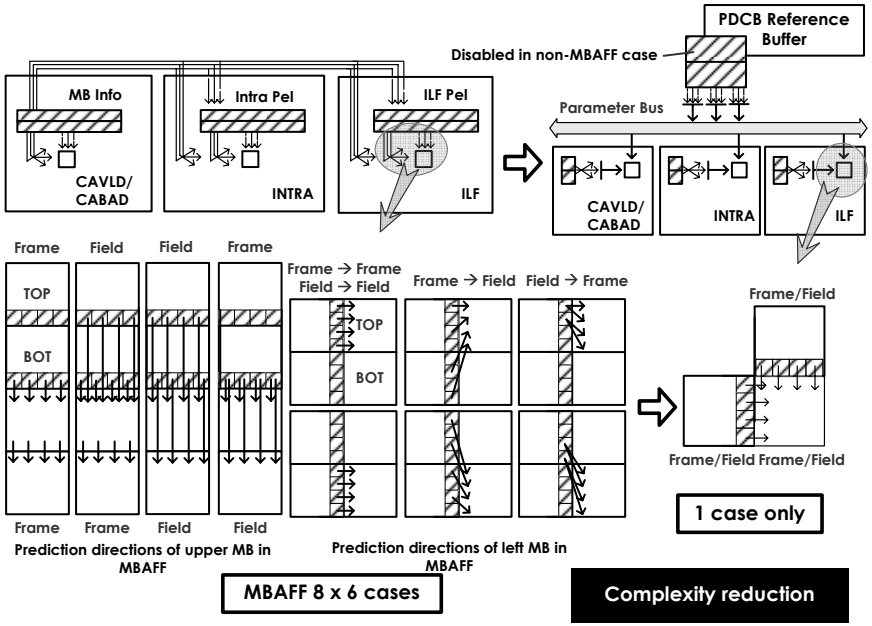
Dual Mode Video Decoder (H.264 HP/MPEG-2 MP) Supporting Temporal/Spatial Scalable Video (SBP mode 0)

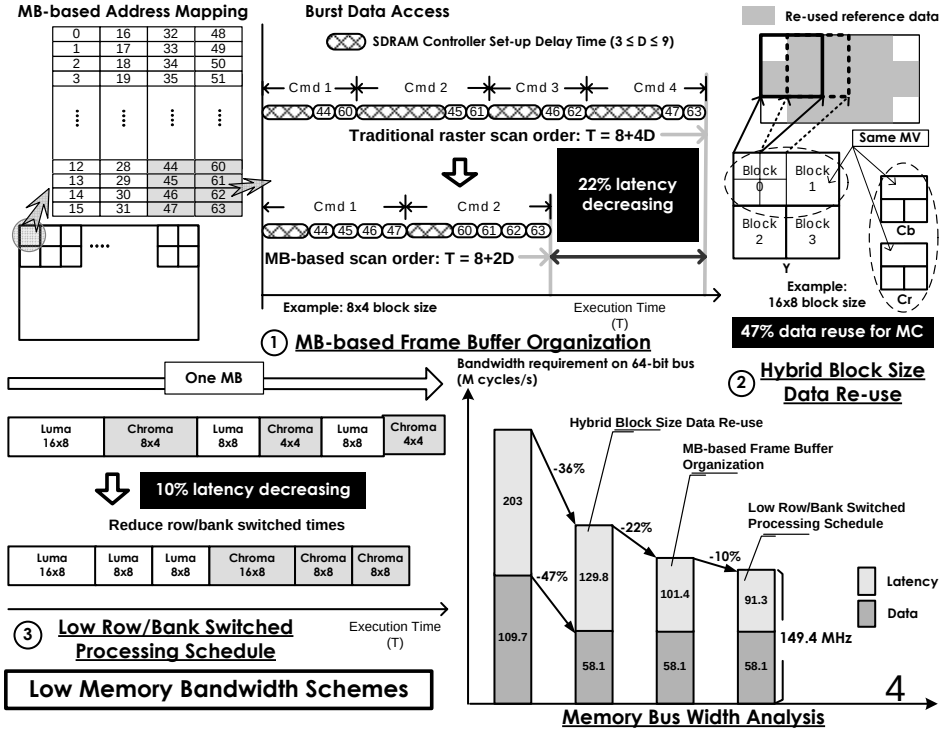
Proposed Design – System Architecture



Proposed Techniques - System Level Optimization

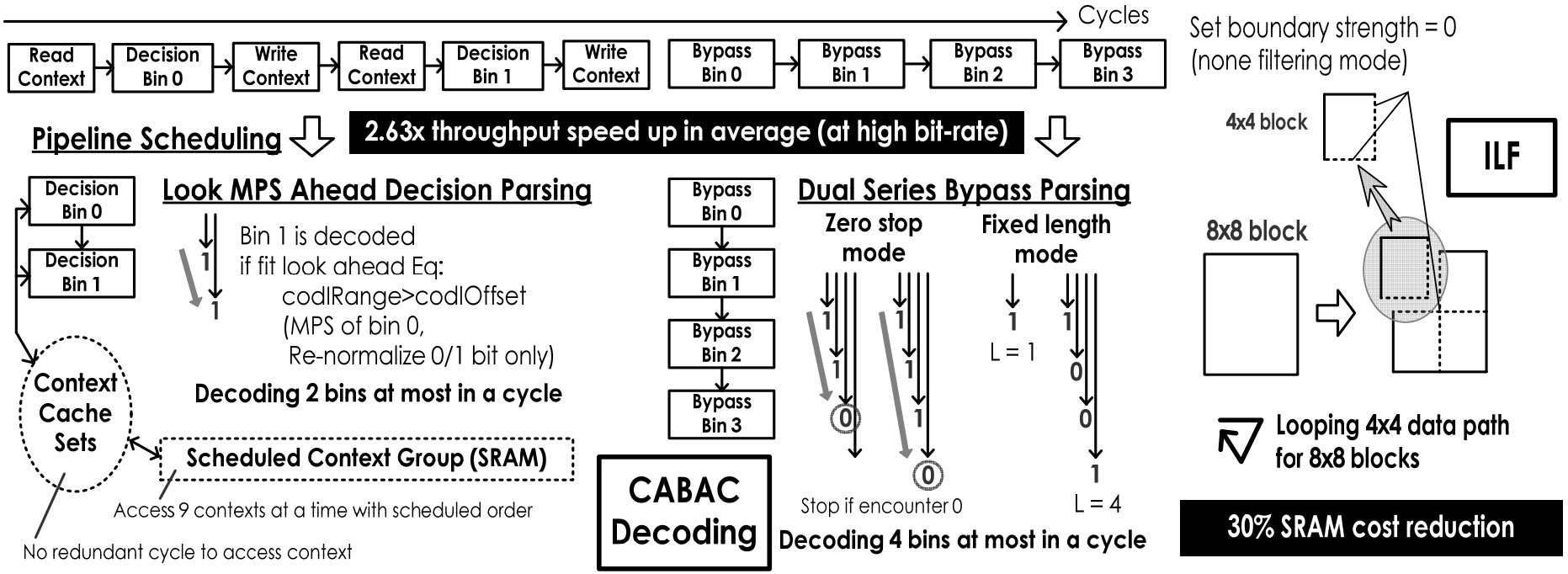
- ***Central Dispatching Prediction Data Management***
  - Control complexity reduction
- ***Low Memory Bandwidth Schemes***
  - MB-based frame buffer organization
  - Hybrid block size data reuse
  - Low row/bank switched processing schedule



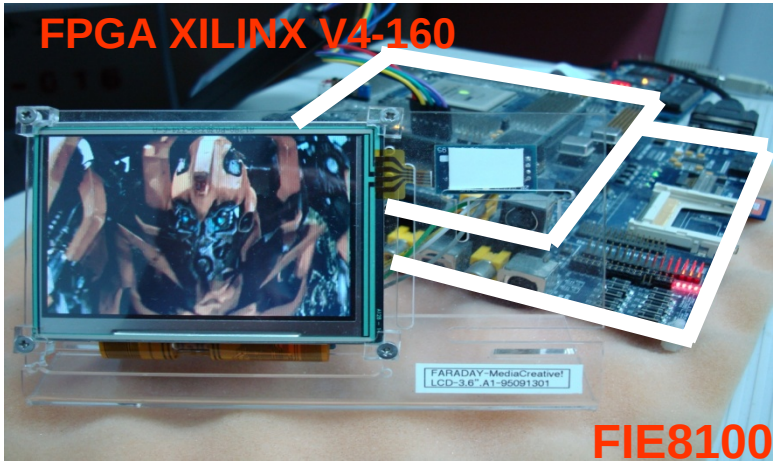


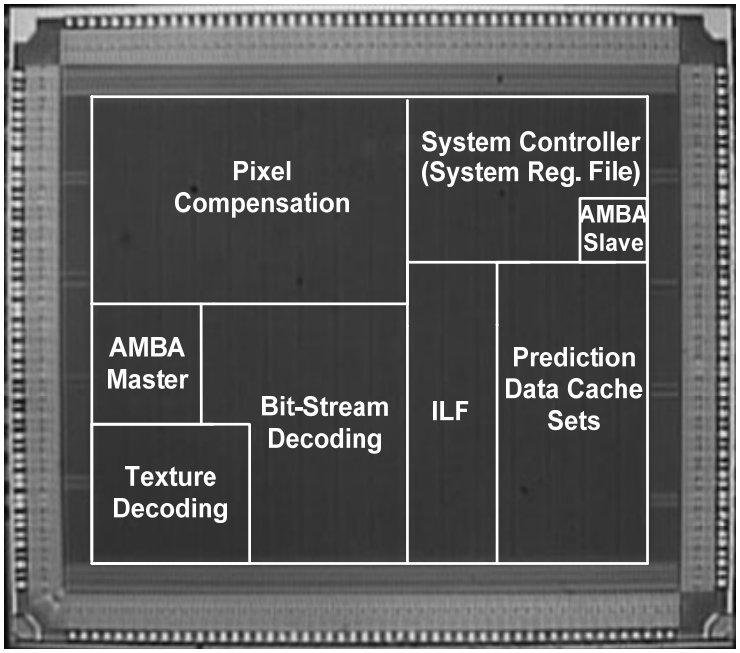
Proposed Techniques - Component Level Optimization

- **High Throughput CABAC Decoding**
- **Hybrid Block(4x4/8x8) Data Reuse**
  - In-loop deblocking filter



FPGA & Chip Implementation





•Supporting Scalability

Designs	Proposed Design
Specification	MPEG-2 MP
	H.264 HP
	SVC SBP (5-level)
	1920 x 1088
Gate Count	439K
SRAM Size	10.9KB
Clock Rate	150 MHz (H.264, HD1080@30fps) 163 MHz (SVC, HD1080@20fps)
SDRAM Bus	Single SDR 32/64-bit adjustable bus
Technology	0.13μm
Power	328mW (HD1080)