

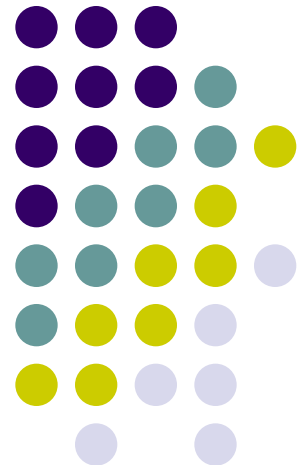
Design and Chip Implementation of a Heterogeneous Multi-core DSP

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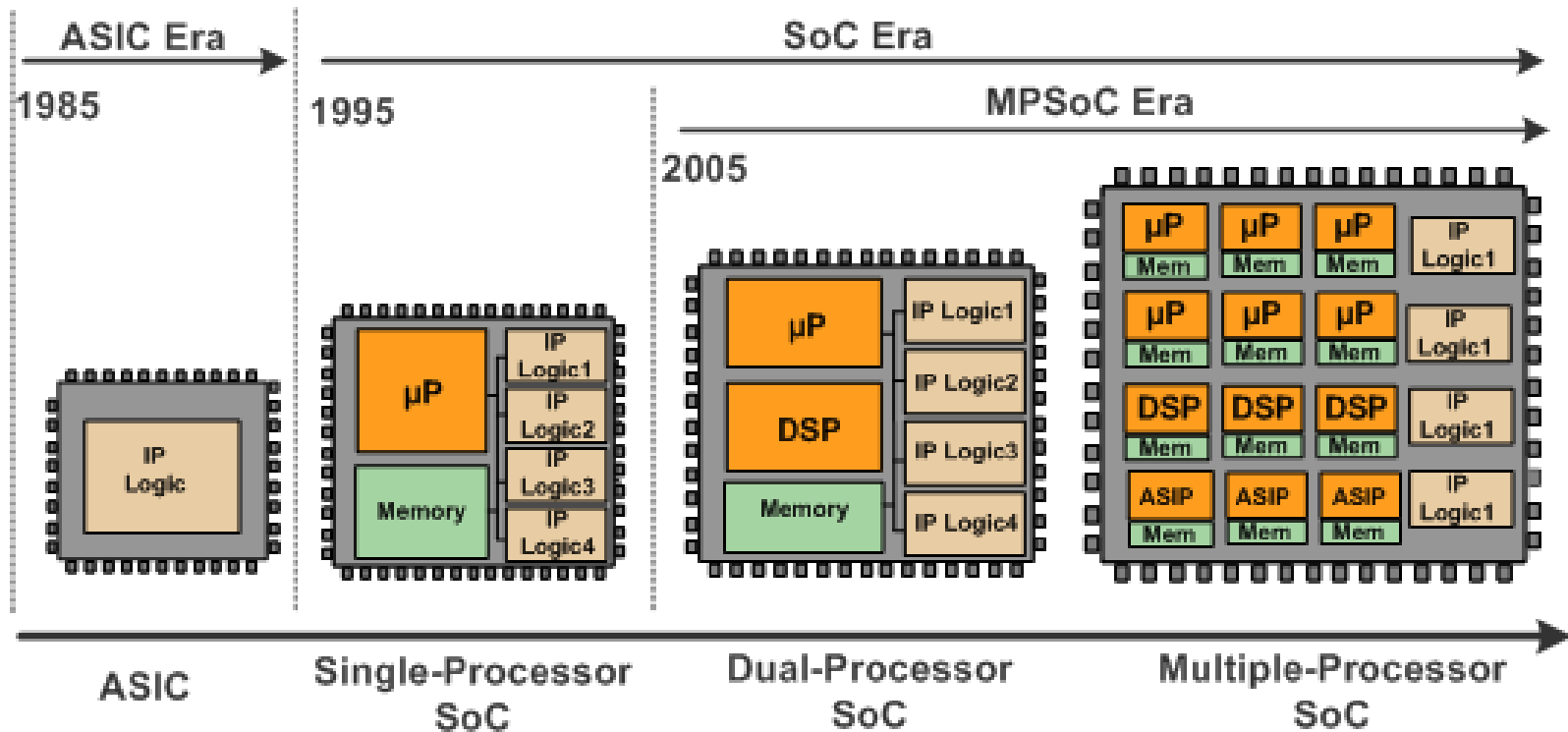
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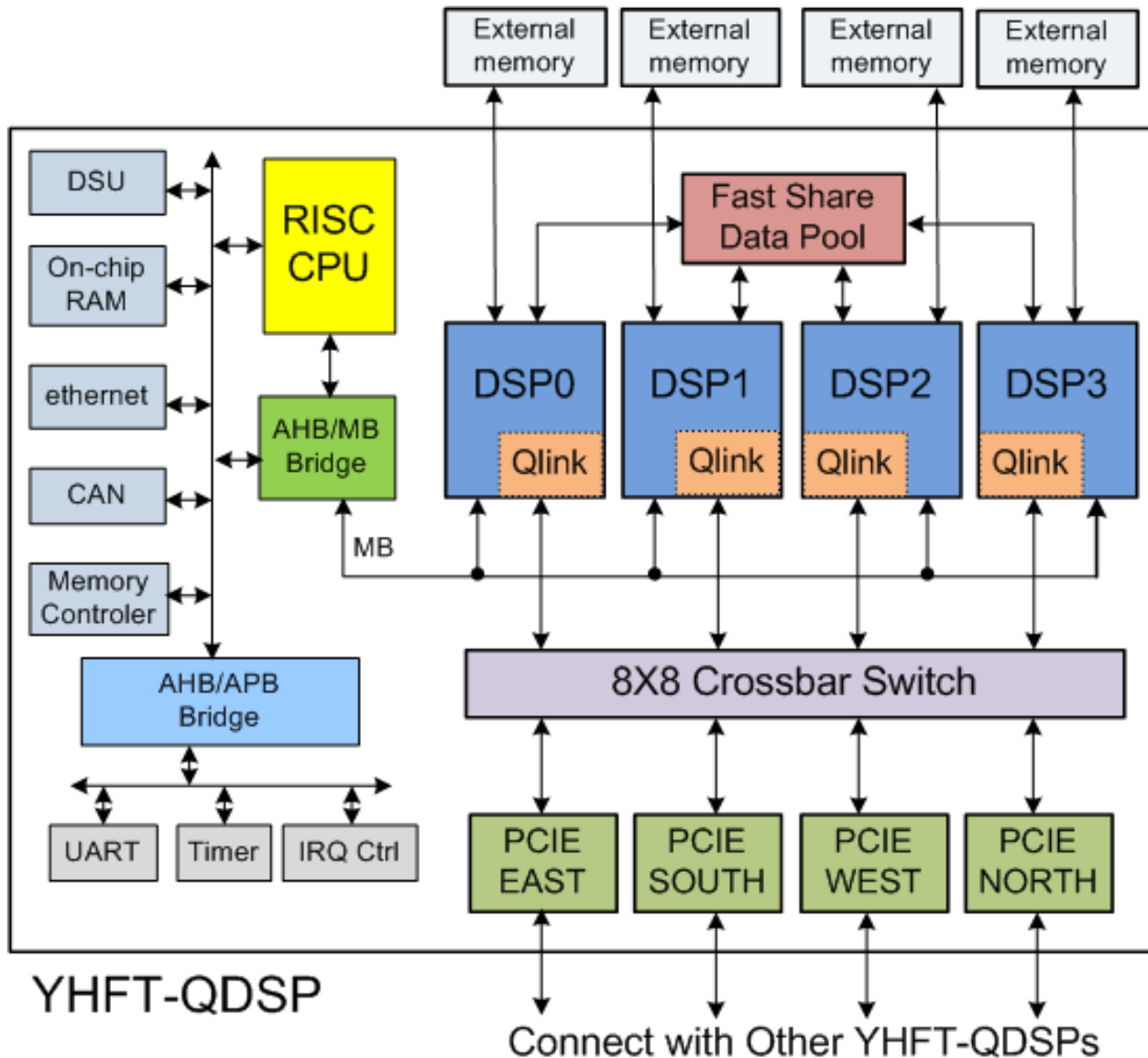


Trend of System-on-Chips (SoCs)



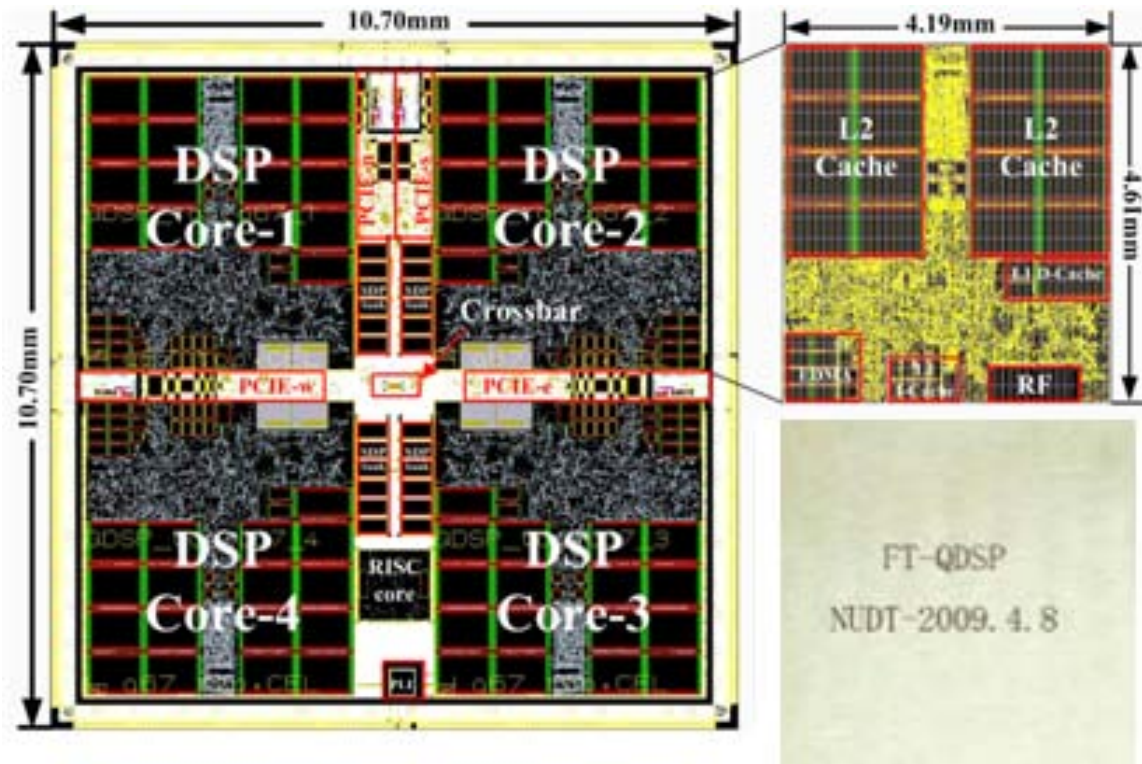
Evolution of processor chips

YHFT-QDSP: a heterogeneous multi-core Digital Signal Processor



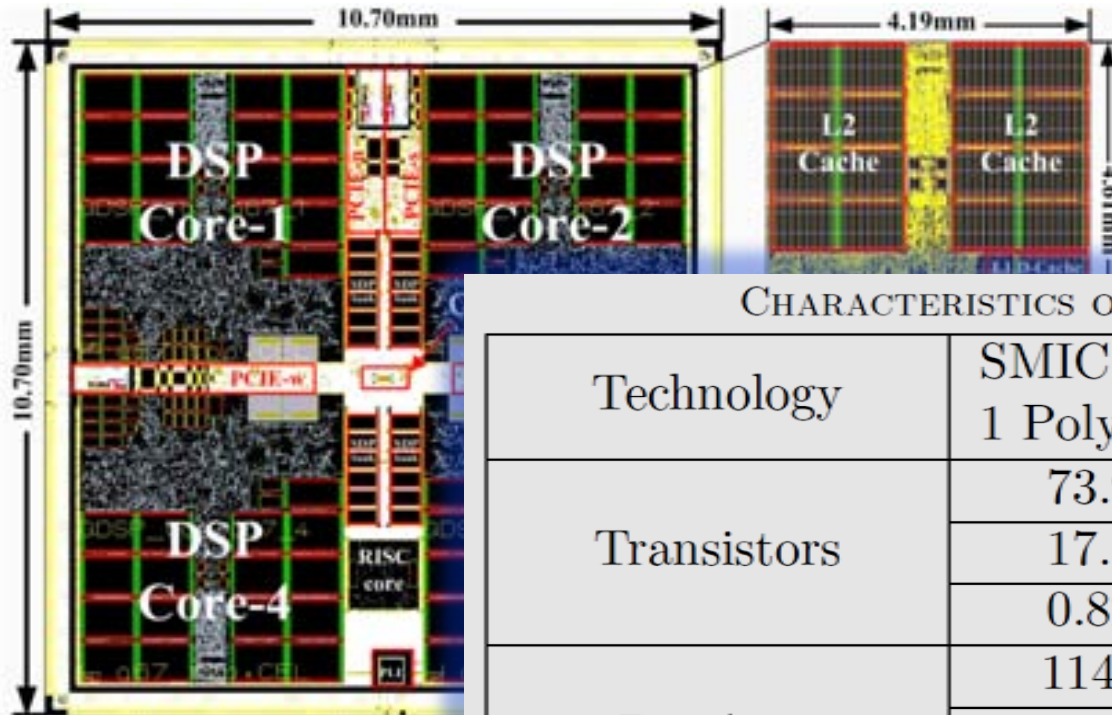
- A RISC CPU core
- Four enhanced YHFT-DSP/700 cores
- several peripherals
- individual memory interfaces
- Three kinds of communication
 - AHB/MB Bridge
 - Fast Shared Data Pool (FSDP)
 - Qlink-Crossbar-PCIE mechanism

Chip Implementation of YHFT-DSP



micrograph of YHFT-QDSP

Chip Implementation of YHFT-DSP

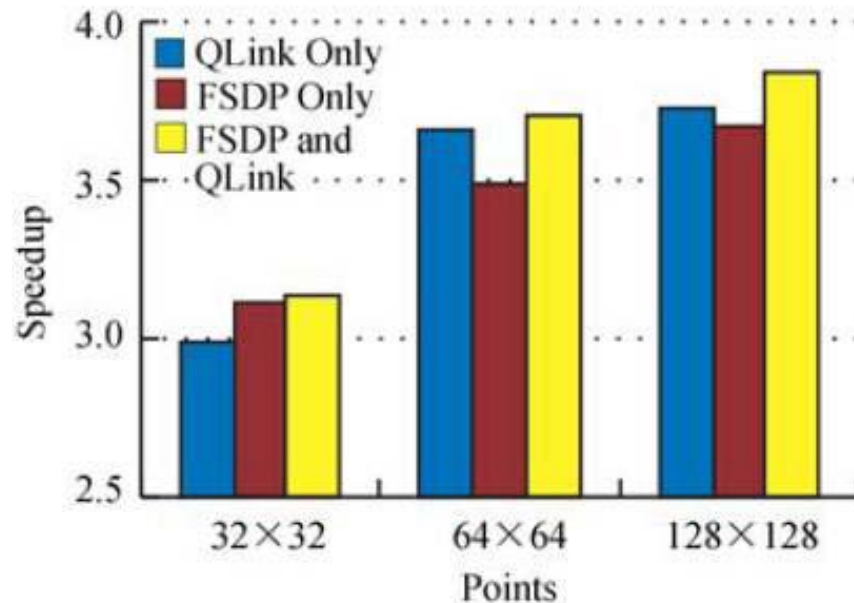


CHARACTERISTICS OF THE YHFT-QDSP

| | |
|-------------------|---|
| Technology | SMIC 130nm LVT CMOS, 1 Poly, 8 Metals (Cu) |
| Transistors | 73.9 million (YHFT-QDSP) |
| | 17.1 million (DSP core) |
| | 0.82 million (CPU core) |
| Die Area | 114.49 mm ² (YHFT-QDSP) |
| | 19.32 mm ² (DSP core) |
| | 1.29 mm ² (CPU core) |
| Clock Frequency | 350MHz@1.2V (DSP core) |
| | 200MHz@1.2V (CPU core) |
| Power Dissipation | 2.99W@1.2V (YHFT-QDSP) |

Performance Evaluation of YHFT-DSP

2D FFT benchmark



- ◆ When the data size is relatively small, e.g. 32x32 points, data transfer by the FSDP is faster than by the QLink.
- ◆ As the data size is larger, data transfer by the QLink is faster.
- ◆ As we can see, using the FSDP and the QLink together obtains the best speedups.