1D-12
Design and Evaluation of Variable Stages Pipeline (VSP) Processor Chip

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Battery life is a problem for mobile computers

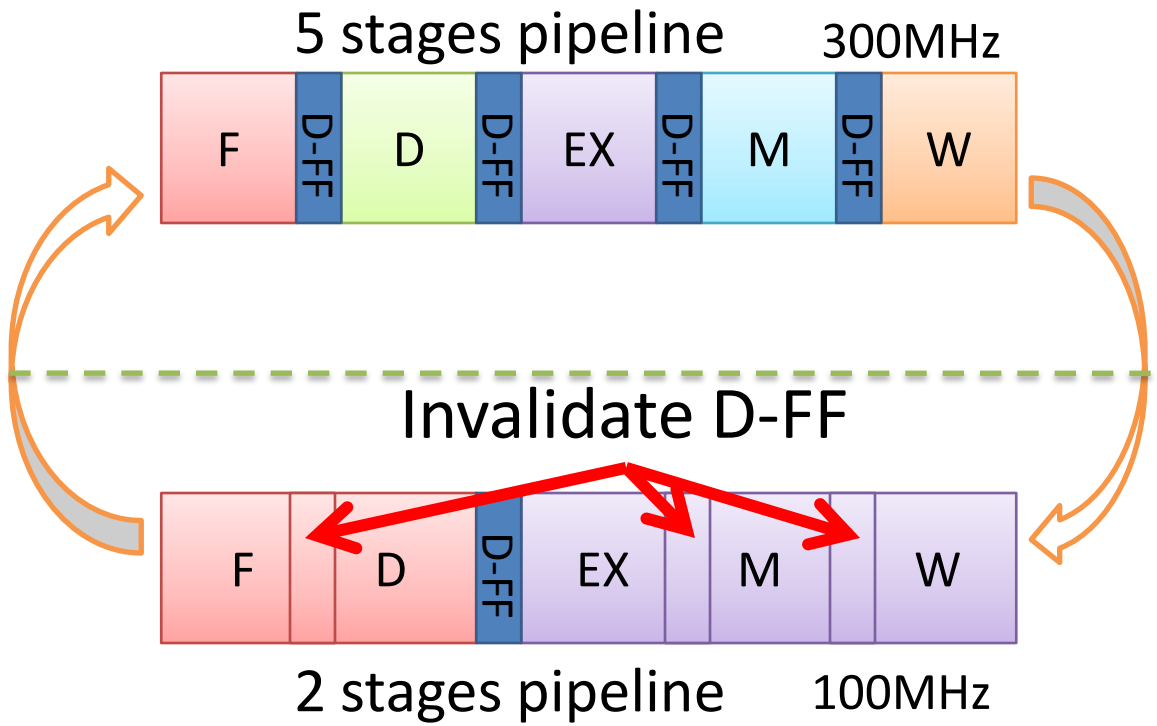
- Mobile computers are required to achieve both **Low energy** and **High performance**.

We propose low energy processor architecture

VSP (Variable Stages Pipeline)

High Speed (HS) mode
- Deep (super) pipeline
- High frequency
- **High performance**
- **High energy**

Low Energy (LE) mode
- Short pipeline
- Low frequency
- **Low performance**
- **Low energy**



Vary the pipeline depth dynamically.

Glitch propagation becomes serious problem.

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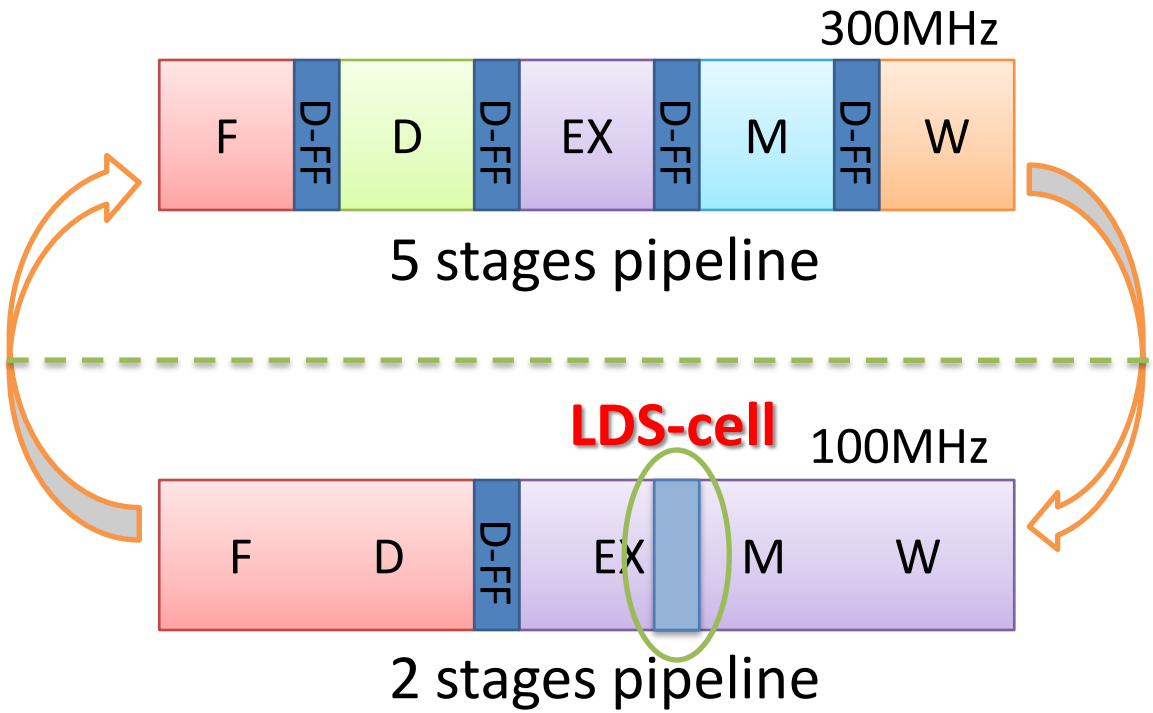
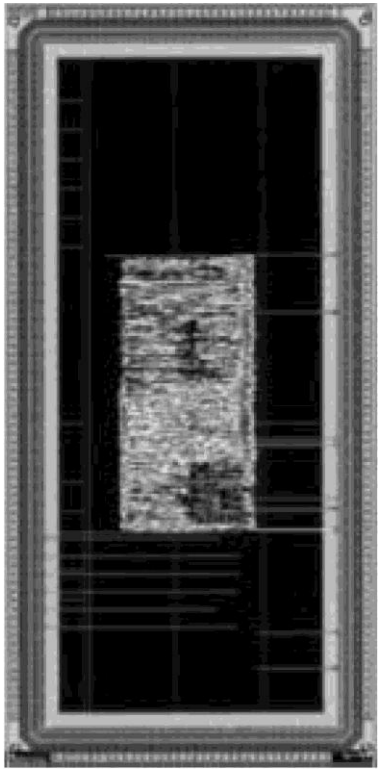


Vary the pipeline depth dynamically.

LDS-cell **prevent glitch propagation.**

LSI Design

Technology	ROHM0.18μm CMOS process
Standard cell library	VDEC Kyoto University Library
Chip size	2.5 × 5.0 mm^2
Measure energy	HP83000 LSI tester



	HS mode	LE mode
Instruction set architecture	MIPS R3000	
Pipeline depth	9 stages	3 stages
Target frequency	100 MHz	25 MHz

	VSP
Number of transistor	521,971

VSP can reduce 13% energy than conventional approach.