A 58-63.6GHz Quadrature PLL Frequency Synthesizer Using Dual-Injection Technique

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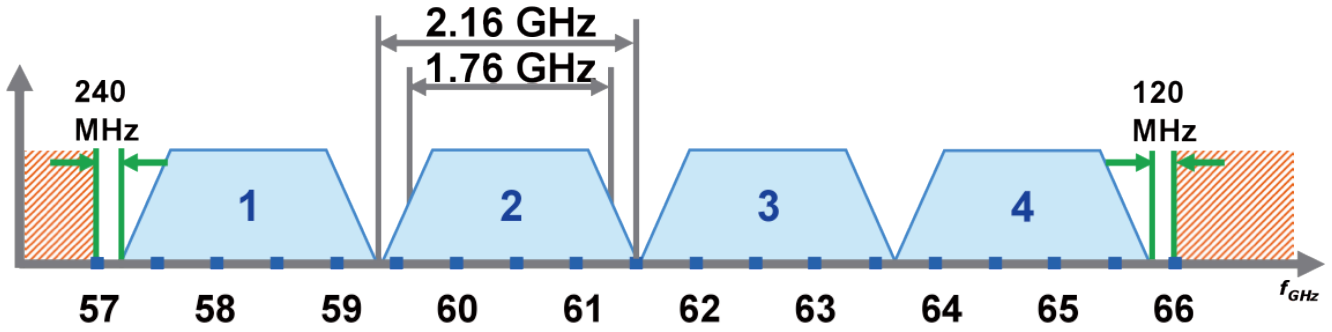
60GHz Communications

- 9 GHz unlicensed band at 60 GHz
- Several Gbps transfer rate speed
  - 3.5Gbps/ch (QPSK)
  - 7Gbps/ch (16QAM)

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (GHz)	Roll-Off Factor
A1	57.24	58.32	59.40	1.76	0.25
A2	59.40	60.48	61.56	1.76	0.25
A3	61.56	62.64	63.72	1.76	0.25
A4	63.72	64.80	65.88	1.76	0.25

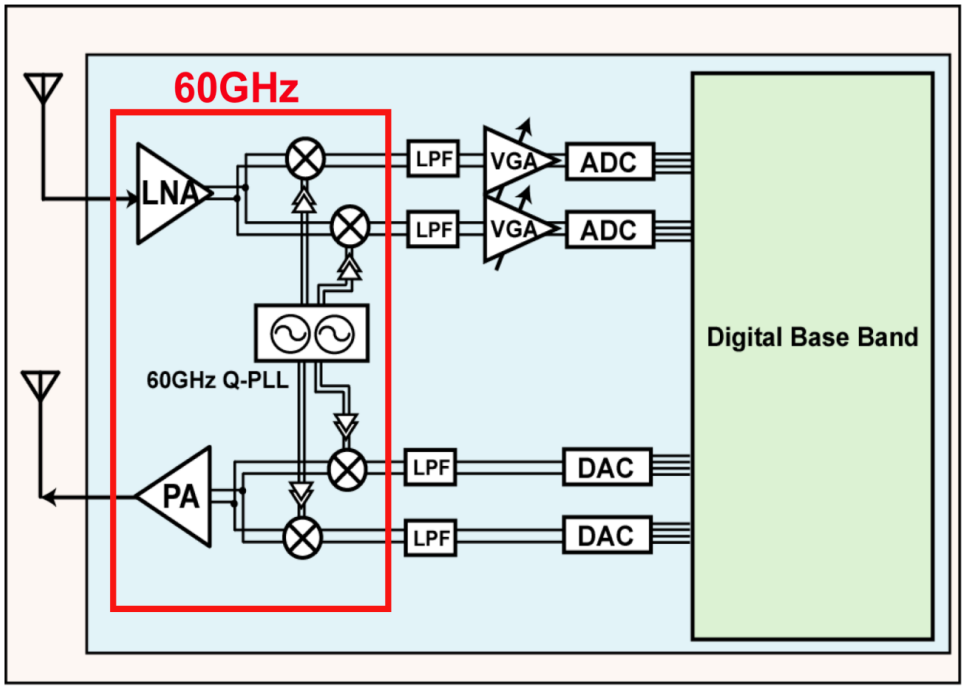


IEEE802.15.3c Specifications

from IEEE802.15.3c-2009

Transceiver Architecture

- **Direct conversion architecture for single chip implementation**
  - **Small area**
  - **Lower power consumption**



Single chip implementation

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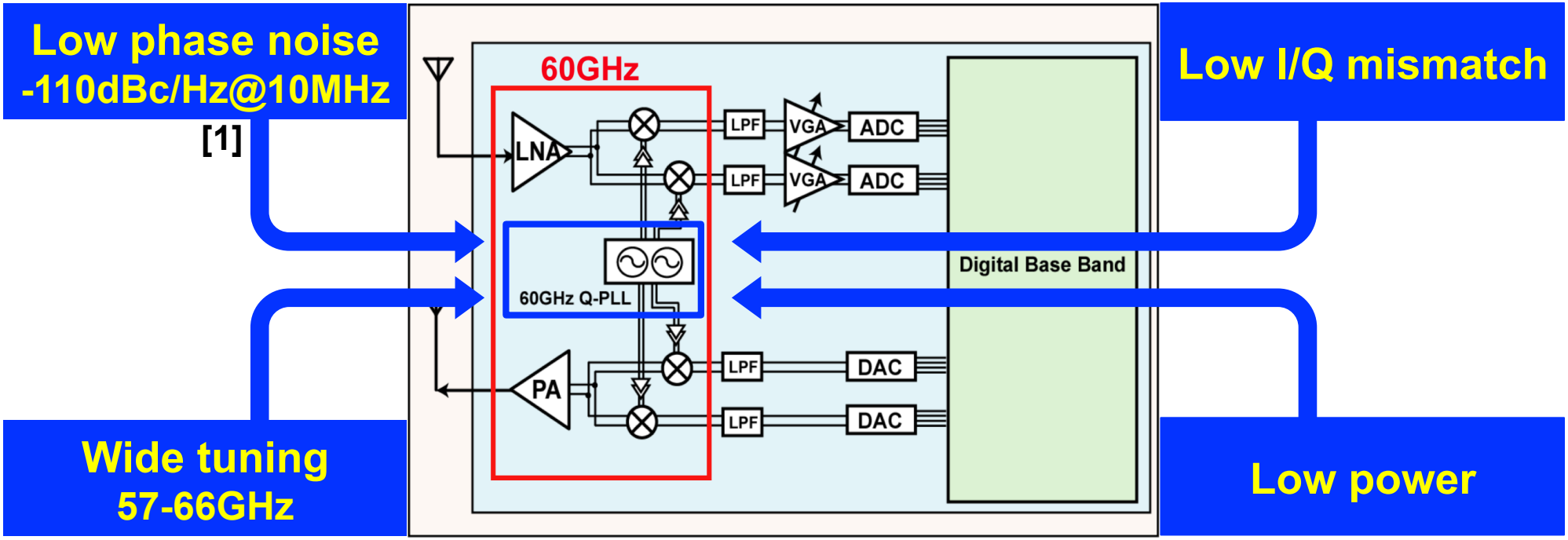


Single chip implementation

[1] Brian A. Floyd, JSSC 2008

LO Topologies

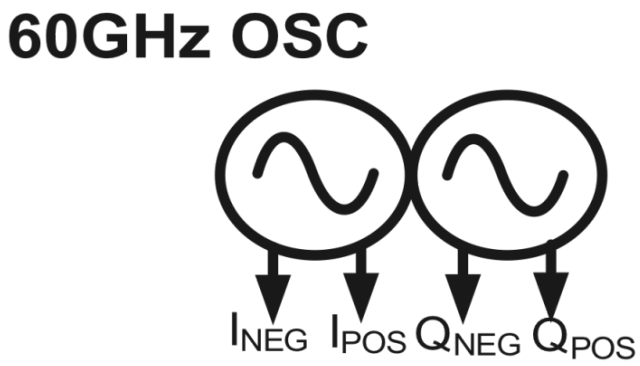
- 60GHz QPLL
  - 9GHz tuning range
  - Low Q for capacitors

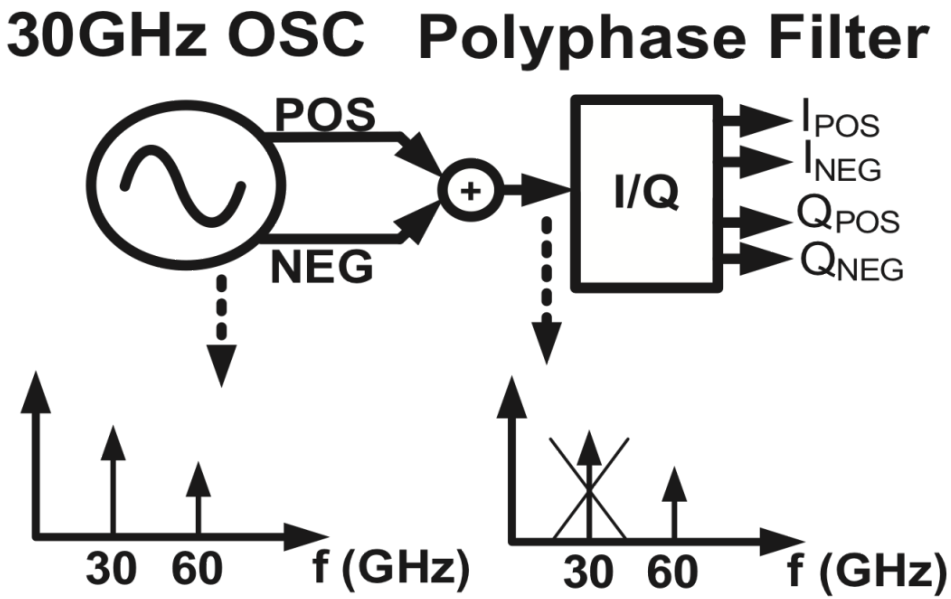
  Poor Phase Noise

- 30GHz PLL
  - 2nd harmonic is utilized
  - Polyphase filter is used

  High power consumption

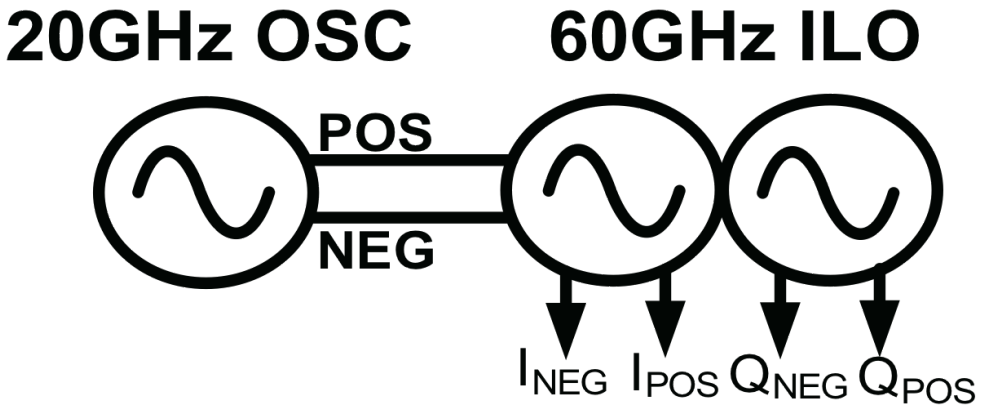
  I/Q mismatch





Proposed Architecture

- 20GHz PLL + Injection Locked Oscillator
  - Good tradeoff between phase noise & locking range
  - Tail feedback VCO [2]
  - Proposed dual Injection ILO



- 21dB improvement in phase noise (-96dBc/Hz@1MHz)
- 7Gbps wireless transfer rate using (16QAM)

[2] S. Hara and al., VLSI 2010