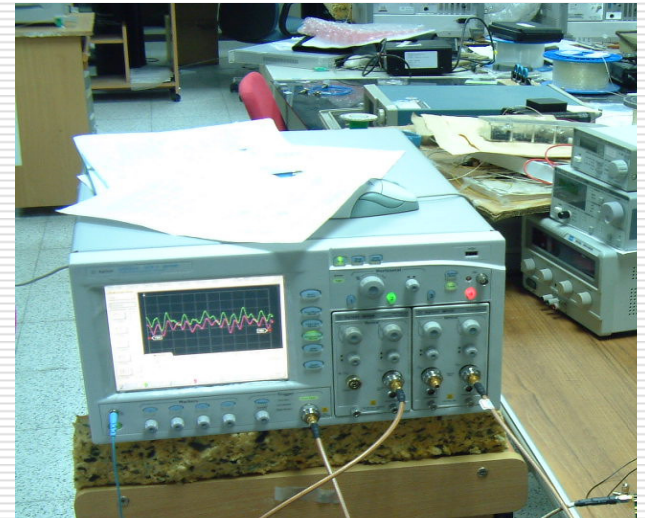
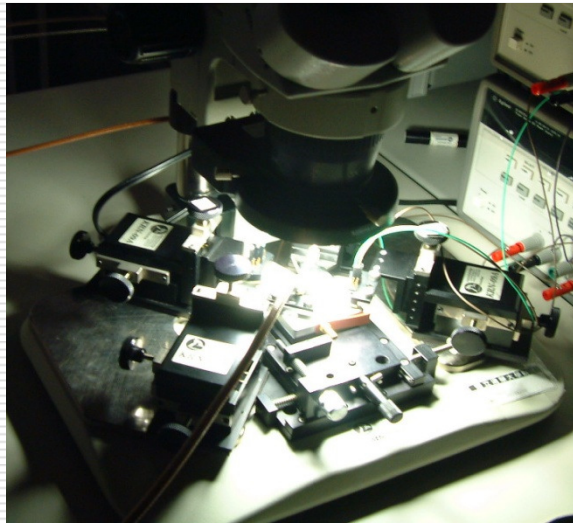
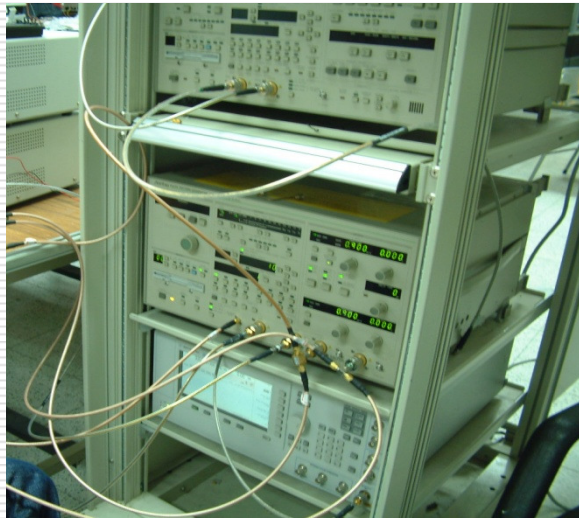


A 32Gbps Low Propagation Delay 4x4 Switch IC for Feedback-Based System in 0.13 μm CMOS Technology

1D-17



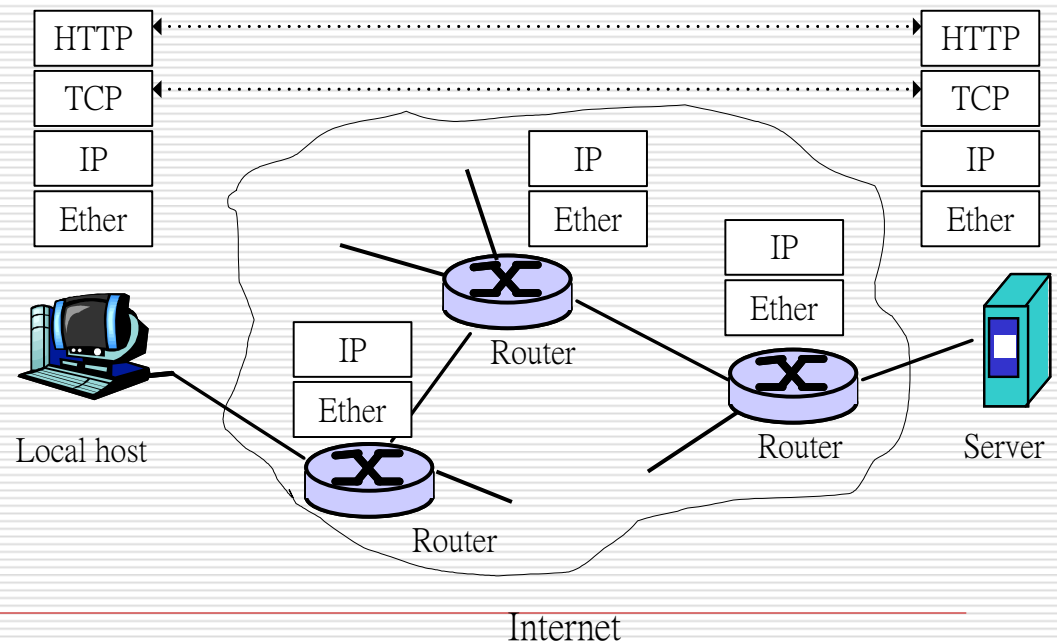
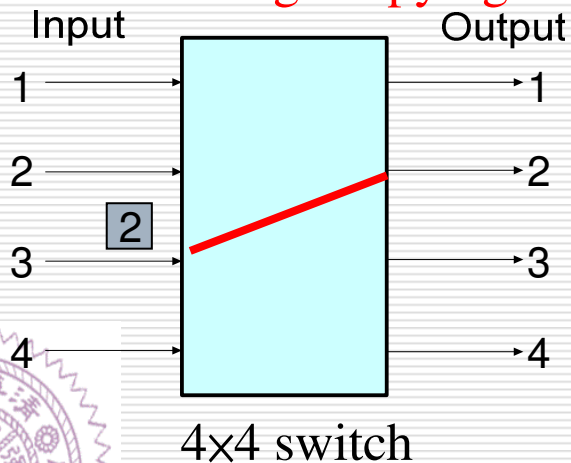
Yu-Hao Hsu, Yang-Syu Lin, Ching-Te Chiu, Jen-Ming Wu, Shuo-Hung Hsu, Fan-Ta Chen, Min-Sheng Kao, [Wei-Chih Lai](#), and YarSun Hsu

National Tsing Hua University, Taiwan



Network Router/Switch

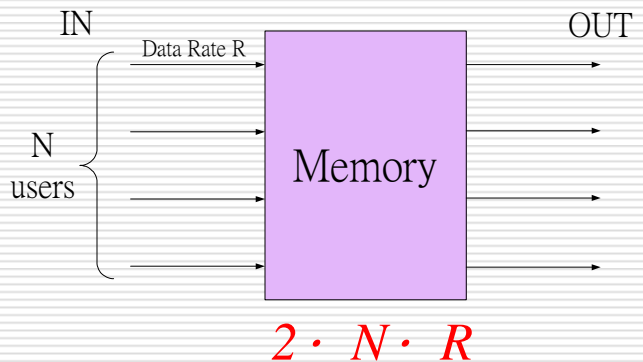
- A router/switch is a network element with multiple input ports and output ports.
- $N \times N$ switch: N input ports and N output ports
- Basic functions:
 - ✓ table lookup
 - ✓ message copying



Output Switch and Input Switch

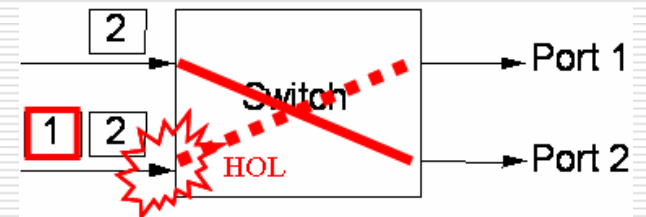
- Output-buffered switch:

- ✓ Feature: common shared memory, speedup of N requirement
- ✓ Problem: memory access limitation
- ✓ Solution: parallel-buffered switch



- Input-buffered switch:

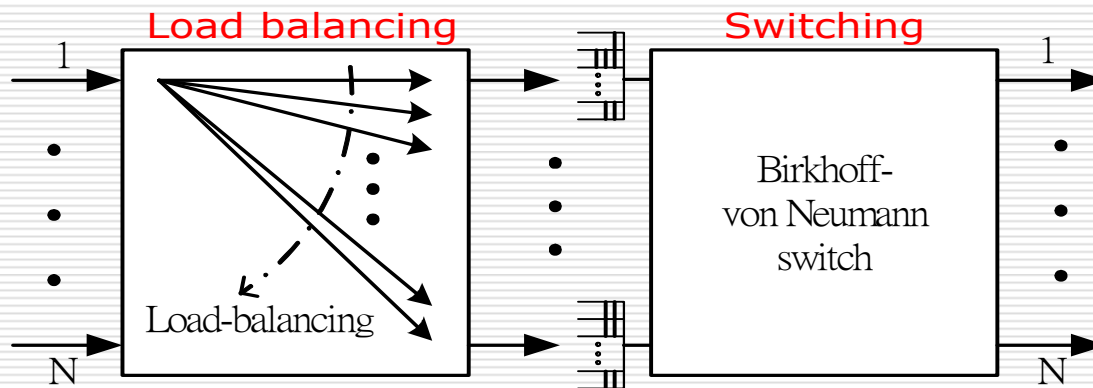
- ✓ Feature: one buffer per input port
- ✓ Problem: head-of-line blocking, 58% throughput



✓ Solution: VOQ (virtual output queuing) technique



Load balanced Birkhoff-von Neumann Switch Architecture

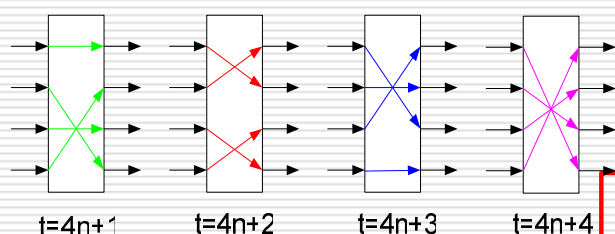


- Features:
 - ✓ 100% throughput
 - ✓ scalability: $O(1)$, periodic, deterministic
 - ✓ lower average delay in heavy or burst traffic
 - ✓ better buffer utilization
 - ✓ lower hardware complexity
- Problem: out-of-sequence issue

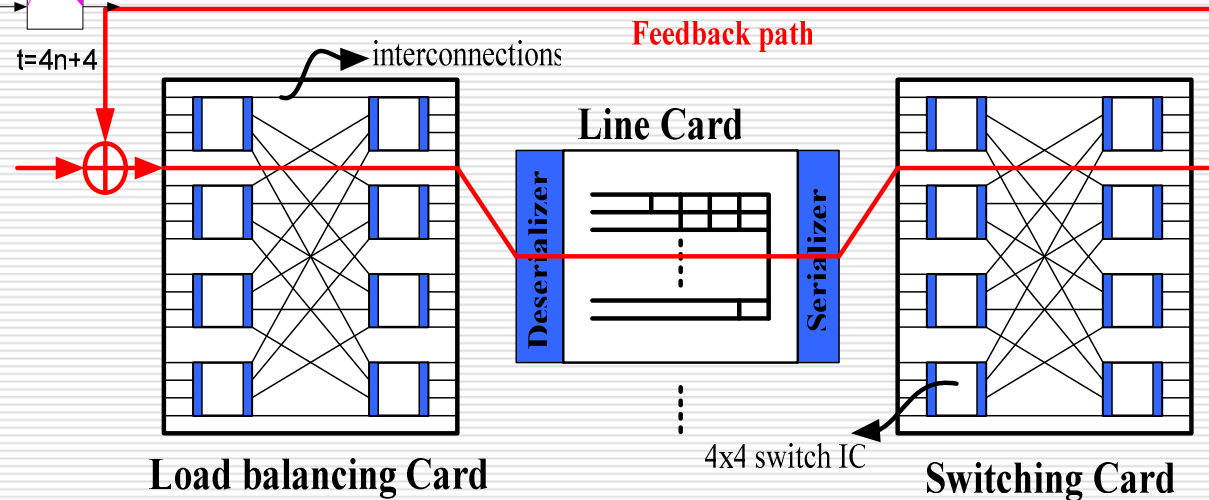


Feedback-based System

Symmetric TDM Patterns



50ns for each SerDes interface



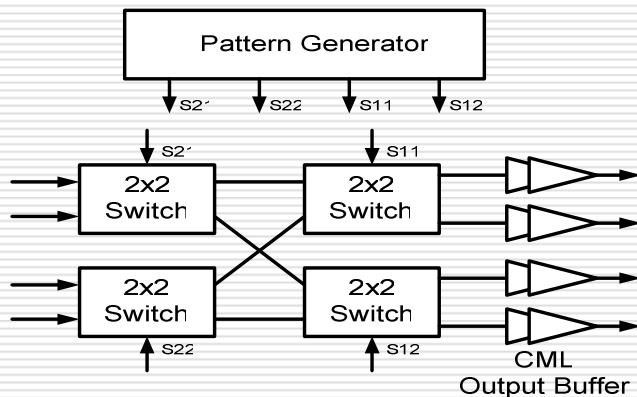
Motivation : switching packet directly in RF domain

- Low propagation delay in feedback system

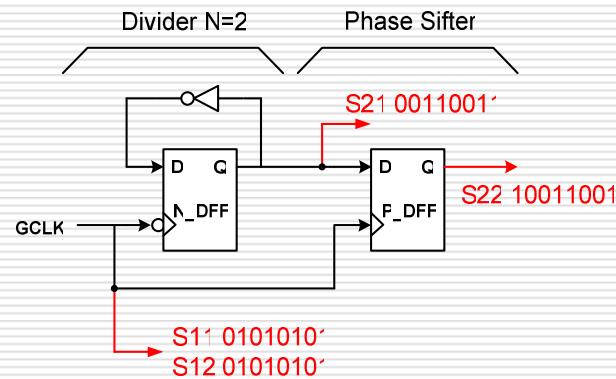


Proposed Low Propagation Delay 4x4 Switch Architecture and Measurement Results

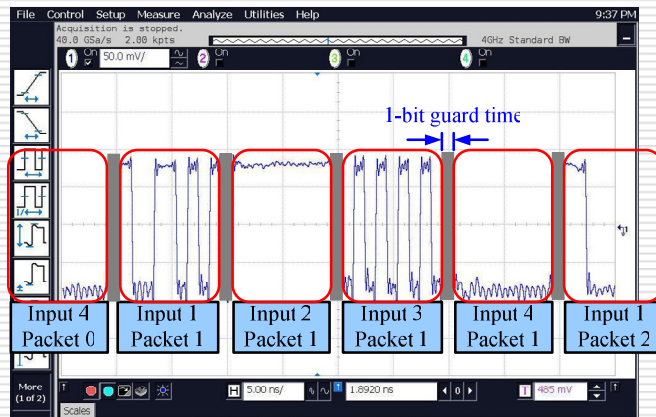
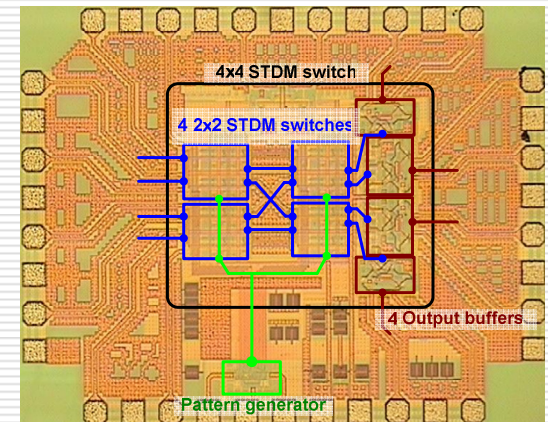
Overall Architecture



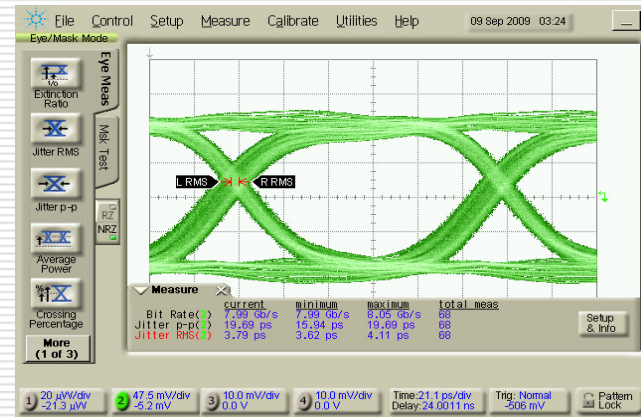
Pattern Generator



Die Photo



One of the Output Waveform



Measurement Eye Diagrams: 6
Jitter_{p-p} = 20ps @8Gbps.

