

A Fully Integrated Shock Wave Transmitter with an On-Chip Dipole Antenna for Pulse Beam-Formability in 0.18- μ m CMOS

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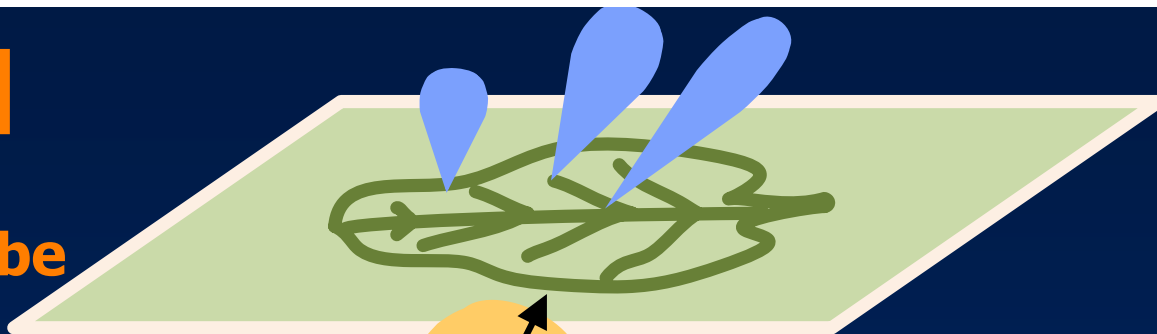
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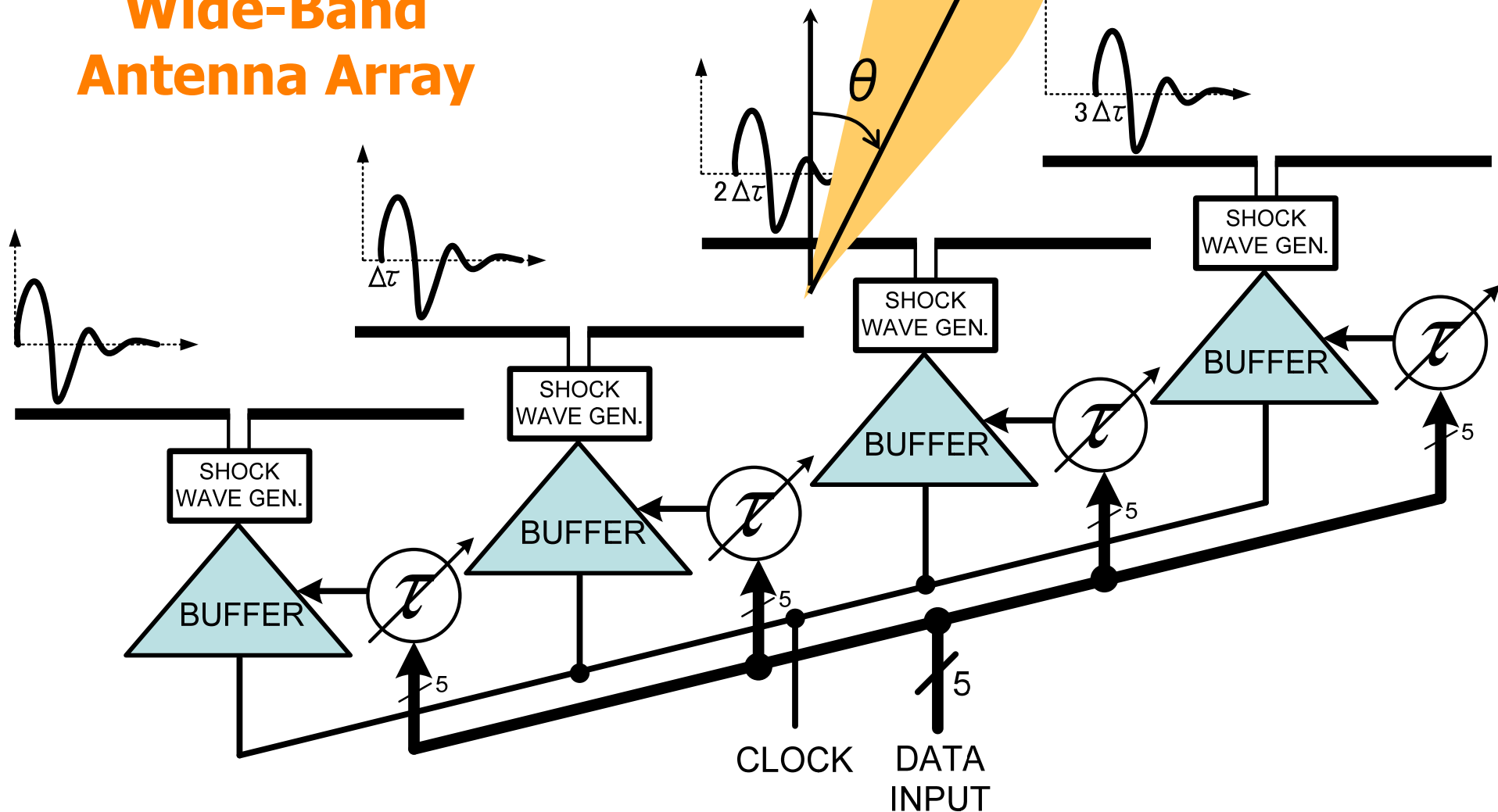
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MOTIVATION

Object to be imaged



Wide-Band
Antenna Array

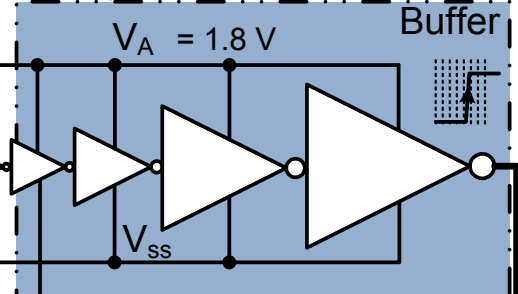
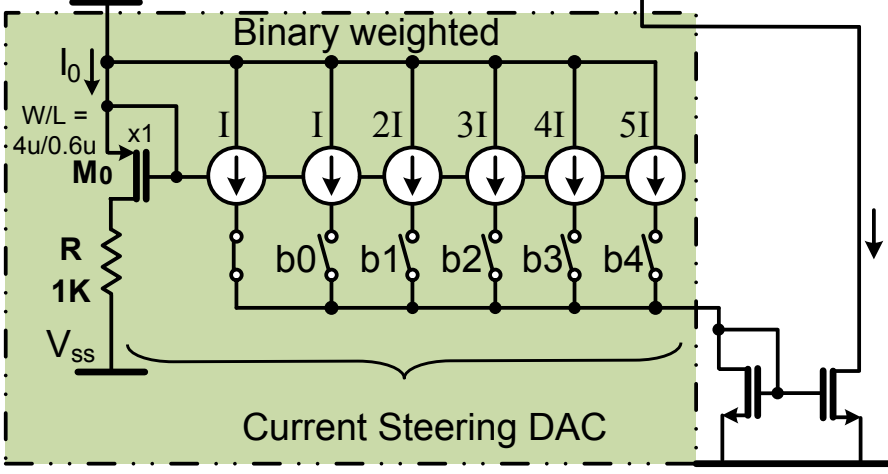


IMPLEMENTATION (0.18 μm CMOS)

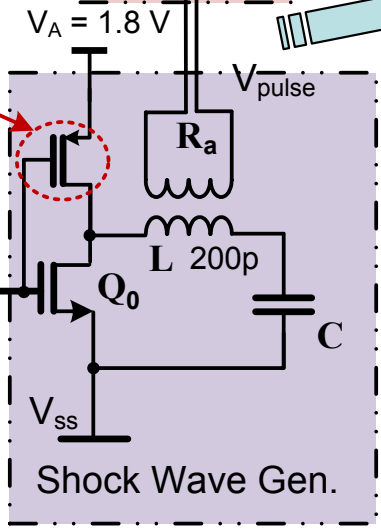
Analog part

Digital part

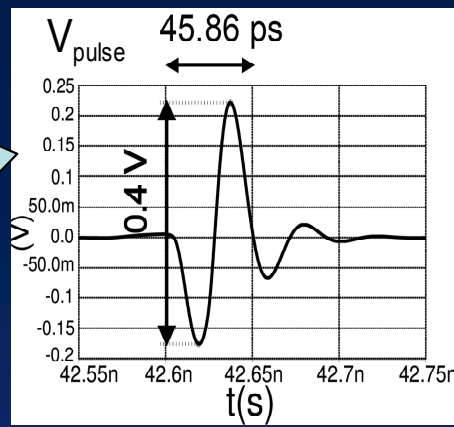
$V_{DD} = 1.8\text{ V}$



Radiation part



SHOCK WAVE OUTPUT (sim.)

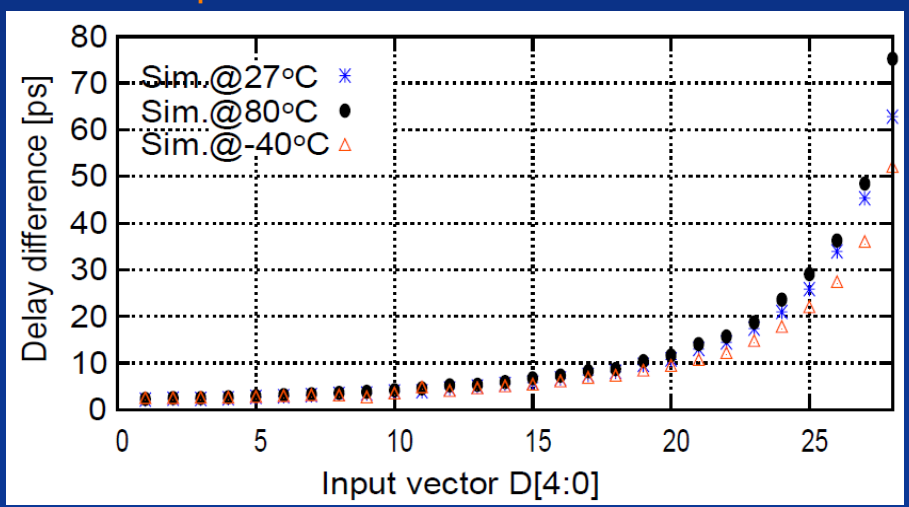
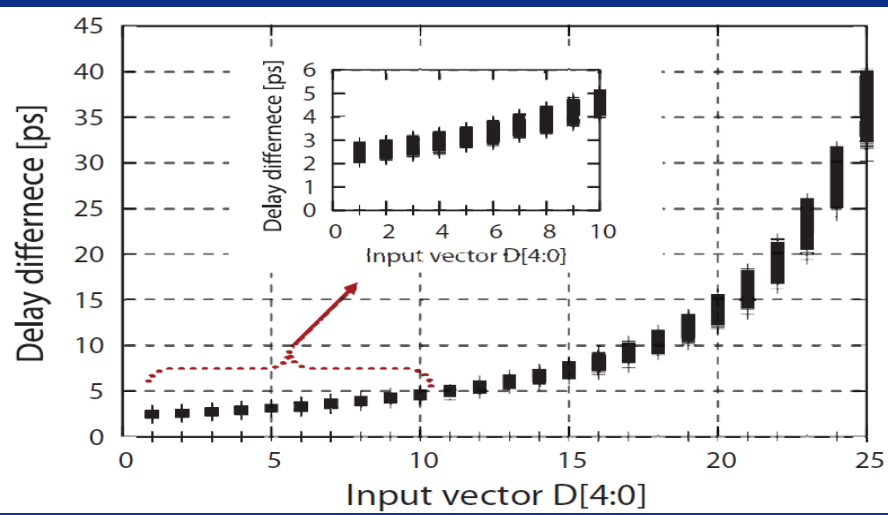


- Target freq. 10 – 12 GHz
- Suitable to achieve $\theta_{min} = 14.4^\circ$ for the array antenna.

PULSE DELAY SIM.

Monte Carlo : $V_{threshold}$ (3σ ; 5%), 5000 points

Temperature: -40°C to 80°C



Measurement for an on-chip Antenna

HP 8510 Network Analyzer

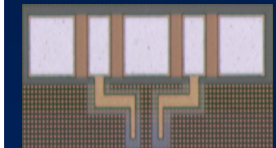
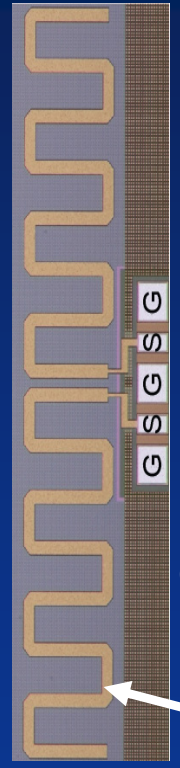


cable

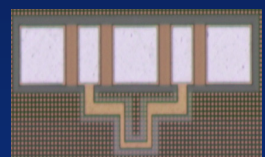


100 μm pitch GSGSG probe

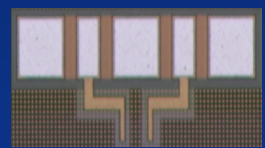
On-chip AUT



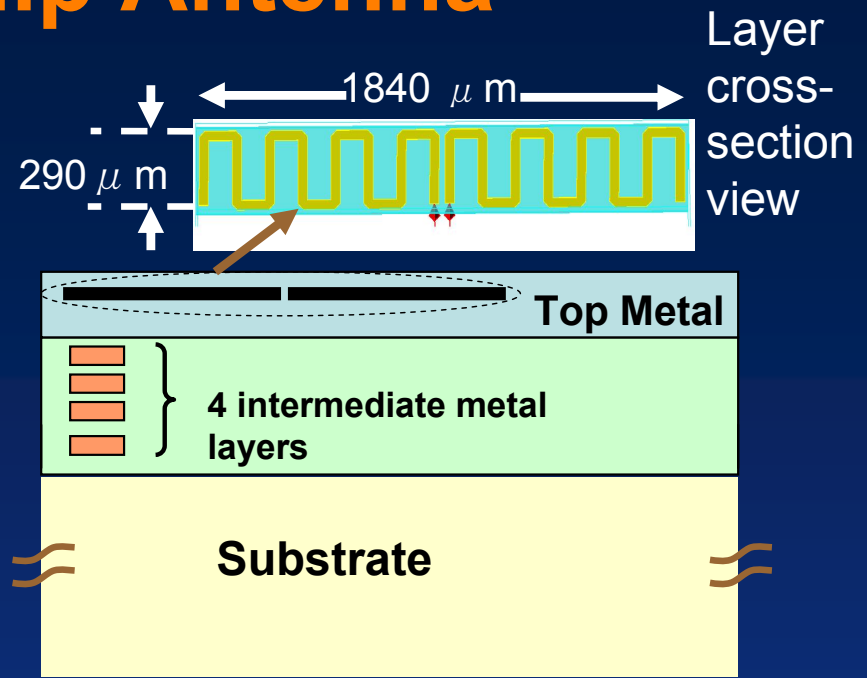
"open"



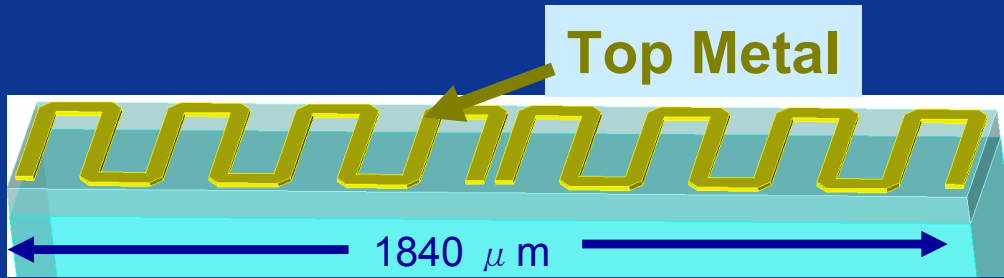
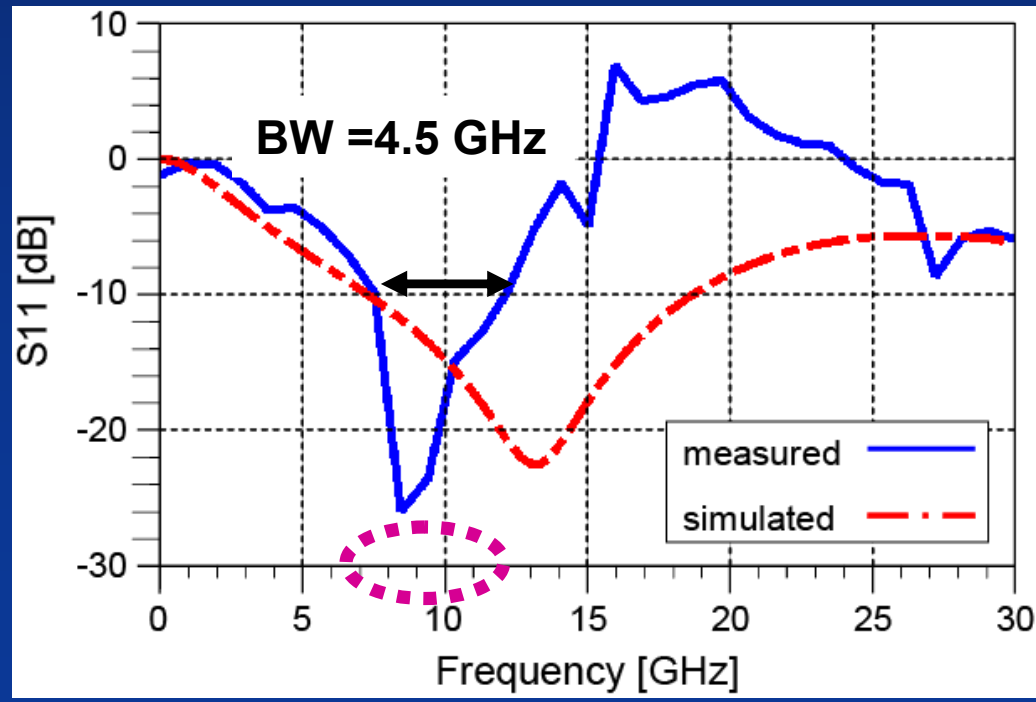
"through"



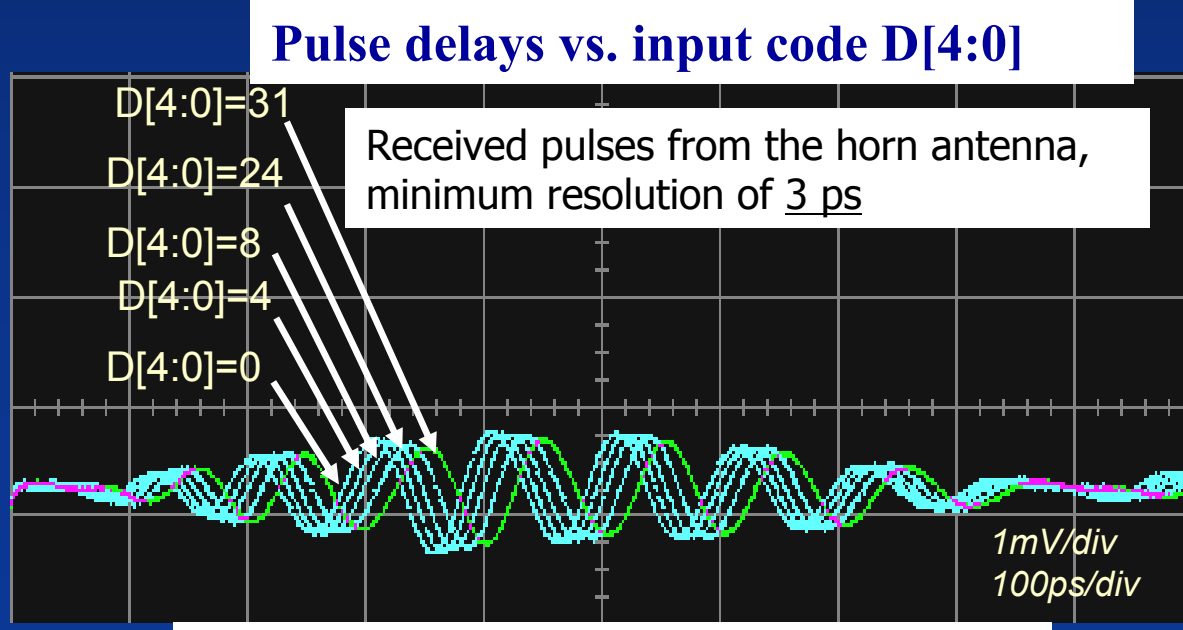
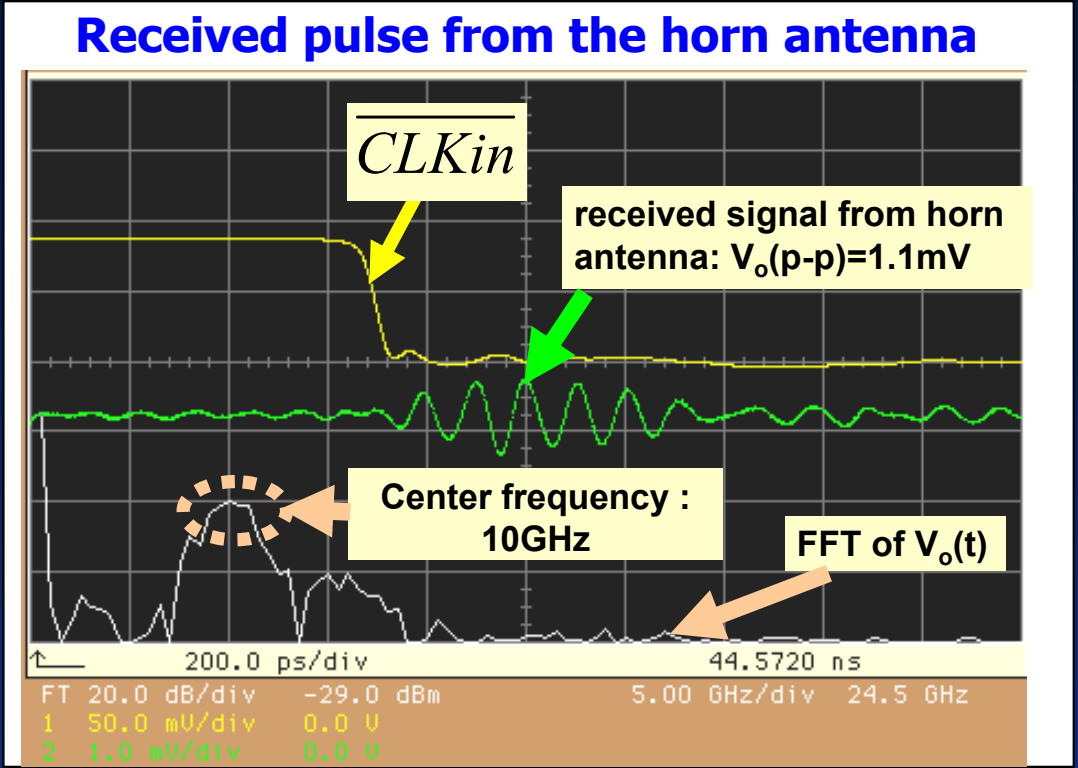
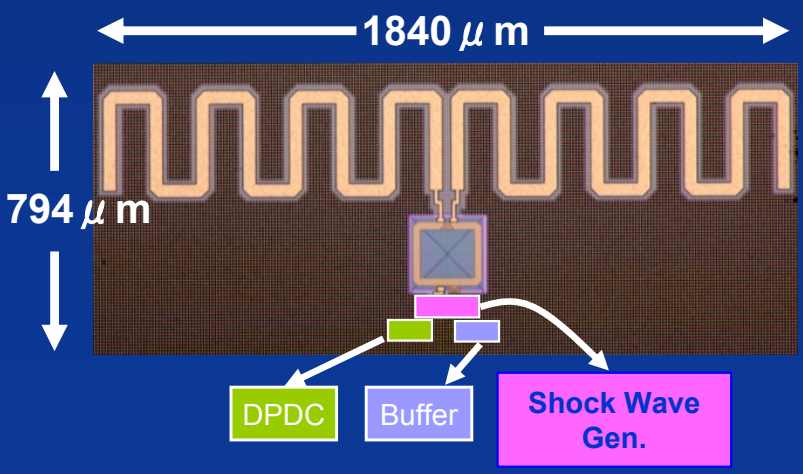
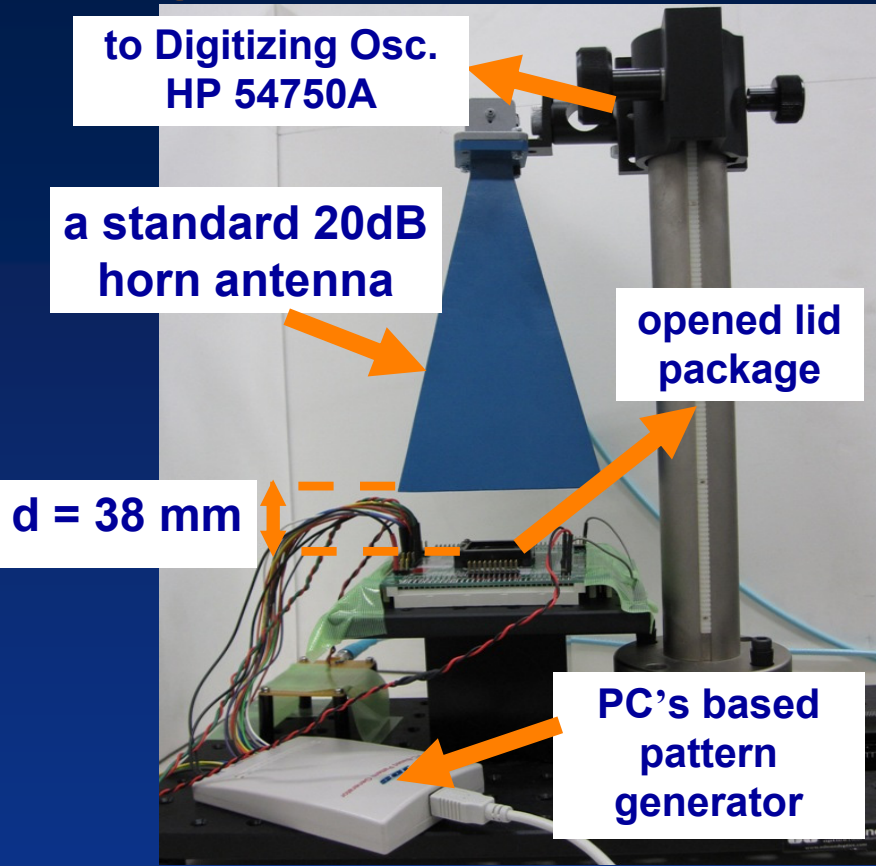
"short"



Return loss, S11



Meas. of the Fully Integrated Transmitter



Suitable for pulse beam-forming

Ref.	Process	BW (GHz)	Vout (V)	Freq (GHz)	P (mW)	Beam-formability	dre & drag (*) (ps)	On-chip ant.	Circuit description
[1]-2007	1.5-V 0.13- μ m CMOS	1 – 15	-	-	555	YES	dre = 15 drag = 225	NO	UWB timed-array <i>receiver</i> with 188 on-chip inductors
[2]-2009	1.2-V 0.13- μ m CMOS	4.3	1	N/A	2.7	NO	-	NO	UWB pulser co-designed with wire-bond transition with pulse width = 0.6 ns
[3]-2009	3-V 0.5- μ m CMOS	0.5	0.289 – 0.337	0.485	1.3	NO	-	NO	Turnable sub-GHz UWB generator
[4]-2007	1.2-V 90-nm CMOS	N/A	1 (sim.)	N/A	22	YES	drag = 1000 – 3000	NO	UWB 3.1 – 10.6-GHz triangle pulse generator pulse width = 250 ps
[5]-2006	2.5-V 0.25- μ m CMOS	-	-	-	100	YES	dre = 100 drag = 100 – 500	NO	not integrating pulse transmitter, beam-steering subsystem only
This work	1.8-V 0.18- μ m CMOS	2	0.4 (sim.) 0.0011 (received)	10	32.4	YES	dre = 3 drag = 34	YES	Pulse generator with an integrated antenna for beam-formability purpose

[1] T. S. Chu, 2007

[3] Y. Joo, 2009

[2] S. Bourdel, 2009

[4] F. Zito, 2006

[5] M. Yan-Wah Chia

(*) **dre** is delay resolution; and **drag** is delay range