An On-Chip Characterizing System for Within-Die Delay Variation Measurement of Individual Standard Cells in 65-nm CMOS

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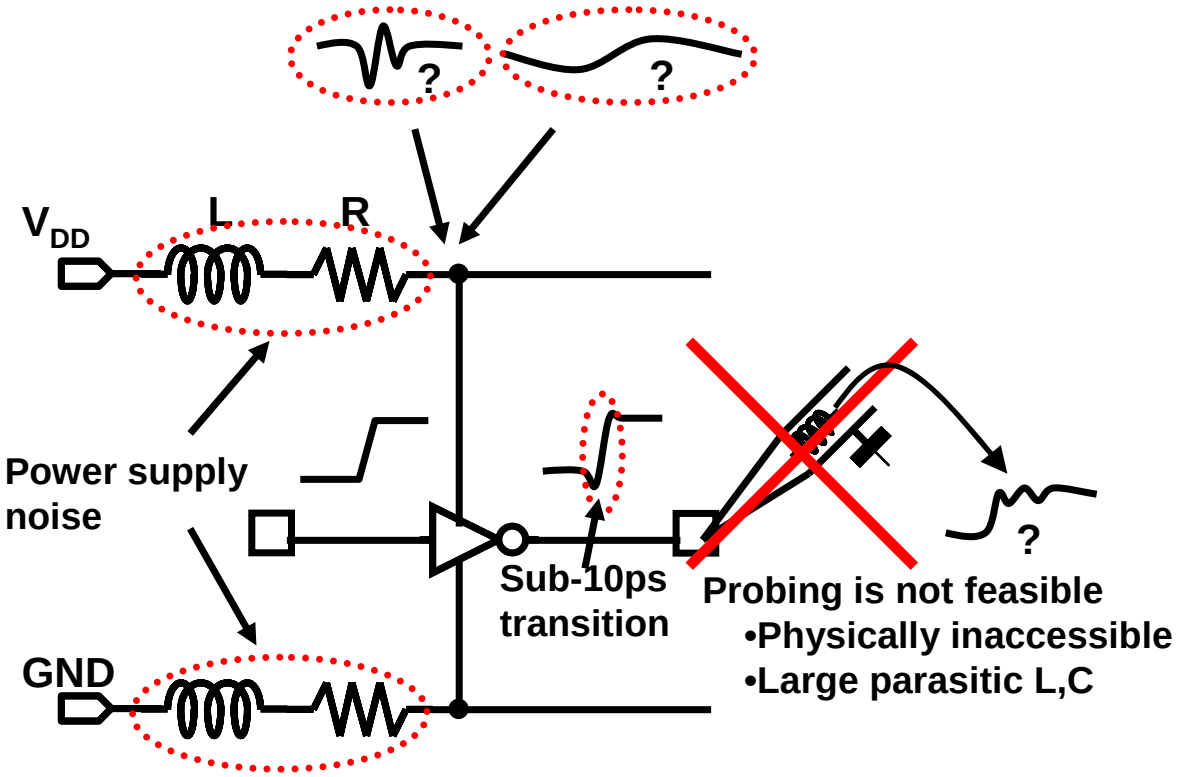
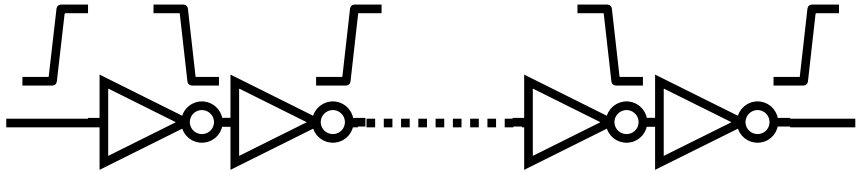
Problem of conventional methods



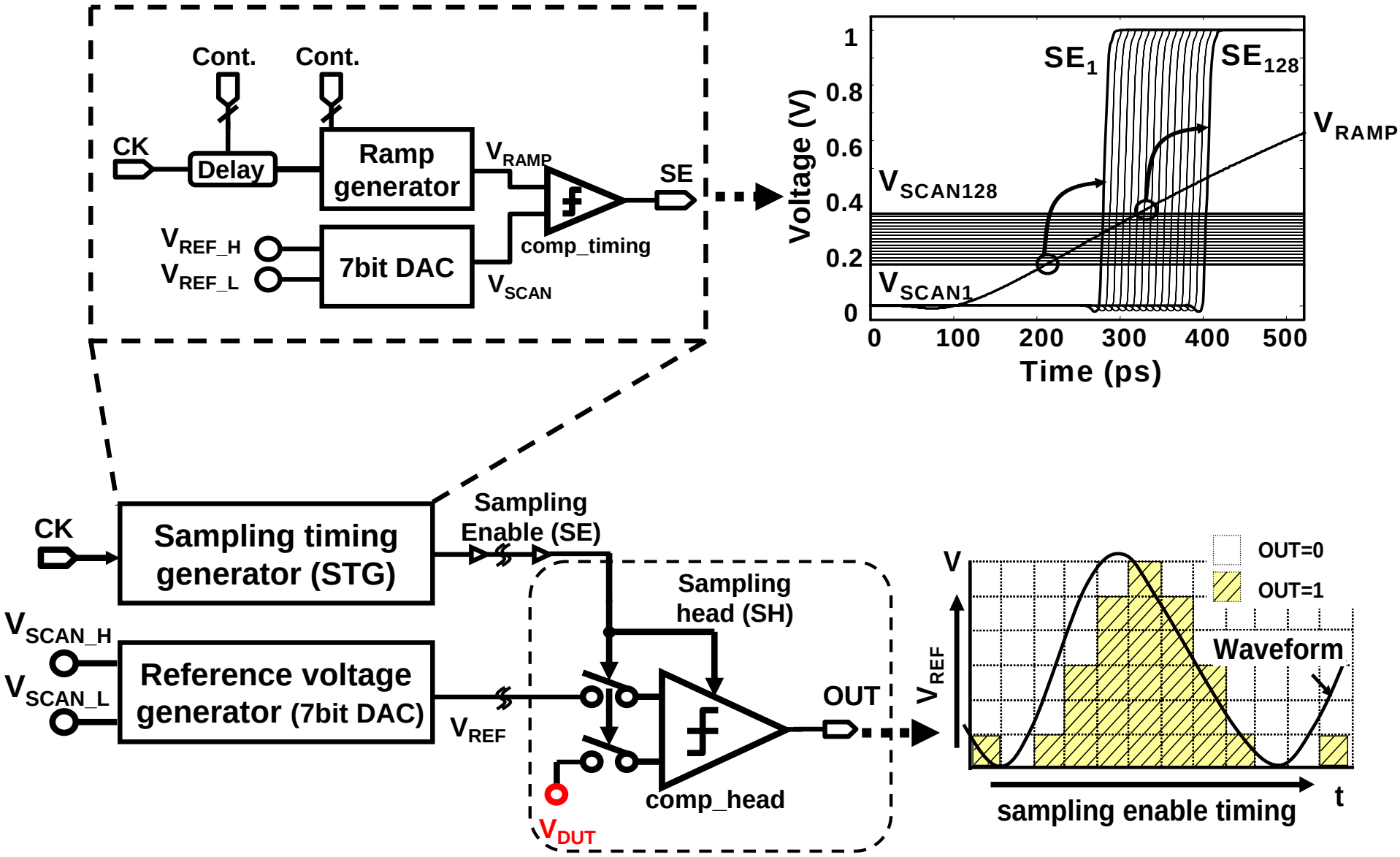
Directly probing



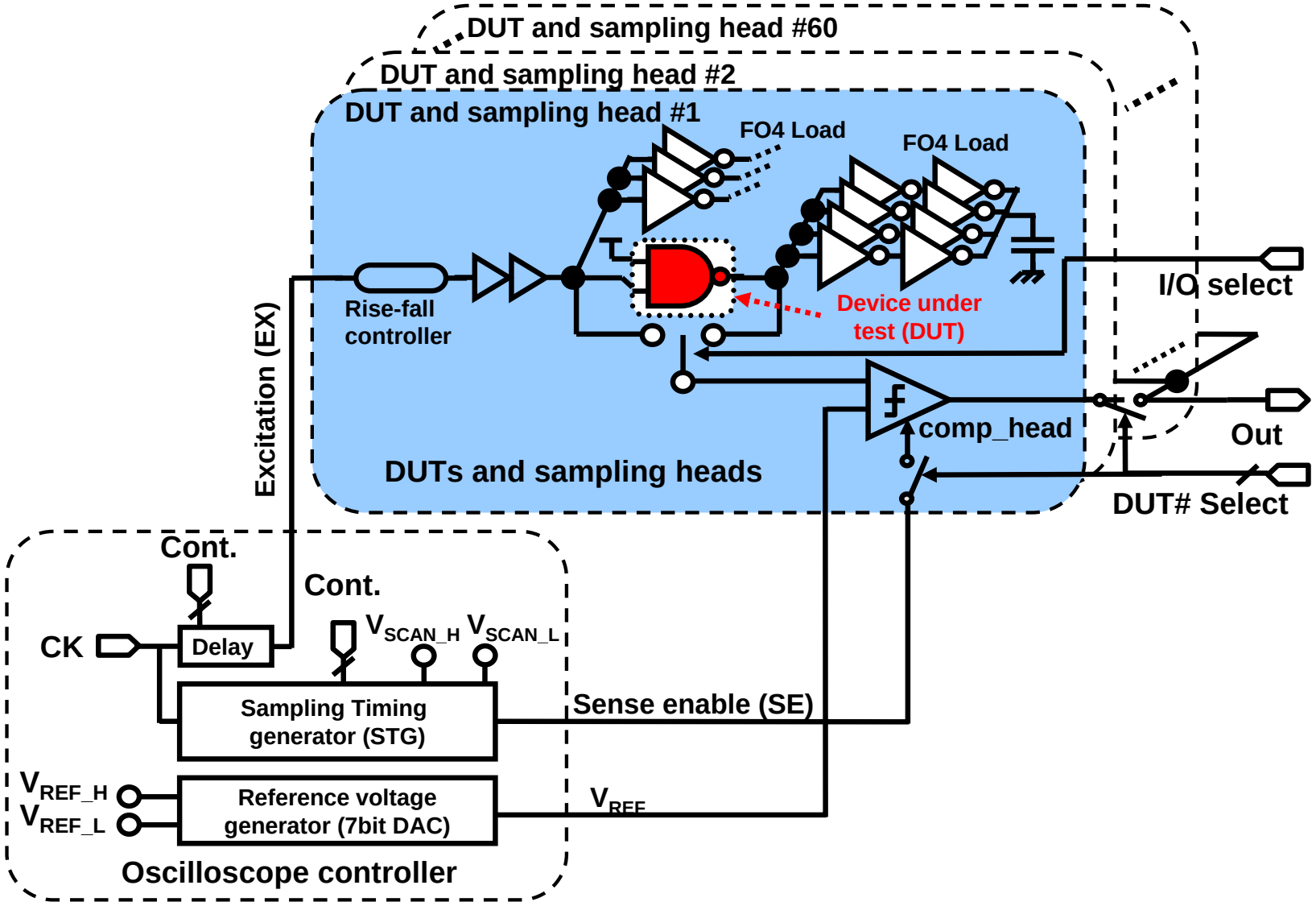
- single-gate contribution is impossible
- Rising and falling delays are mixed

Inverter chain or ring oscillator

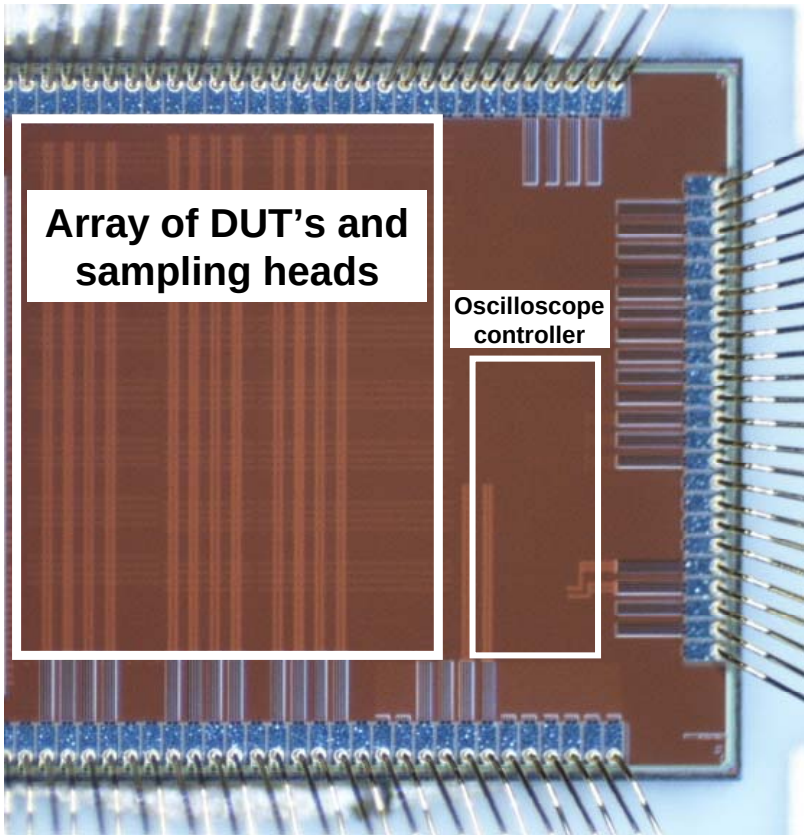
On-chip sampling oscilloscope

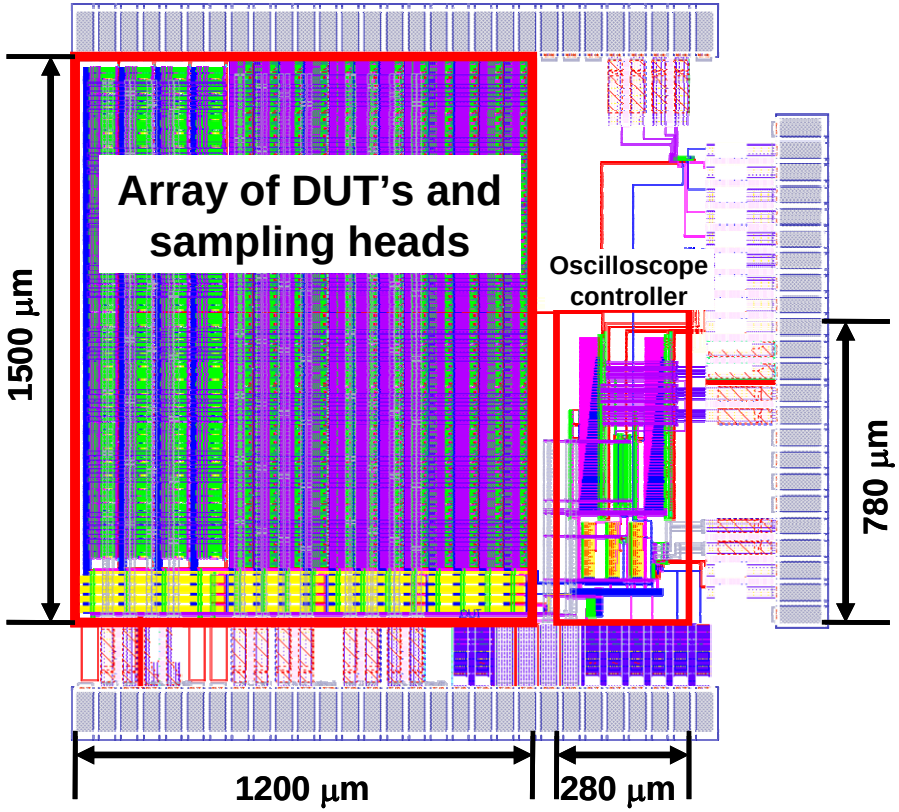


Within-die delay variation measurement using on-chip sampling oscilloscope



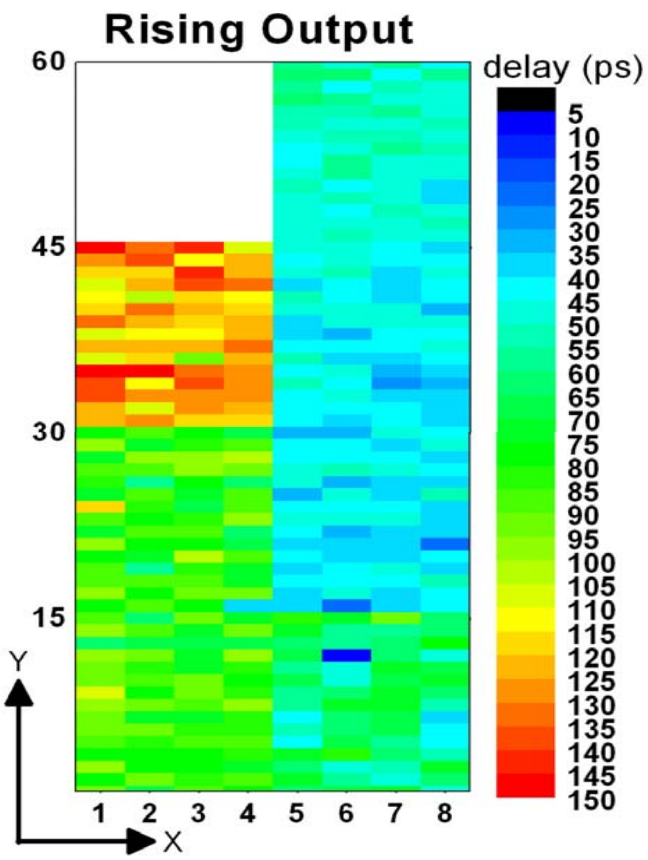
Chip photo and layout

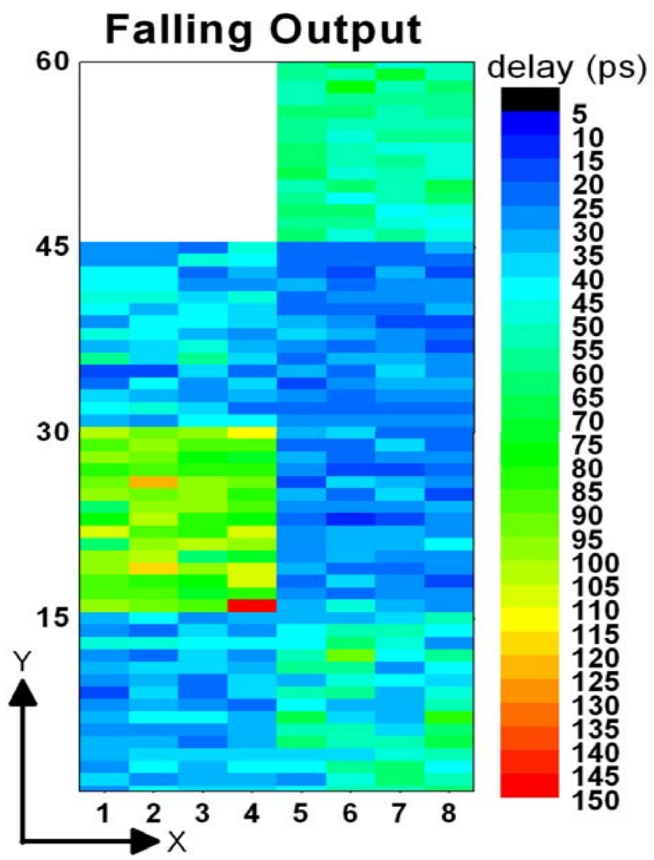


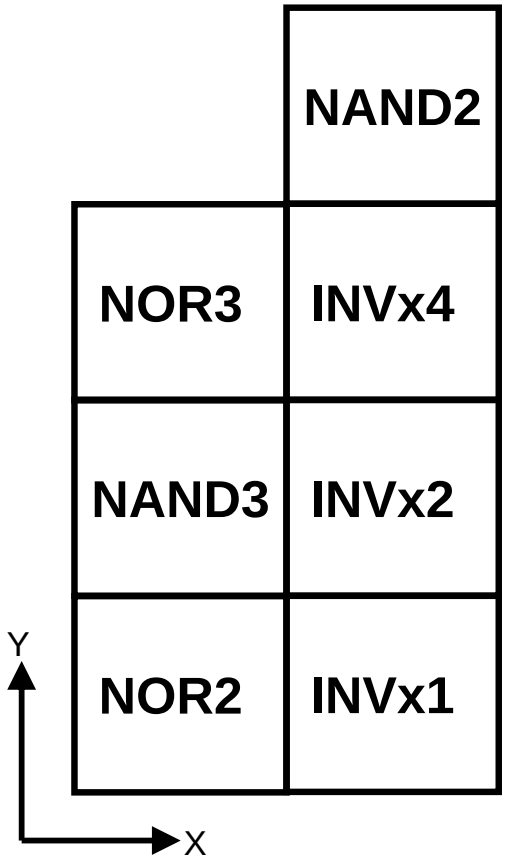


- The test chip is fabricated in 65nm CMOS process.
- Chip size is 2mm x 2mm.
- 7 types of standard cells: INVx1, INVx2, INVx4, NAND2, NOR2, NAND3, and NOR3 are implemented with 60 DUT's for each.

Measurement results of propagation delay







- **The positions cells are corresponding to the actual test chip.**
- **The measured variation is random, no systematic component due to IR-drop on power lines is observed.**
- **More detailed results and analyses will be shown in the poster.**