A Gate-level Pipelined 2.97GHz Self Synchronous FPGA in 65nm CMOS

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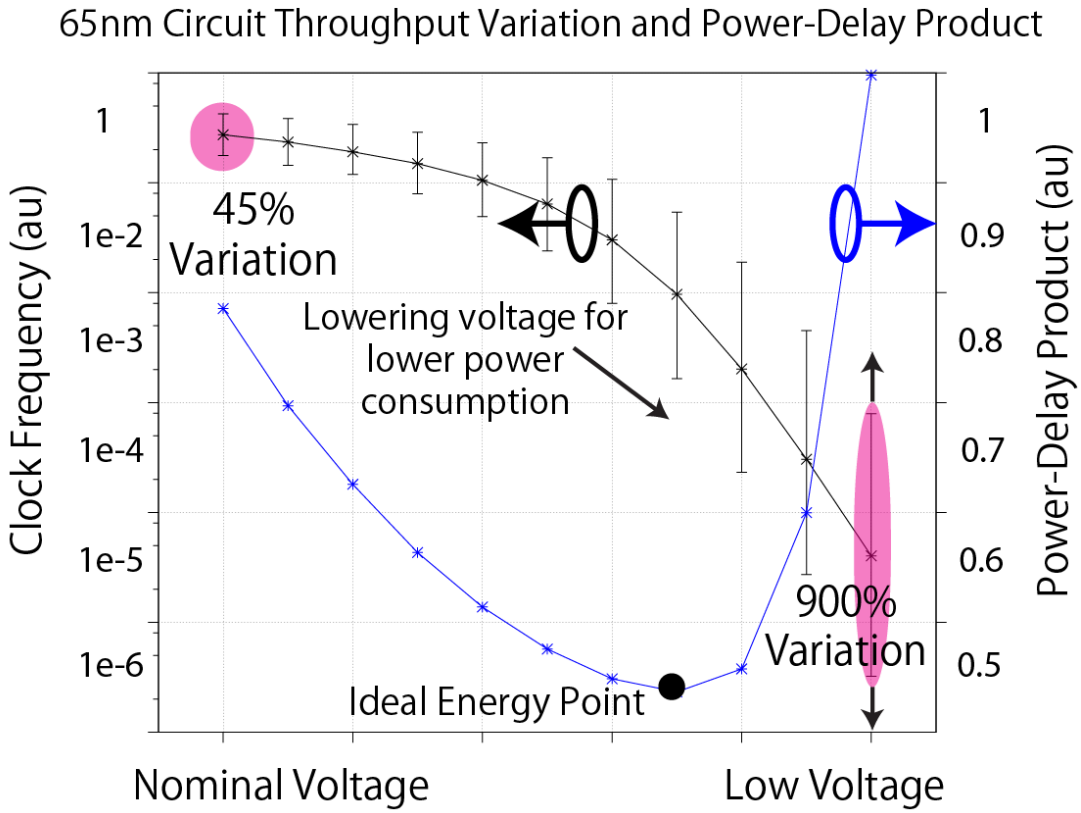
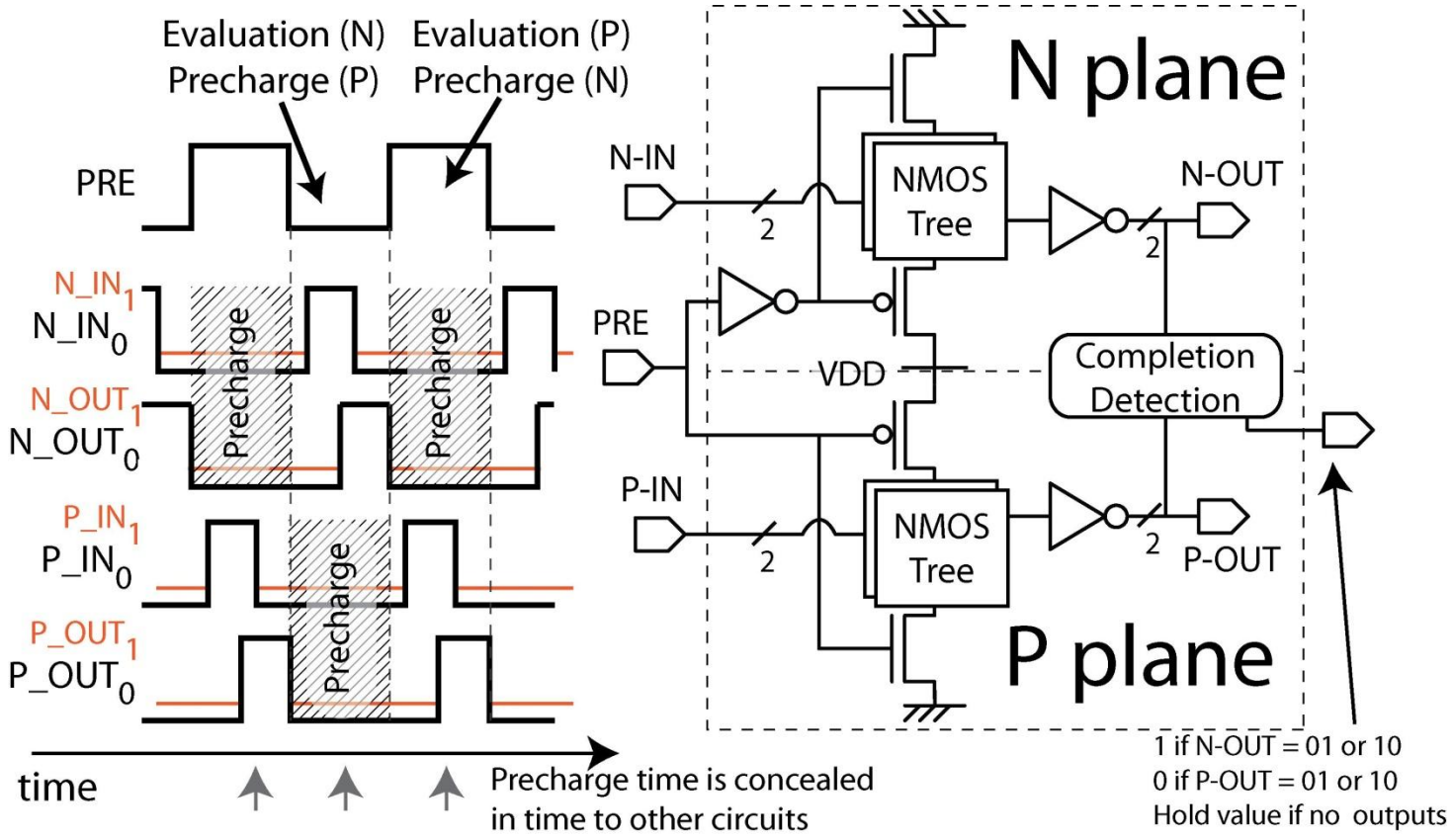
Motivation

- Variation is increasing
- Want to operate at ‘Ideal Energy Point’
  - Need PVT (process, voltage, temperature) variation robust systems



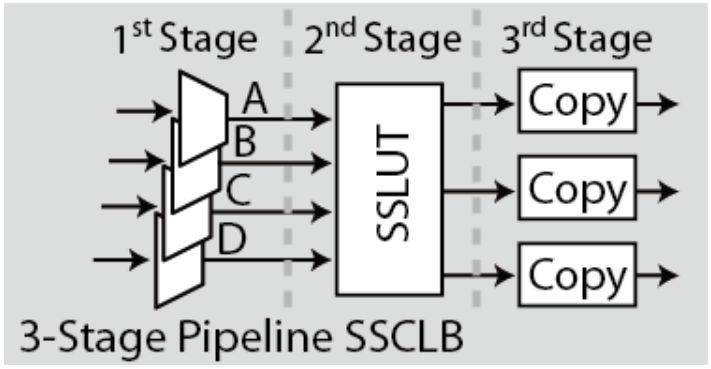
Dual Pipeline DCVSL

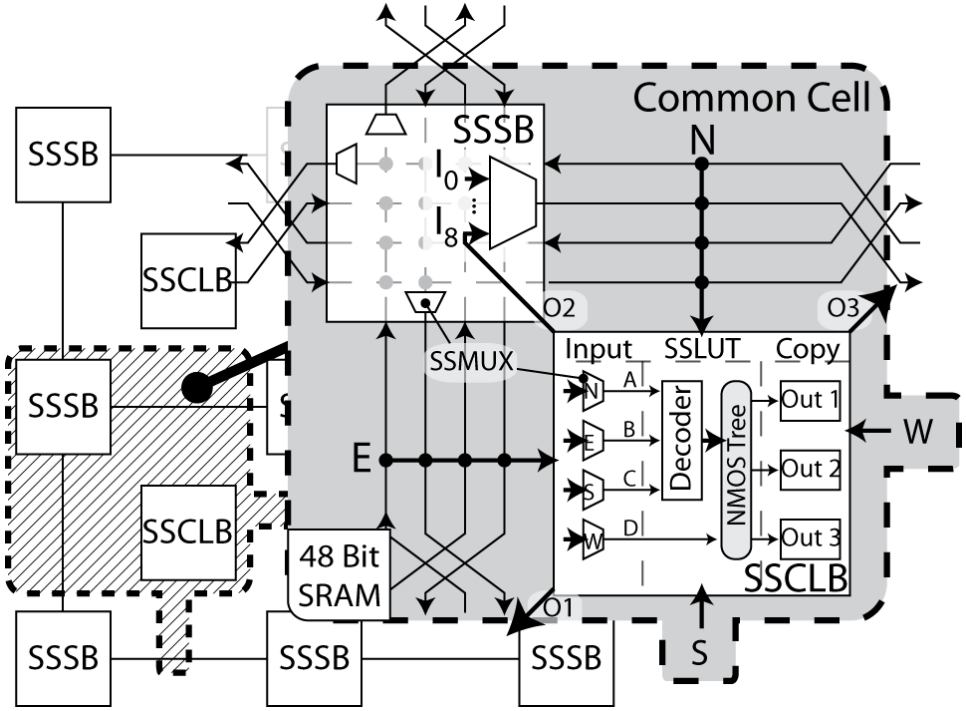
- Dual Pipeline conceals DCVSL precharge delay
- Self Synchronous operation with Completion detection for delay insensitivity

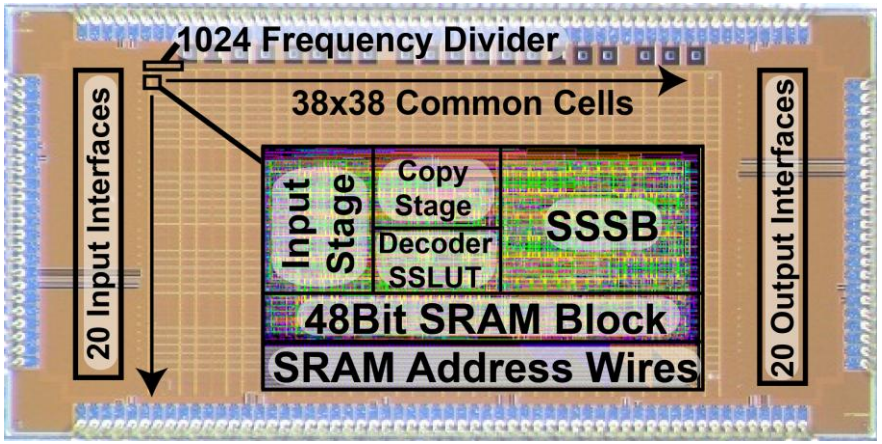


SSFPGA Chip

- A Self Synchronous FPGA was fabricated in 65nm and measured
- Dual Pipeline DCVSL, Completion Detection circuits
- Gate level Pipeline
- 4-input lookup table, 3-output, 4 channels

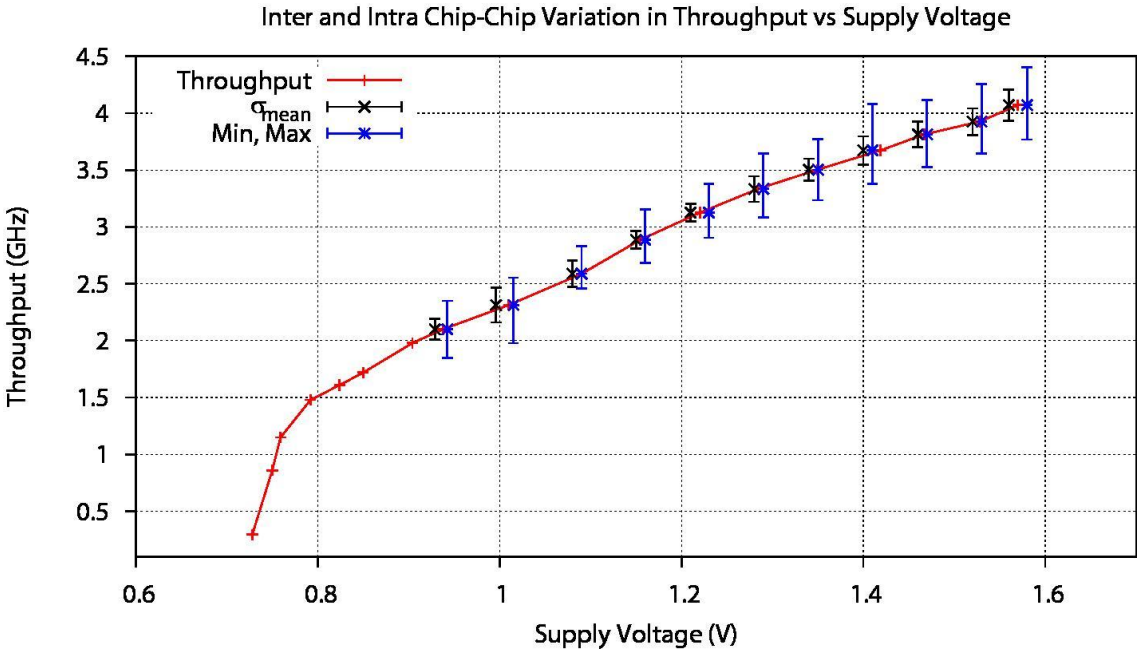


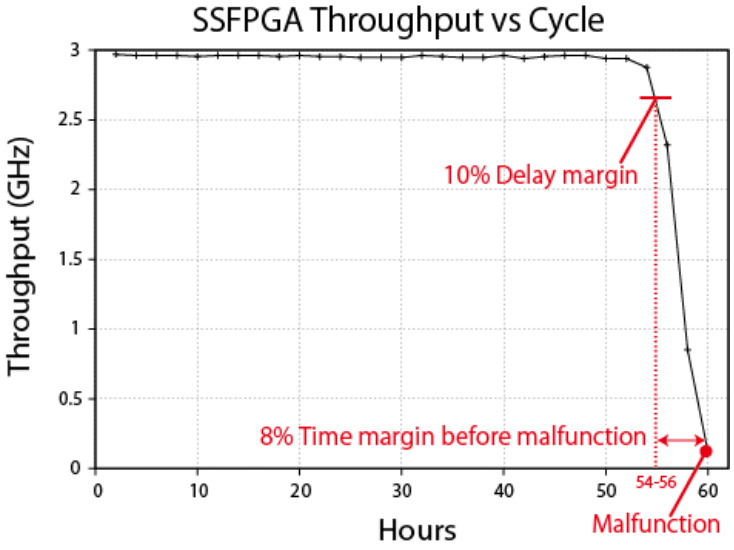




Measurement Results

- Throughput of 3GHz @ 1.2V (highest reported)
- Correct operation to 750mV, 0-120ºC
- Self Synchronous Signaling improves aging characteristics, 8% longer compared to Synchronous System





Conclusions

- The fabricated SSFPGA was measured against PVT variations, and showed robust, correct operation over 750mV to 1.6V, 0ºC to 80ºC, with process variation
- Aging measurements show correct operation 8% longer past a 10% delay margin, until chip malfunction
- **This research shows Self Synchronous Circuits can offer Reliable, Ideal Energy Point Operation in nano-meter node processes for future VLSI systems**

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The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd.