1D-22

A 95-nA, 523ppm/°C, 0.6-μW CMOS Current Reference Circuit with Subthreshold MOS Resistor Ladder

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Ultra Low Power LSIs

Ubiquitous network

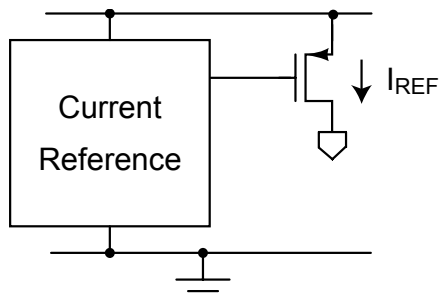
Key devices

- Smart sensor LSIs

Demand for ultra low power LSIs

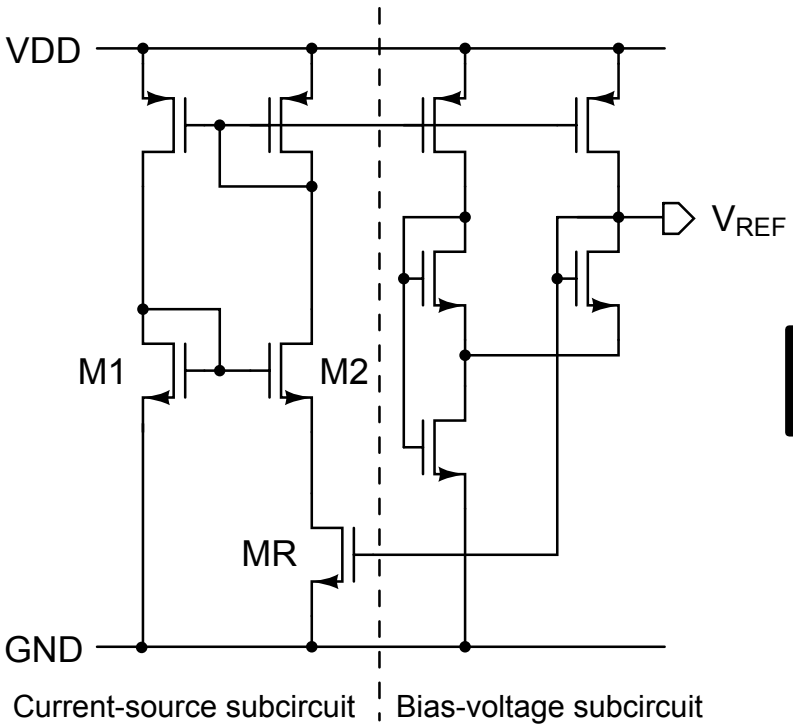
Current reference circuit

- Provide a nano-ampere current
- Tolerant to PVT variations

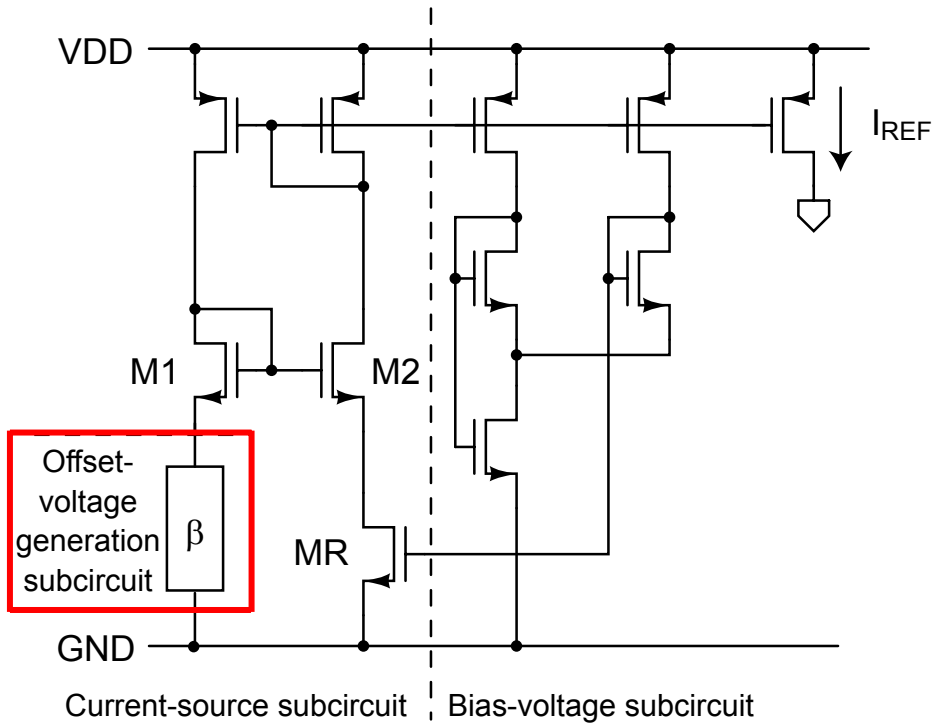


Proposed Current Reference Circuit

Conventional



Proposed



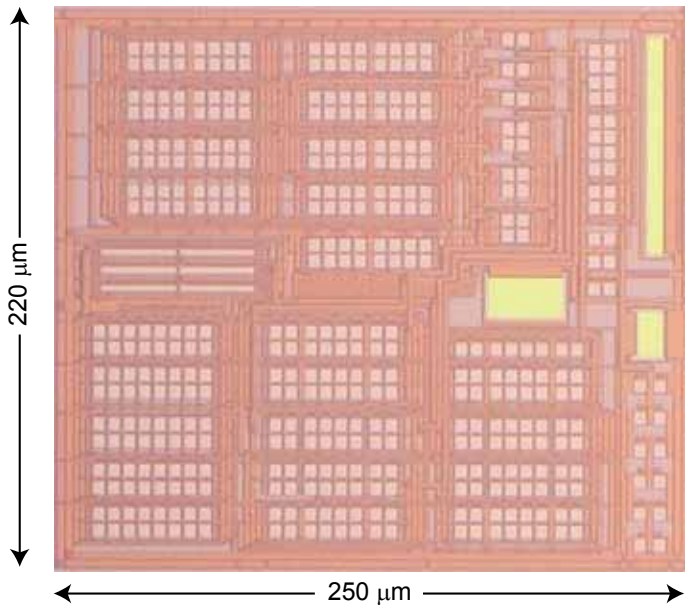
Add offset-voltage generation subcircuit

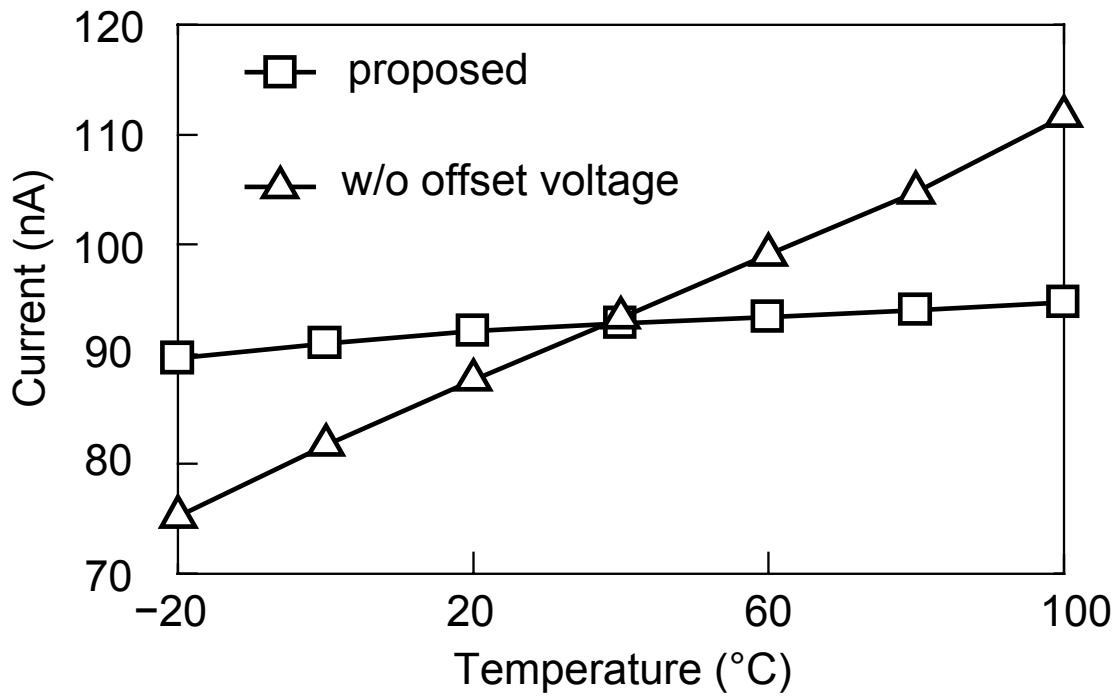
Control temperature characteristics of current

Current tolerant to PVT variations

Chip Photo & Experimental Results

CMOS 0.35 μm





Area : 0.055 mm²

TC : 459ppm/°C
(89% reduction)

Comparison

References	This work	[1]	[2]	[3]	[4]	[5]
Technology (μm)	0.35	0.35	0.35	N/A	0.8	3
I_{REF} (nA)	94.9	96	10	287	430	774
Power (nW)	598	1000	170	N/A	2150	7000
Temp. (°C)	-20 – 100	0 – 80	-20 – 80	0 – 75	N/A	0 – 80
TC (ppm/°C)	523	520	1190	226	6000	375
Min. Supply (V)	1.8	1.8	1.3	N/A	2.5	3.5
Line reg. (ppm/V)	1780	2000	460	4000	5000	150
Chip area (mm^2)	0.055	0.015	0.12	N/A	0.04	0.2

[1] K. Ueno et al., IEEE CAS II, vol. 57, pp. 681-685, 2010.

[2] T. Hirose et al., in *Proc. ESSCIRC*, pp. 114-117, 2010.

[3] C. H. Lee and H. J. Park, Electronics Letters, vol. 32, pp. 1280-1281, 1996.

[4] J. Georgious and C. Toumazou, in *Proc. ISCAS*, vol. 3, pp. 193-196, 2002.

[5] W. M. Sansen et al., IEEE J. Solid-State Circuits, pp. 821-824, 1988.