An Adaptively Biased Low-Dropout Regulator with Transient Enhancement

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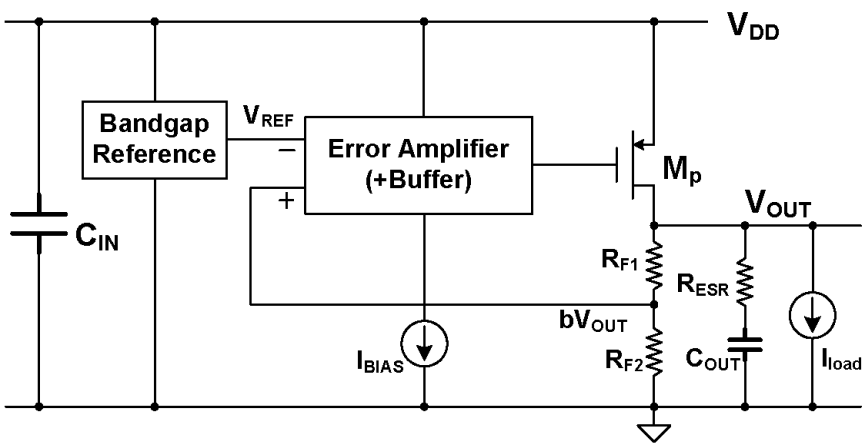
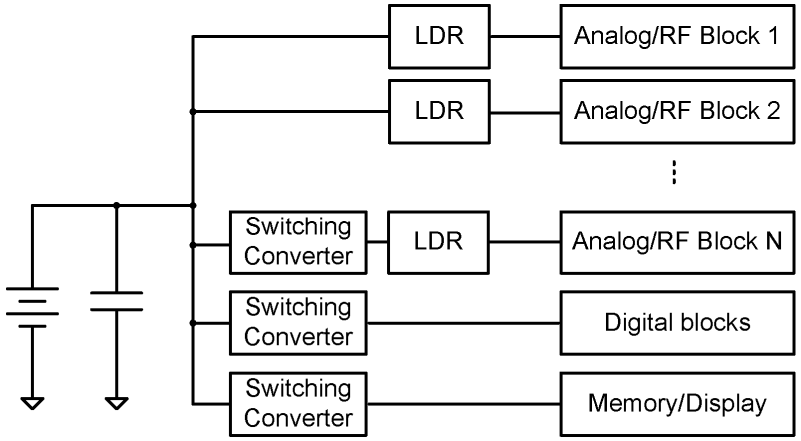
Motivation

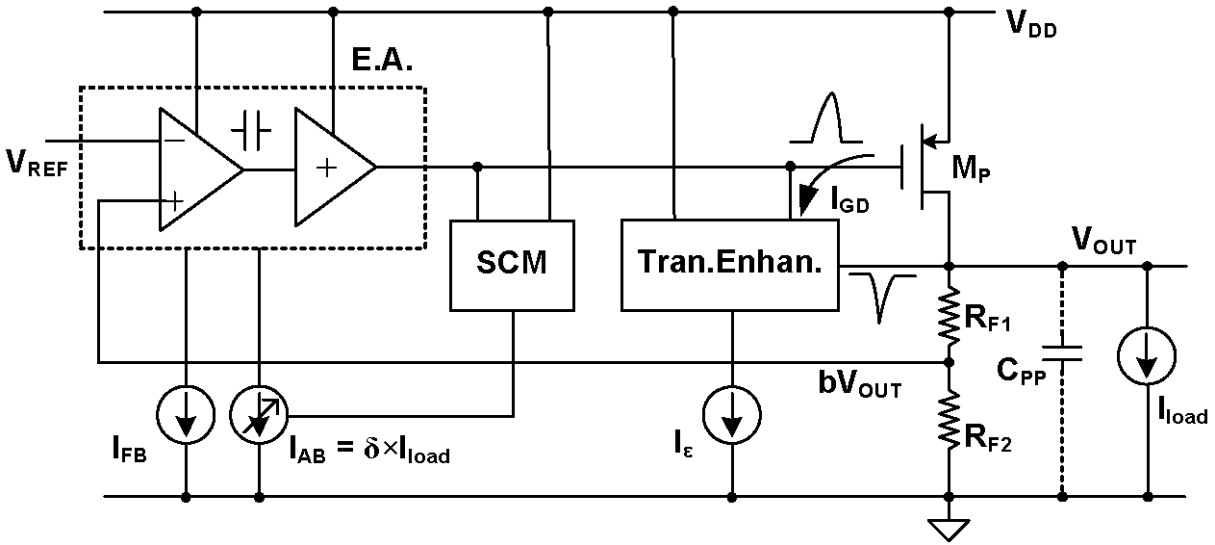




- Low-Dropout Regulators (LDRs) are key blocks in SoC
- They are desired / required to have features:
  - Output-capacitor-free; chip-area efficient
  - Low quiescent current; high current efficiency
  - Low-voltage high-precision regulation
  - Fast transient response; high PSR

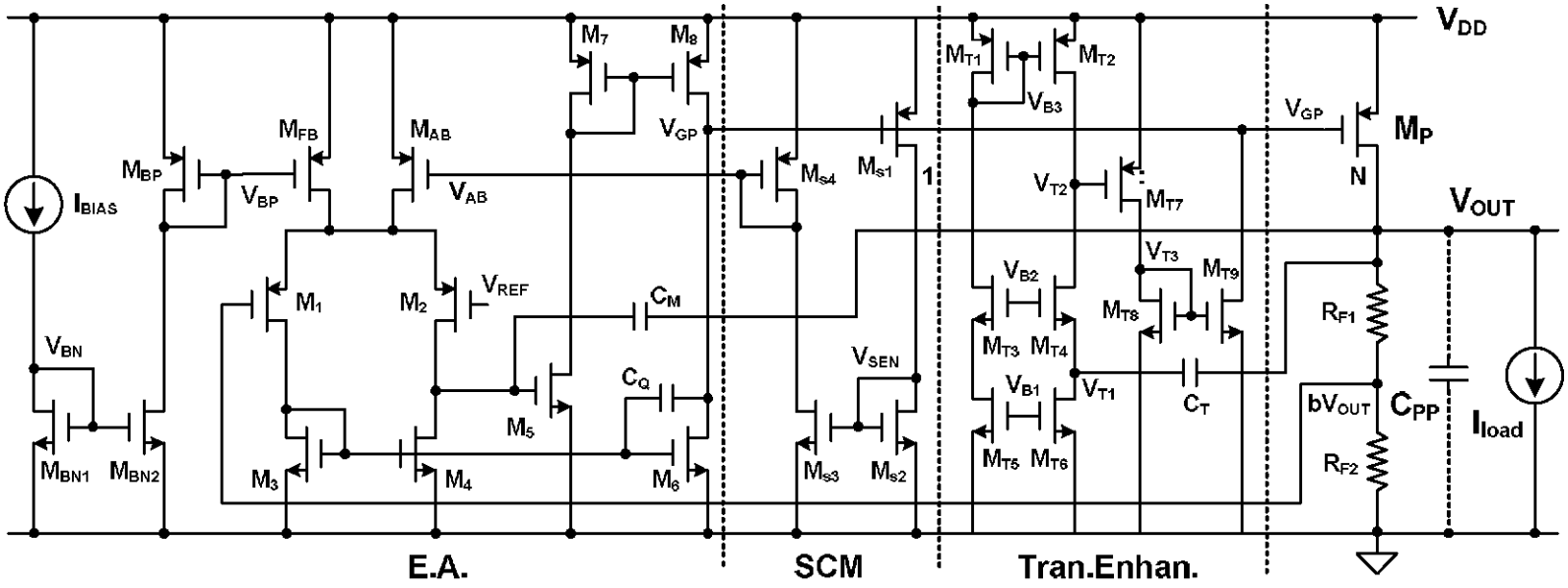
Can we achieve these features simultaneously?

Proposed Design: ABTE LDR



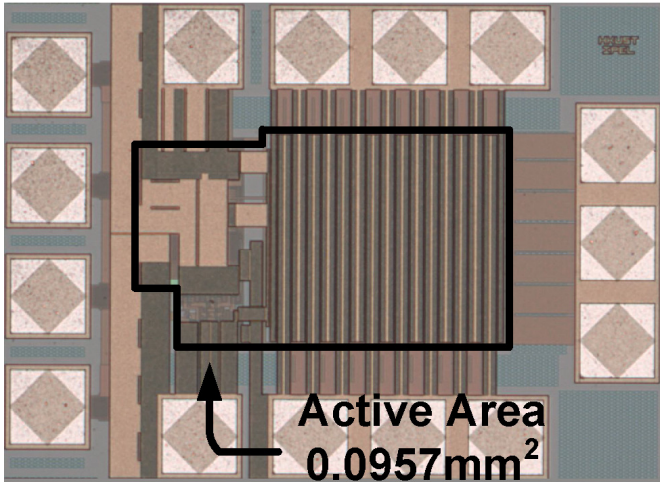
- C_{PP} stands for on-chip de-coupling / parasitic capacitance
- Multi-stage EA provides high-precision regulation
- Simple current mirror (SCM) implements adaptive biasing
- Transient enhancement block provides fast discharging of M_P gate when I_{load} steps up from small to large

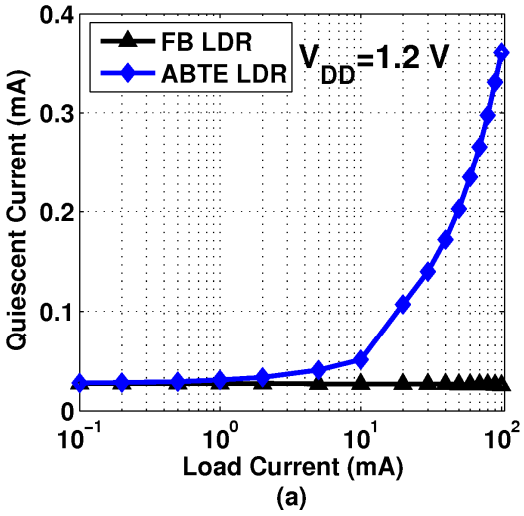
ABTE LDR: Schematic

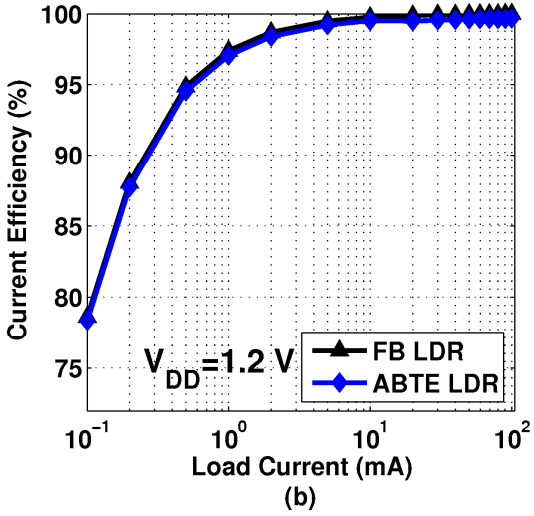


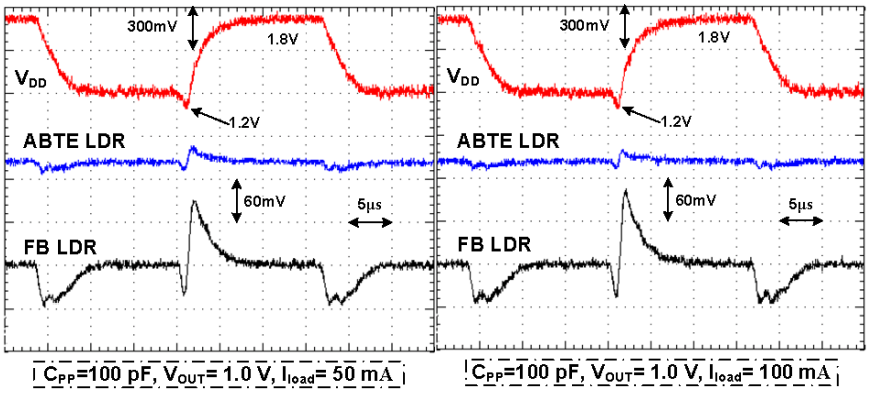
- Miller compensation and Q-reduction (C_M & C_Q)
- Fixed biasing: M_{FB}; Adaptive biasing: M_{AB}; SCM: M_{S1}—M_{S4}
- Transient enhancement: M_{T1}—M_{T9} + C_T: when V_{OUT} shows large undershoot, V_{T1} and V_{T2} decreases → large I_{T9} to pull down V_{GP} quickly → reduce undershoot of V_{OUT}

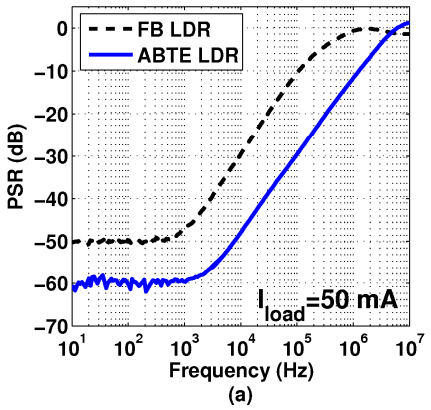
Measurement Results

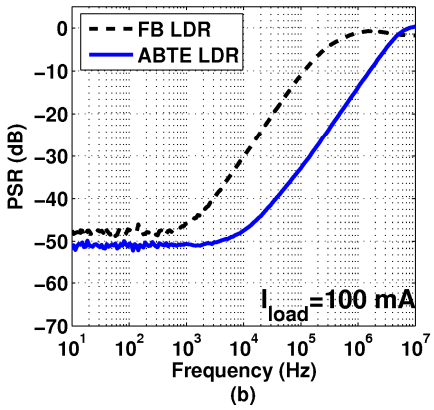




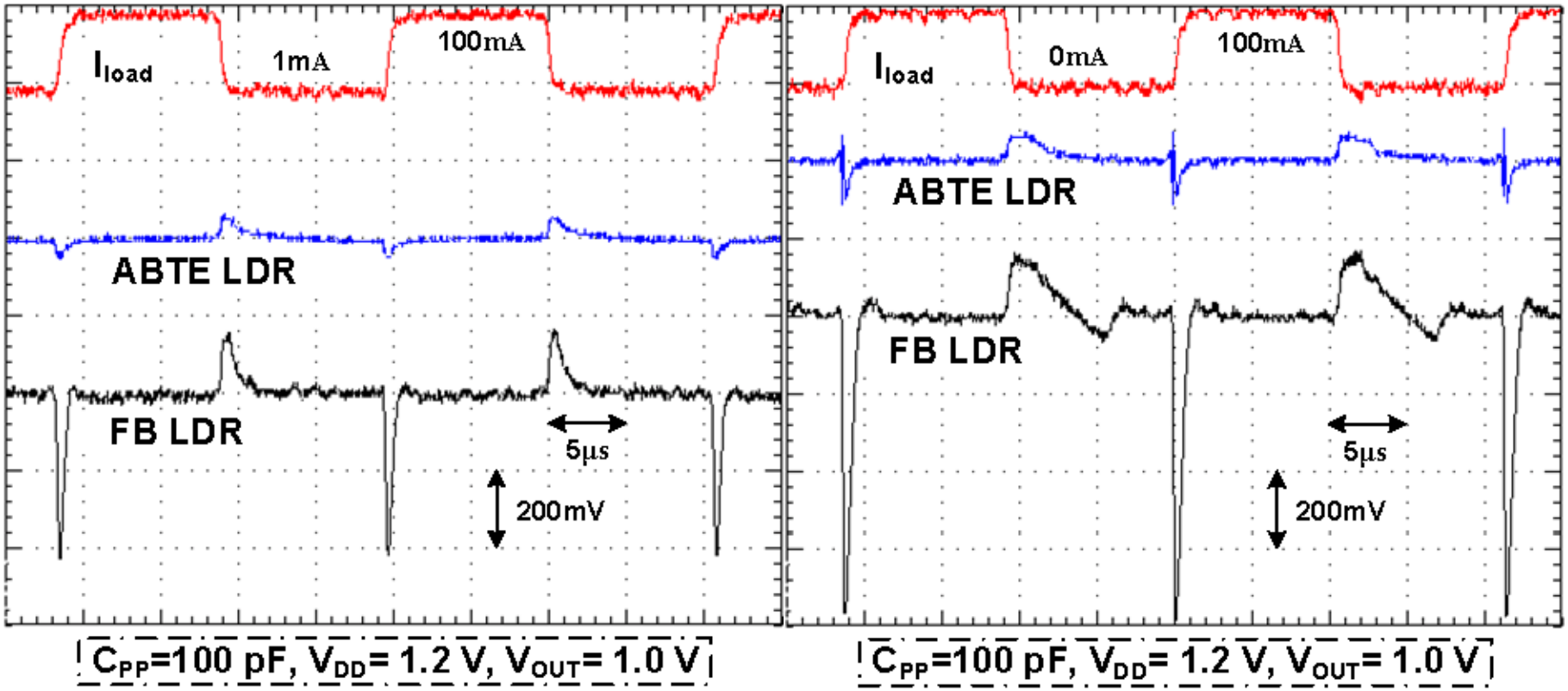








Load Transient



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