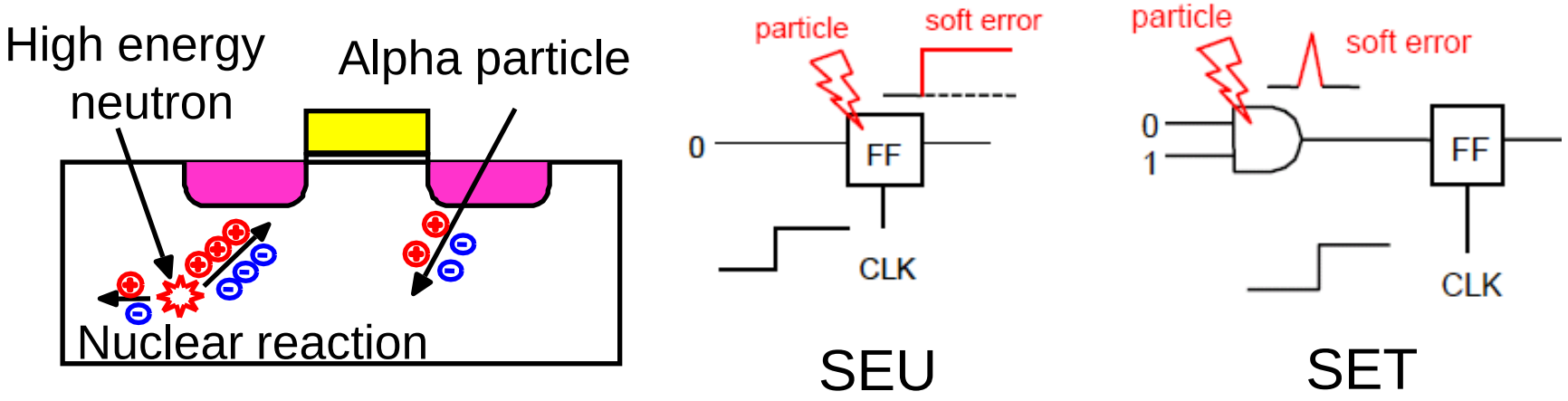
A 65 nm Flip-Flop Array to Measure Soft Error Resiliency against High-Energy Neutron and Alpha Particle



- Process scaling makes LSI less reliable to soft errors
- Soft errors are caused by a particle hit
  - Flips stored value on a Flip-Flop (SEU)
  - Generates temporal pulse on a logic gate (SET)

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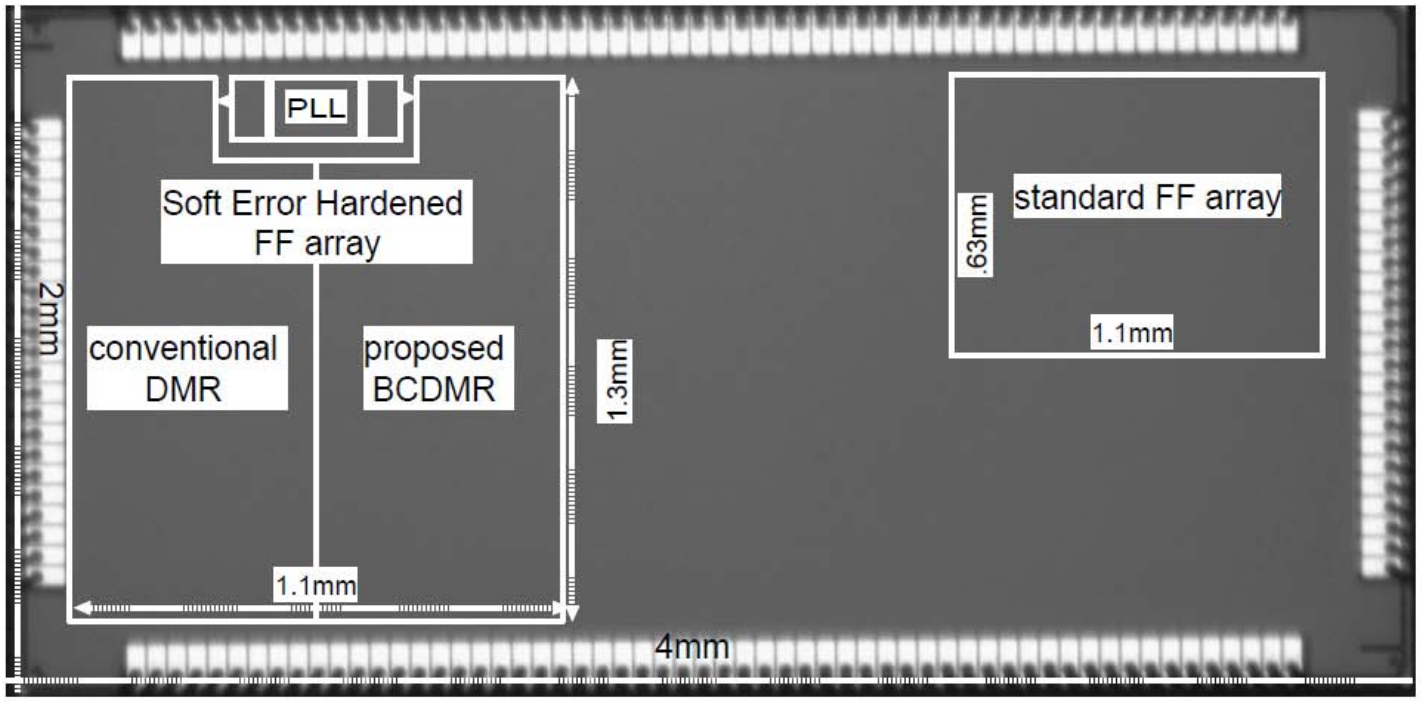
Chip Micrograph



- Fabricate two FF Arrays in a 65nm process
  1. Soft error hardened FFs to compare soft error rates
  2. Standard FF to measure SEU and MCU rates

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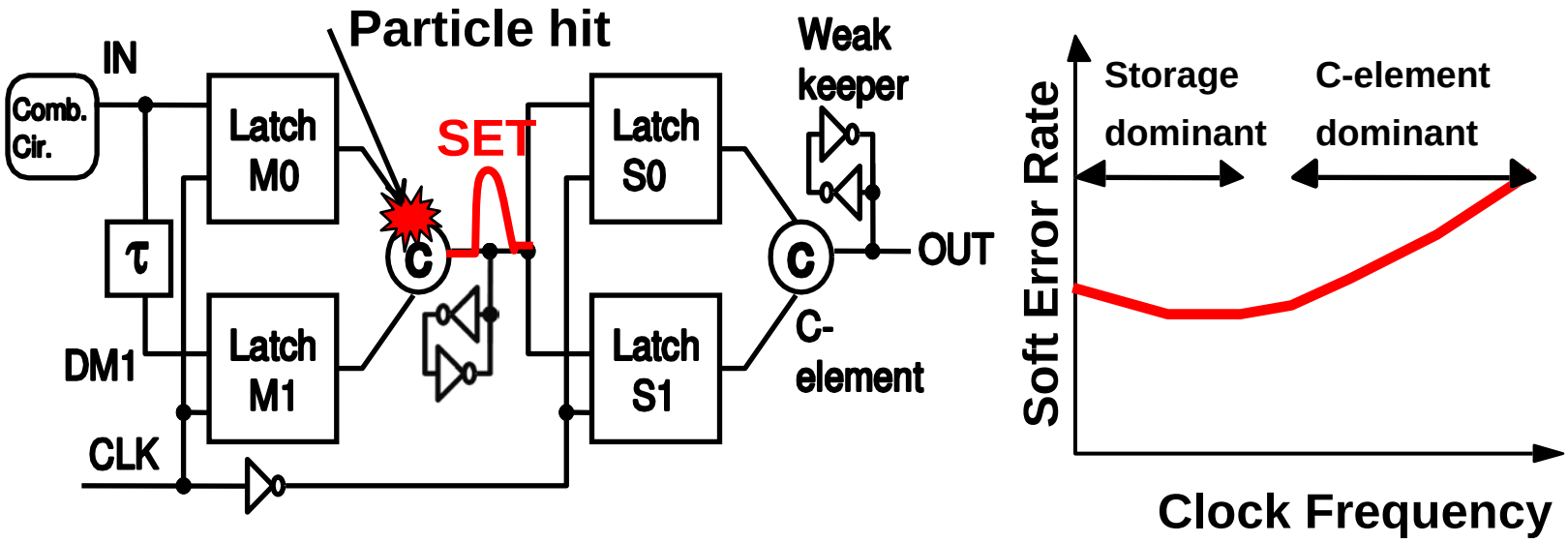
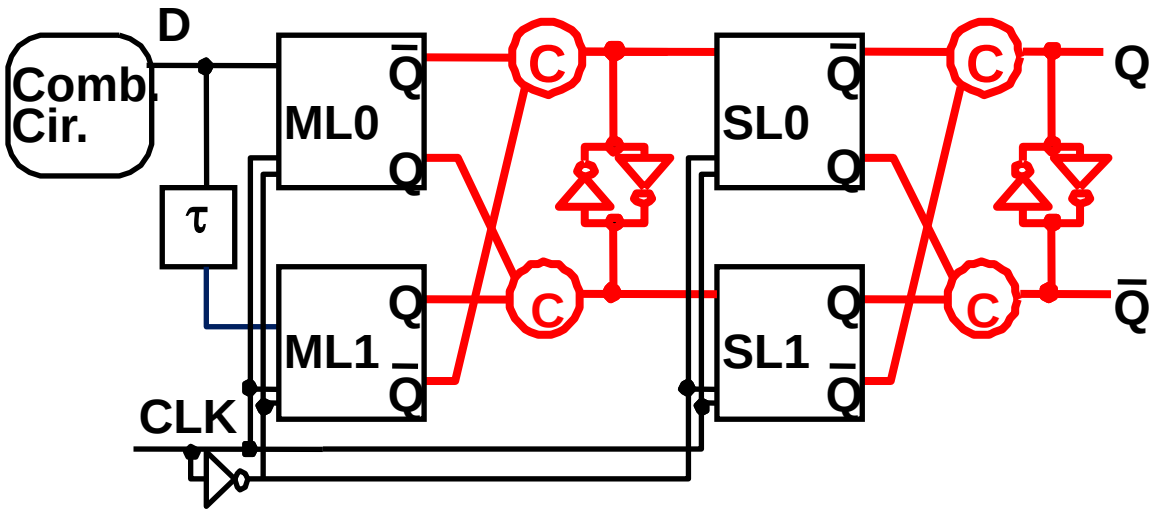
Conventional Soft Error Hardened FF

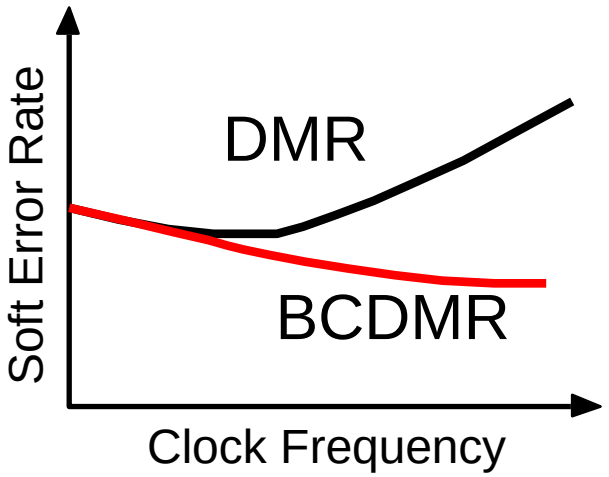


- Conventional DMR(BISER) is weak to SET on C-element
  - Two slave latches capture the SET pulse

Proposed Soft Error Hardened FF

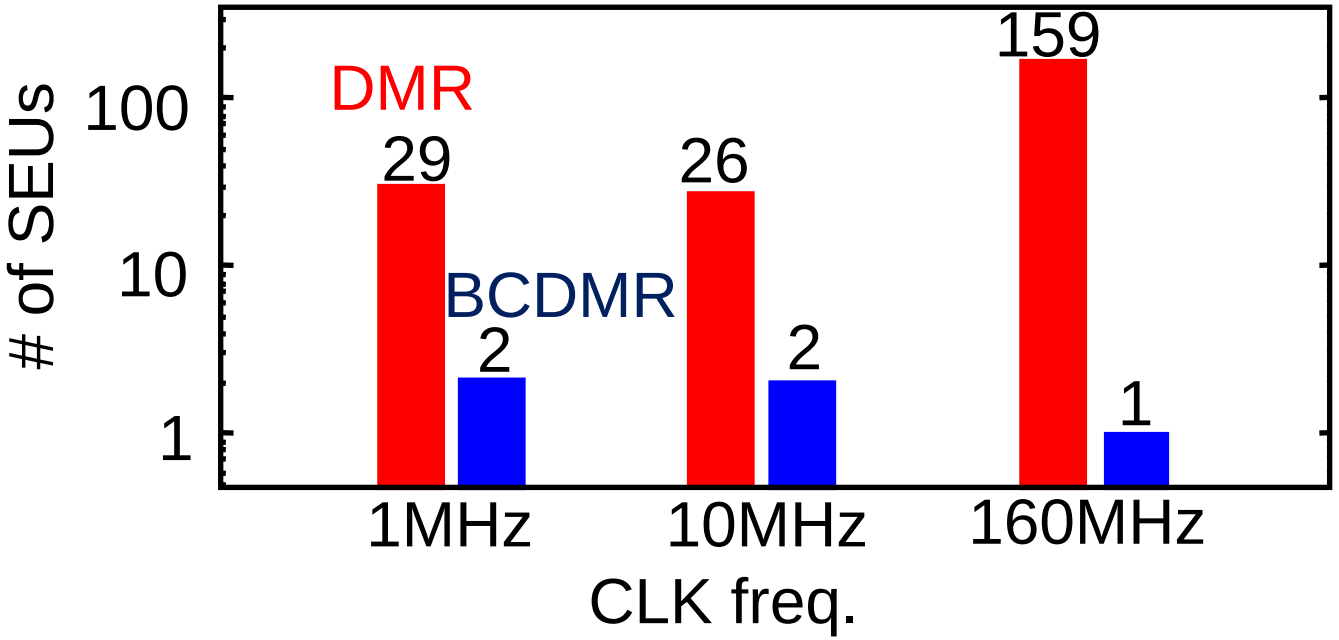


BCDMR



- C-elements are duplicated, and weak keepers are cross-coupled
  - An SET from C-element cannot propagate into both slave latches

Soft Error Rates by alpha particles



Standard FF
= 700,000

- The BCDMR is better than DMR
  - 150x better than conventional DMR at 160MHz
  - DMR is weak to SET pulse on C-element

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Conclusion

- Propose a soft error hardened FF
  - Based on DMR (BISER)
- Measured Soft Error Rates by alpha particles
  - 150x better soft error resilience than DMR at 160MHz
  - DMR has lower error resilience at 160MHz
- Measure MCUs on standard FF by neutron
  - MCU rate depends on distance from tap-cell