Geyser-2: The Second Prototype CPU with Fine-grained Run-time Power Gating

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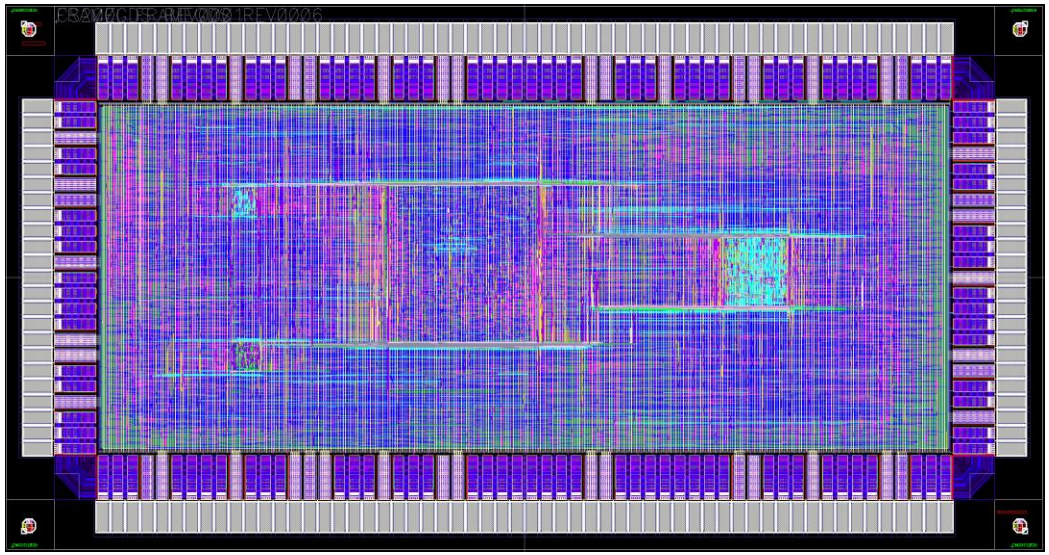
Background: Geyser Project

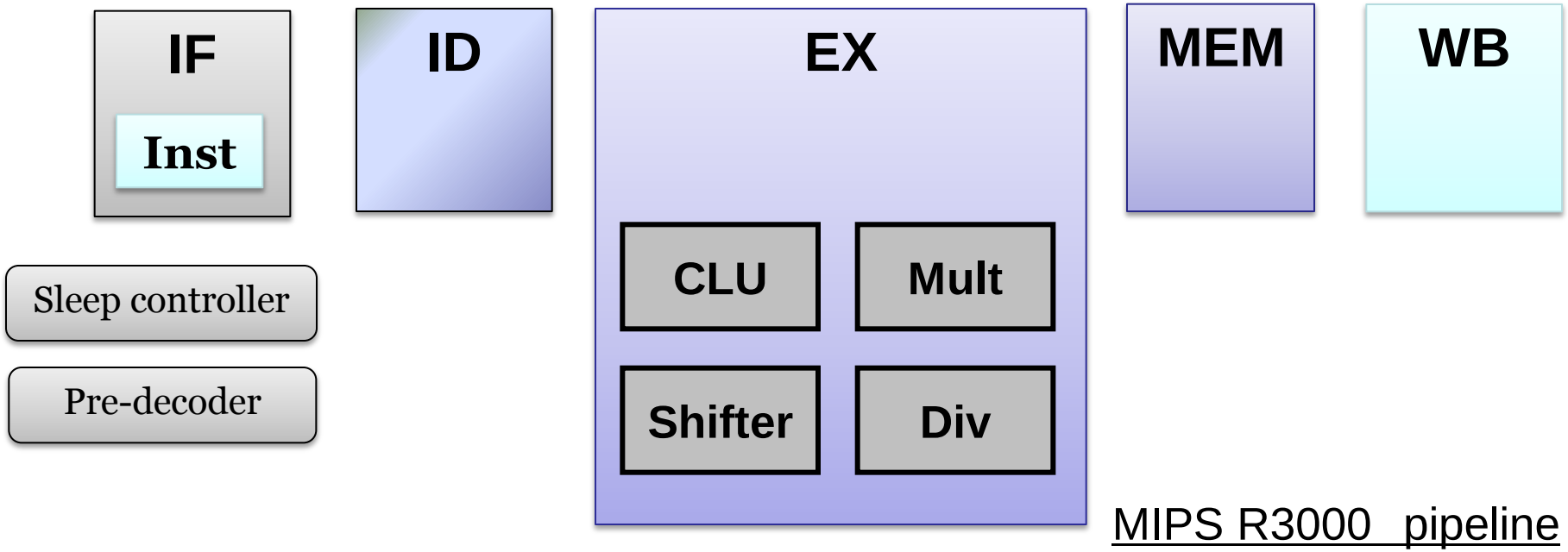
- Aims to establish cross-over techniques for low leakage processor design with integration of architecture, circuits and system software (supported by JST-CREST)
- Geyser-1



- 5-stage standard MIPS R3000 pipeline
- 4 functional units are implemented with fine-grained run-time PG
- Off –chip caches/TLB
- 3% ~ 28% leakage saving with benchmark programs
- 10% area overheads
- 60MHz maximum clock frequency

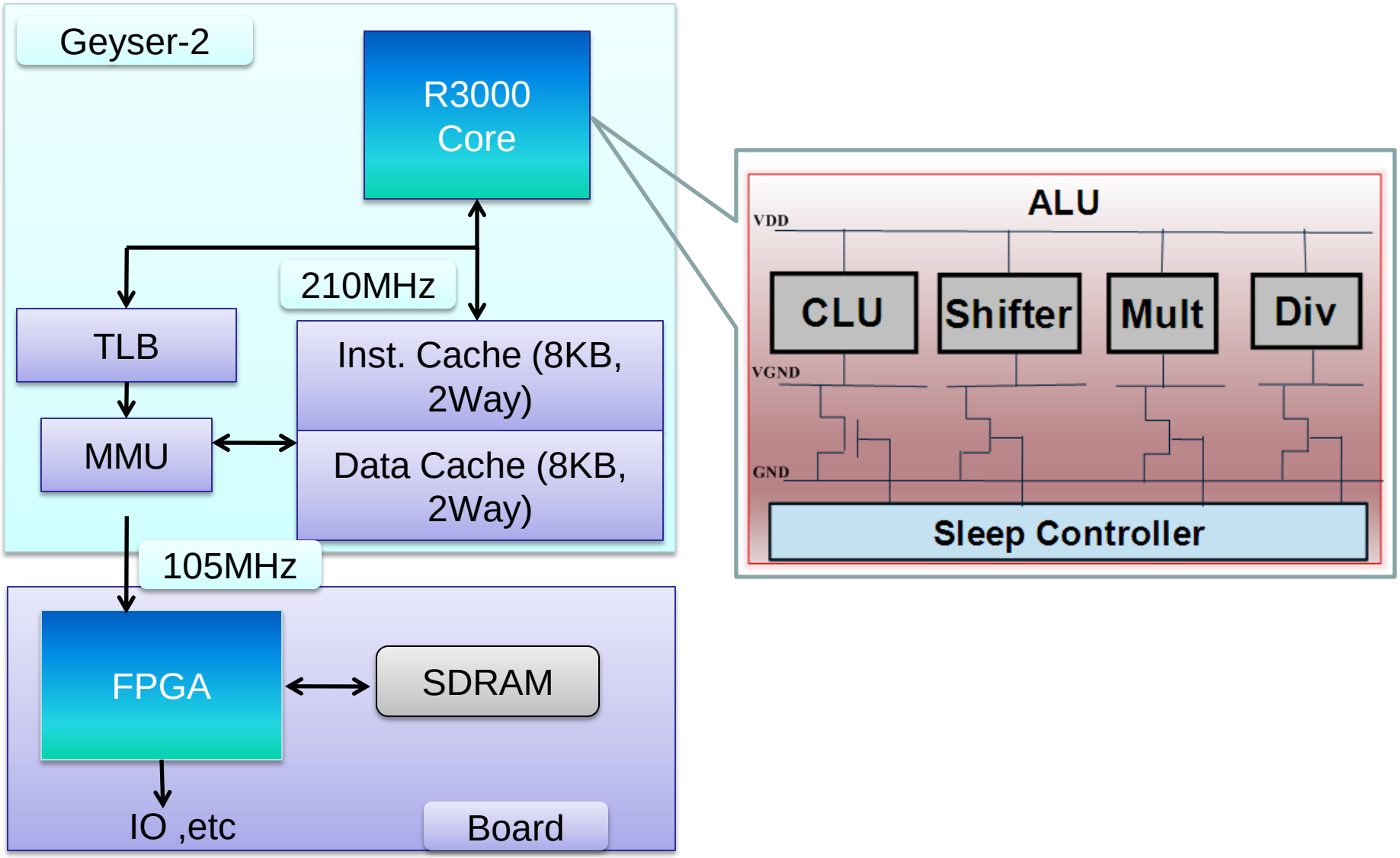
Fine-grained Run-time PG on Functional Units

- A function unit stays in the active mode only when being used
- The pre-decoder in IF stage creates the wake-up signal
- After the operation, the unit will be turned to sleep automatically.

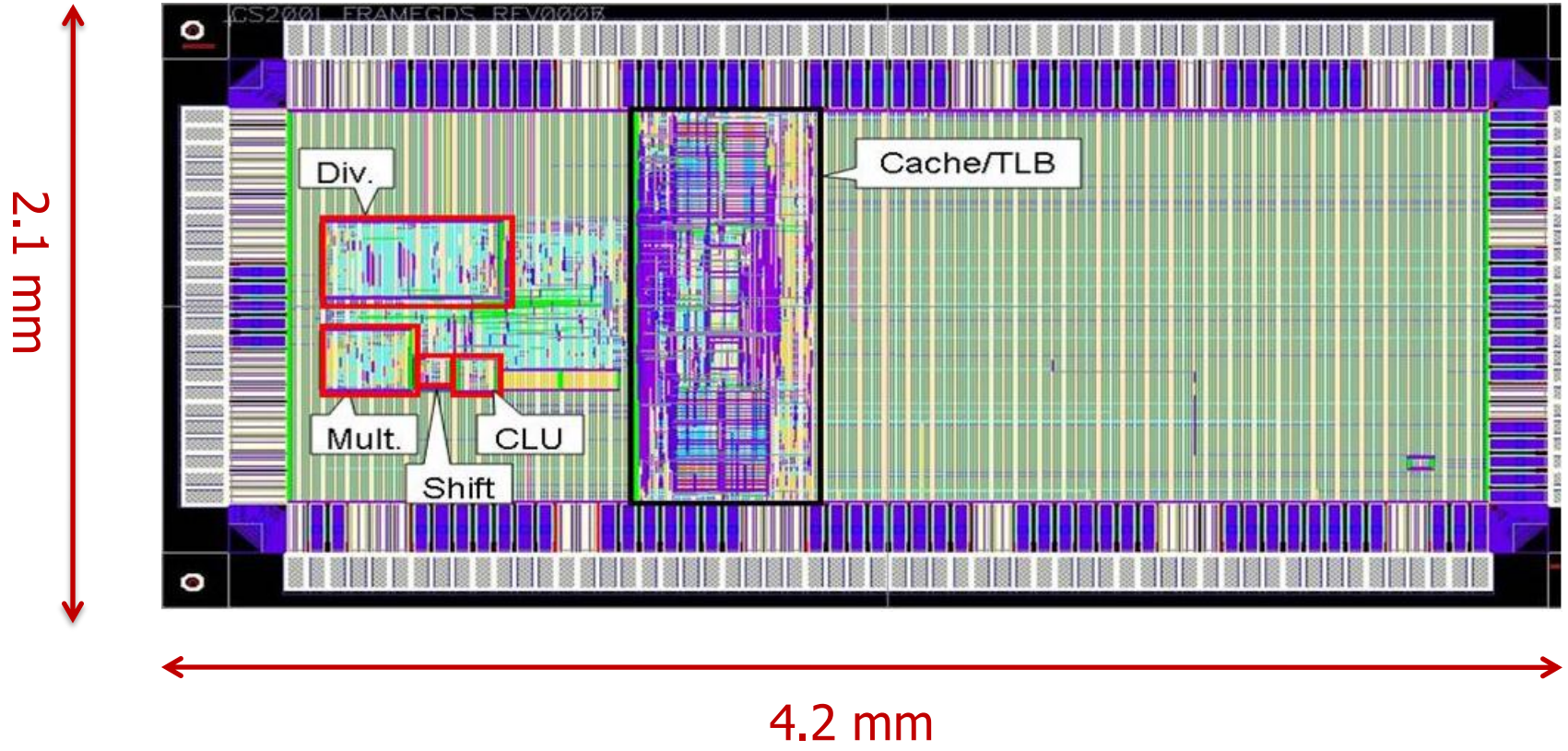


MIPS R3000 pipeline

Geyser-2 Structure



Geyser-2 Layout



Pin-limited design and only half of die area is utilized

Highlights

- Max clock frequency: 210MHz
  - The wakeup latency of all four functional units is less 5ns
- Break Even Time aware leakage control mechanisms:
  - Cooperate with compiler and OS
  - Different leakage control policy at different temperature
- Leakage saving of the processor core: > 60%
  - When all functional units are power-gated
- Area overheads with PG: < 15%
- Leakage saving with benchmark programs is on the way

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