Run-Time Adaptable On-Chip Thermal Triggers

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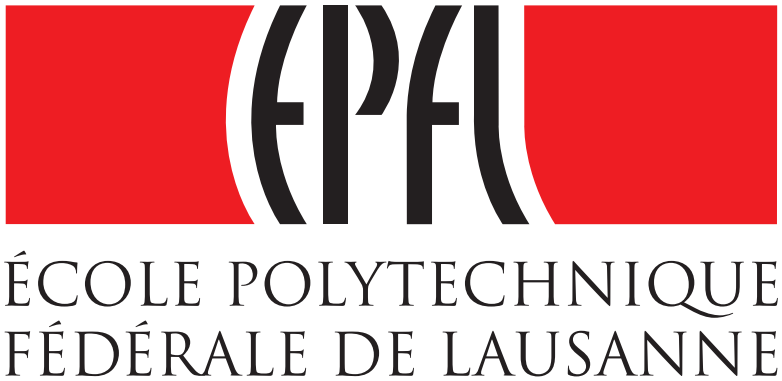
16th Asia and South Pacific Design Automation Conference,

Yokohama, Japan,

26th January, 2011



Outline

1. Introduction
2. Trade-off Space
3. Neural-Network-Based Thermal Simulator
4. Practical extensions to NN simulator
5. Experimental Results
6. Conclusions

The heat is on!

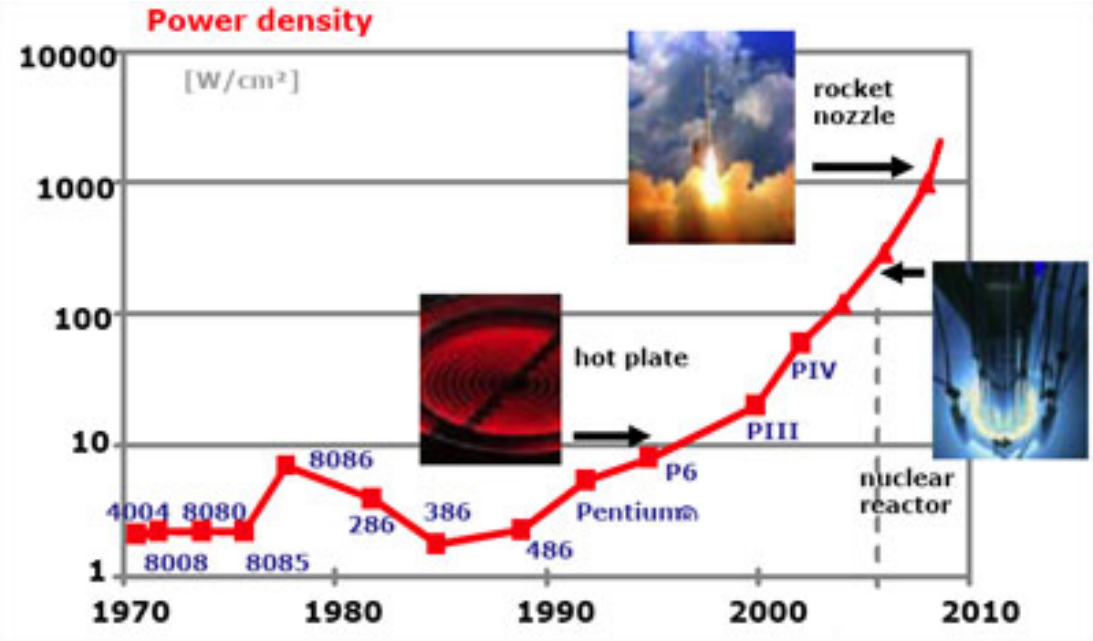


Figure: Rise in on-chip power density. [Source: Intel]

- On-chip power density is rising *exponentially*
- Direct impact: high on-chip temperatures
- Thermal management now a first-class design problem

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- But, when do we *trigger* these controls?

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- What are the *requirements* of a good predictive trigger?

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- Prediction is during run-time. Hence, on-chip resources must be devoted. Thus, computational efficiency is highly desirable
- If prediction engine is modelled at run-time, then we can have errors due to (a) VLSI process variations, (b) thermal modelling errors. Thus, run-time adaptability is required, if these errors are indeed significant

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Qualitative Trade-Off Space

Let us try and qualitatively compare existing techniques to predict on-chip temperatures.

The different classes are

1. Design-time analytical models
2. Software simulators
3. Model predictive control
4. Workload predictive triggers
5. Hardware simulators

Comparison table

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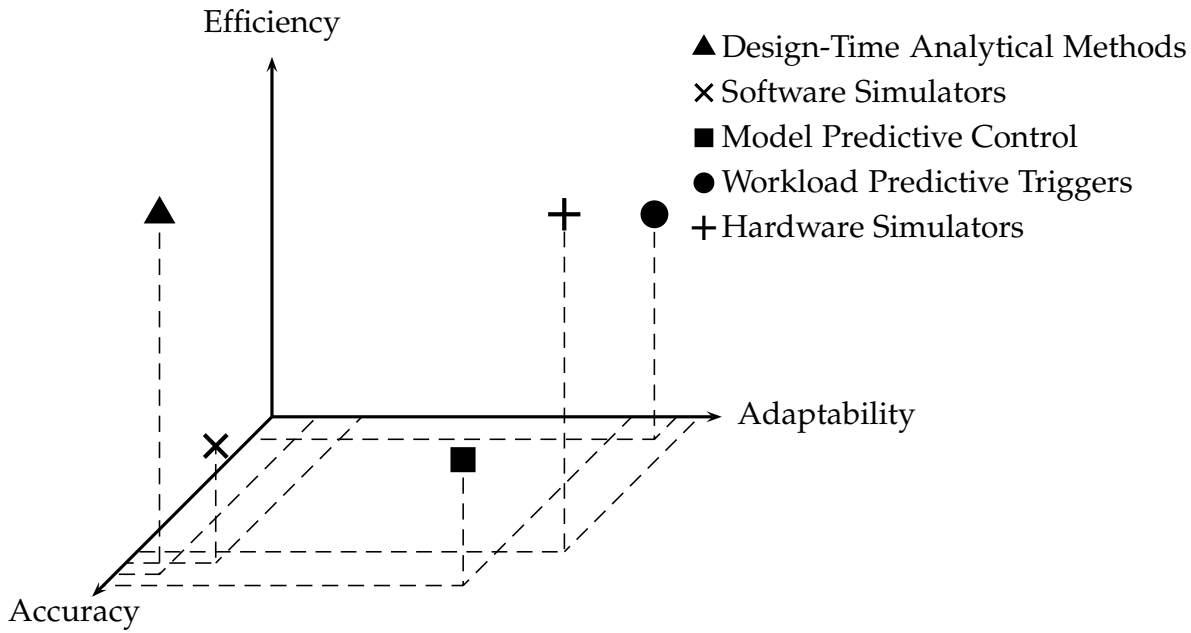

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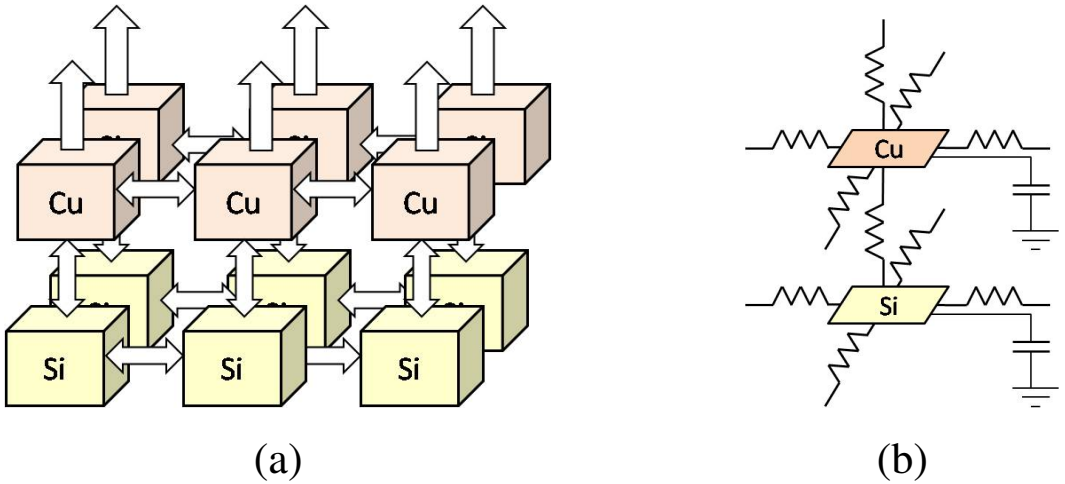
Basics of heat transfer

- Heat transfer represented using the compact thermal model



(a) (b)

- Temperature given by the differential equation

$$GT(t) + C\frac{dT}{dt} = P(t) \tag{1}$$

- The above is a linear time invariant LTI system that can be expressed as

$$T(t_{n+1}) = AT(t_n) + BP(t_n) \tag{2}$$

Neural-Network representation

- A linear neural network mimics the behavior of a system which transforms a vector of inputs $\mathbf{x}$ to a vector of outputs $\mathbf{y} = \mathbf{f}(\mathbf{x}) = w\mathbf{x} + \mathbf{b}$

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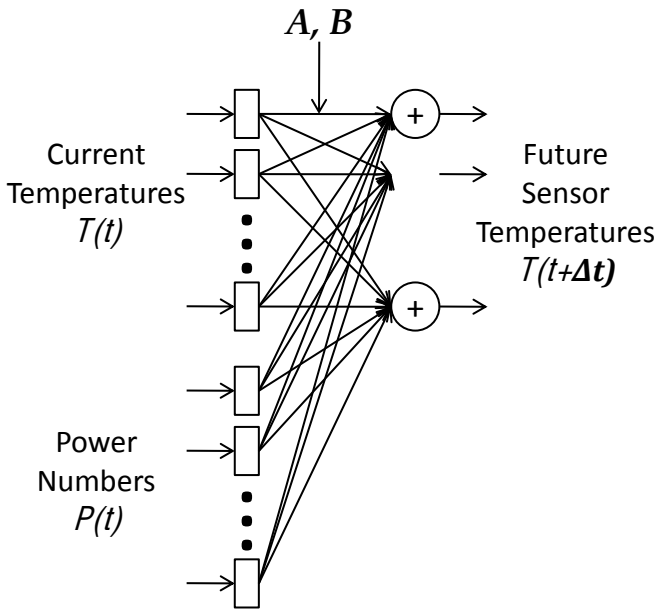
- The thermal LTI system can be *simulated* with a neural network (NN)



- The matrices $\mathbf{A}$ and $\mathbf{B}$ can be learnt by using off-line measurements or design models

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- Implementation

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- **Computation speed**

  An iteration of the LTI model takes only a few gate delays - negligible compared to any software implementation

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- For linear NN, MOR is performed automatically when training with only T_s
- Thus, independent of the number or layout of sensors the NN can be trained and then simulated

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- NNs can be refined during run-time using backpropagation learning methods

$$\Delta w_{ij} \leftarrow \Delta w_{ij} + (y_i^* - y_i)y_j$$

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- What is the hardware implications for on-line refinement?

  1. Every weight term must be programmably stored in say b bits

  2. Run-time learning not as accurate as off-line learning because of quantization of weight terms to b bits

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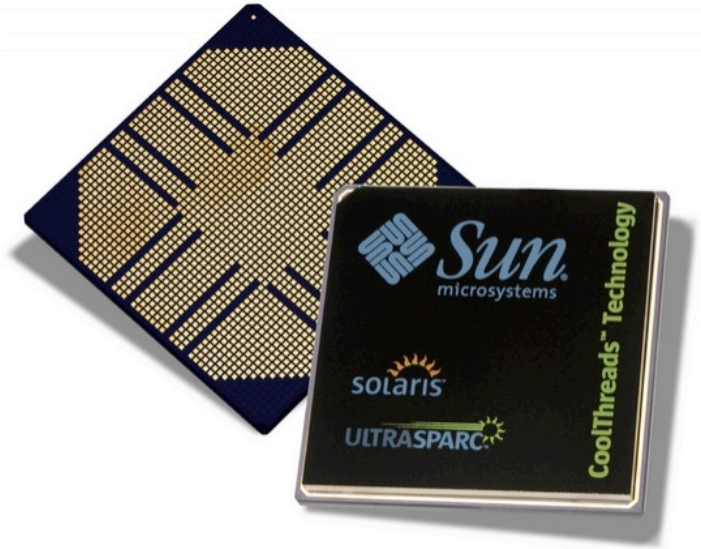
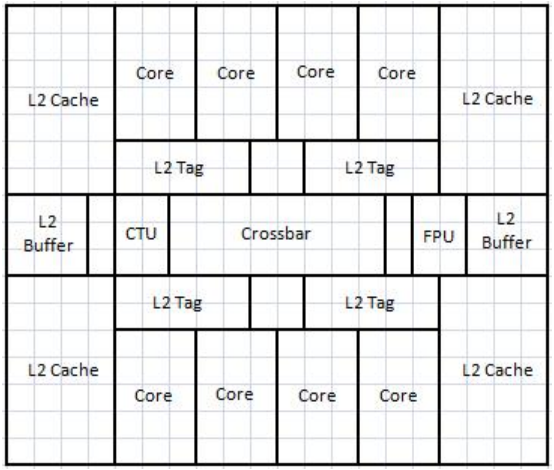
Target system

- 8-core Sun UltraSPARC T1 (Niagara) chip with accurate floorplan
- Accurate thermal properties of the chip derived by an earlier study
- Accurate power numbers derived by benchmark applications running on the same chip





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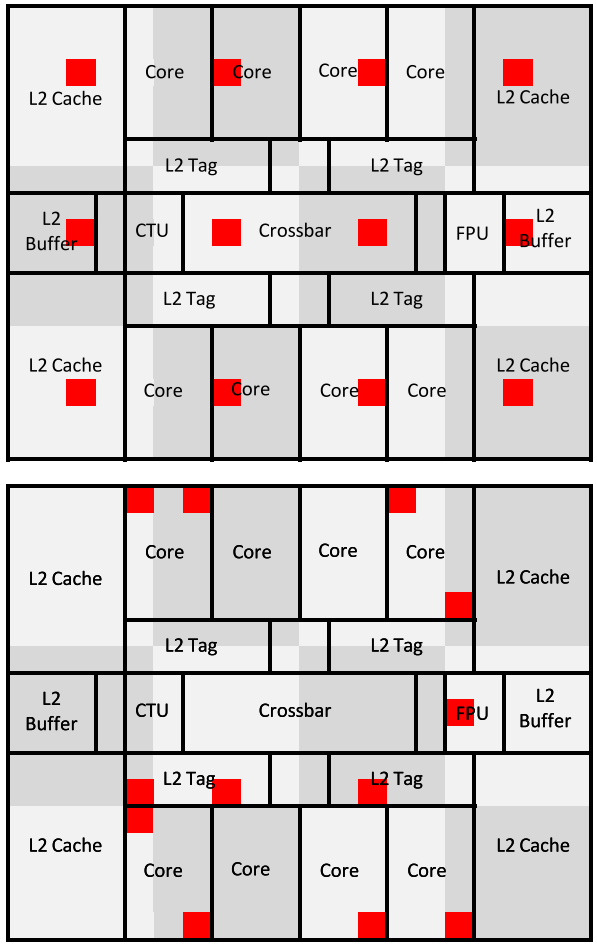
- First experiment to quantify the accuracy
- Does the NN faithfully represent the thermal properties?
- Does the sensor layout affect the results? We consider three layouts:

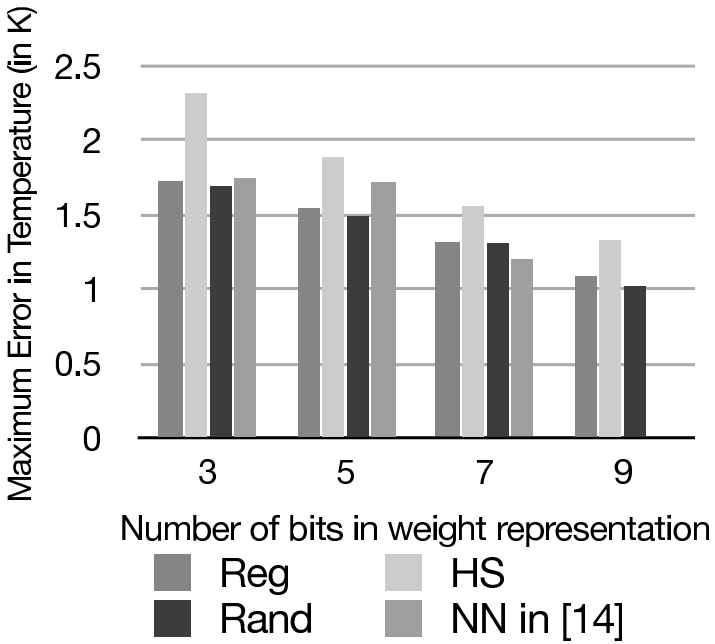
  Reg (figure on top),

  HS (figure on bottom), and

  Rand (randomly generated layouts)



Accuracy of NN simulator - Results



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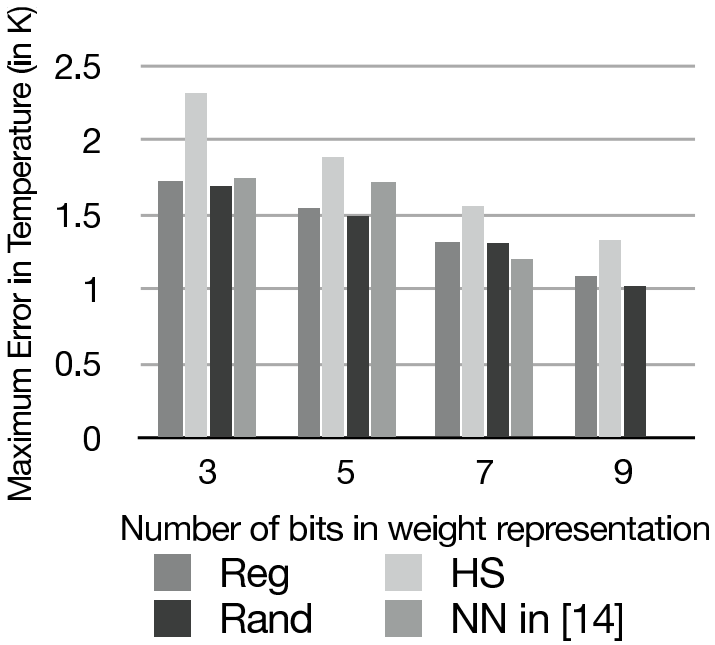

- We plot the results for different values of b - the number of bits in the weight representation
- Clearly, as b increases accuracy increases, for all sensor layouts
- Low errors are noted for all configurations (¡= 1.5K for b = 7)

Adapting to VLSI process variations

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  Further, at higher temperatures leakge current increases exponentially
- Unfortunately, leakge current is highly sensitive to process variations

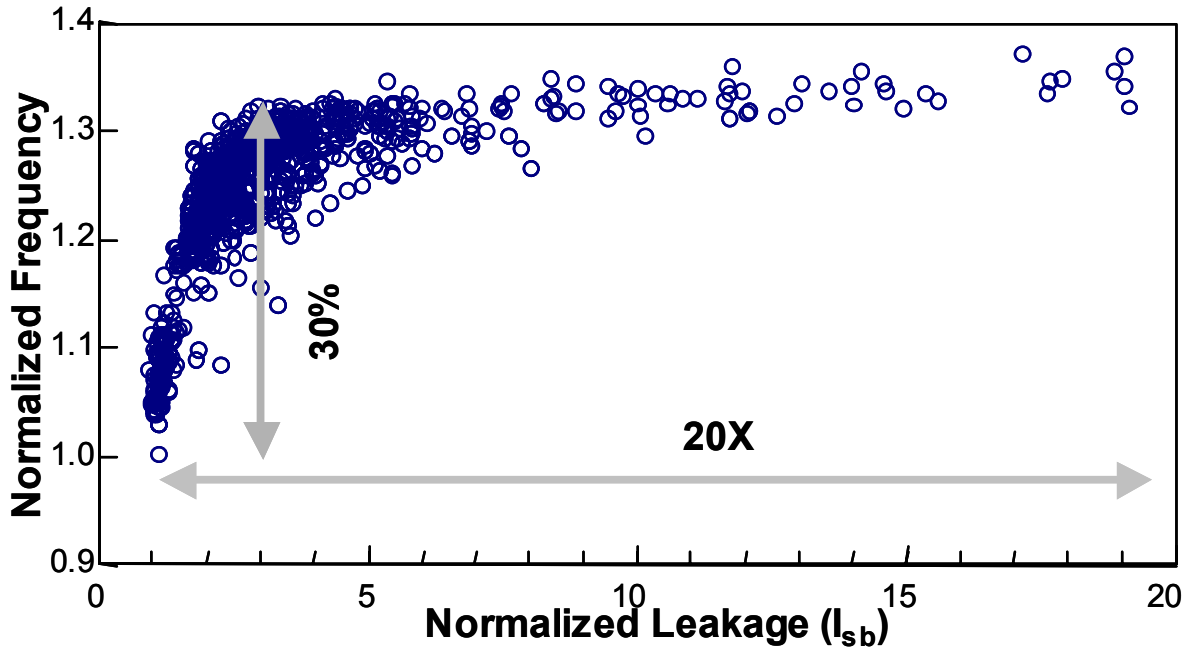

Figure: Leakage current variation for the 180 nm node, [Source: DAC 2003]

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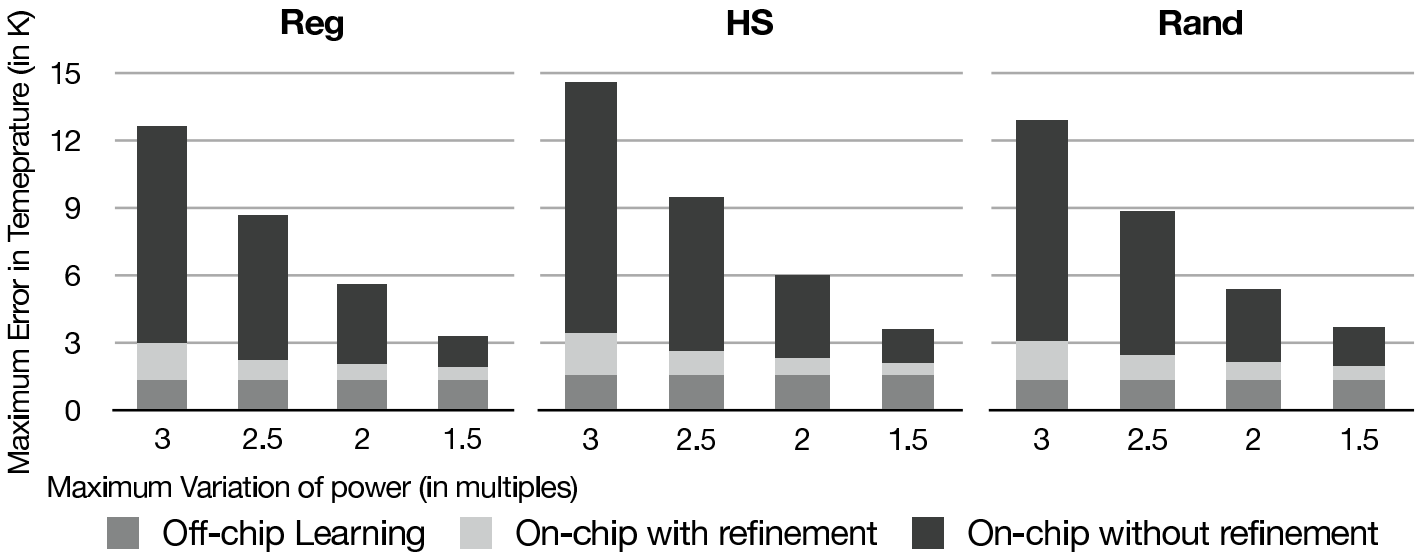

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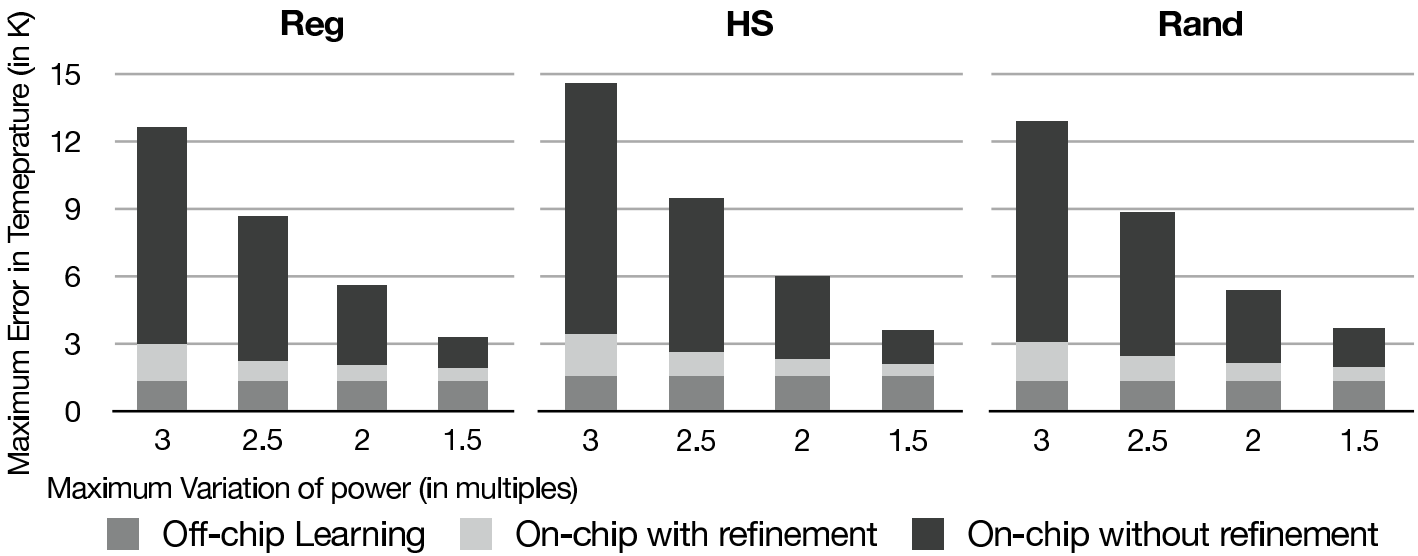

- The good performance of on-chip refinement holds across sensor layout configuration

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- One particular parameter subject to error is conductance to environment denoted as G_{env} - the conductive path to the ambient
- We did not find any study specifically quantifying the variation in G_{env}
- We varied it from +100% to -80% and noted the errors

Adapting to thermal modelling errors - Results

- From our results, fortunately, the errors in G_{env} do not translate to very large errors in temperature (maximum is under 5K)

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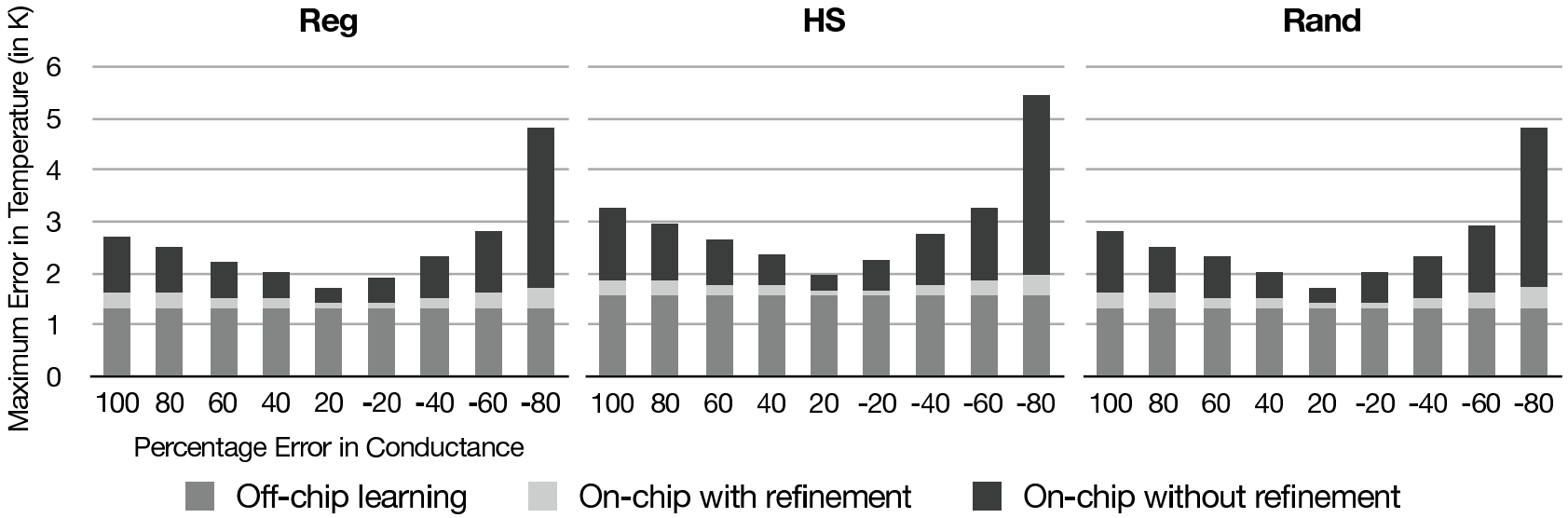
- However, with run-time refinement NNs can nullify even these errors



- Again, refinement works well across sensor layout configurations

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Conclusions and further work

- Run-time thermal management has become a necessity in today's systems
- We compared existing methods of predicting run-time behaviour
- Hardware-based neural network simulators qualitatively out-perform others
- We showed how NN simulators can be used with arbitrary sensor layouts
- We showed that process variations can lead to significant errors in computed temperature (up to 12 K)
- We showed that with run-time refinement, with negligible overhead, NN simulators can adapt to nullify such errors

Thanks