Rethinking Thermal Via Planning with Timing-Power-Temperature Dependence for 3D ICs

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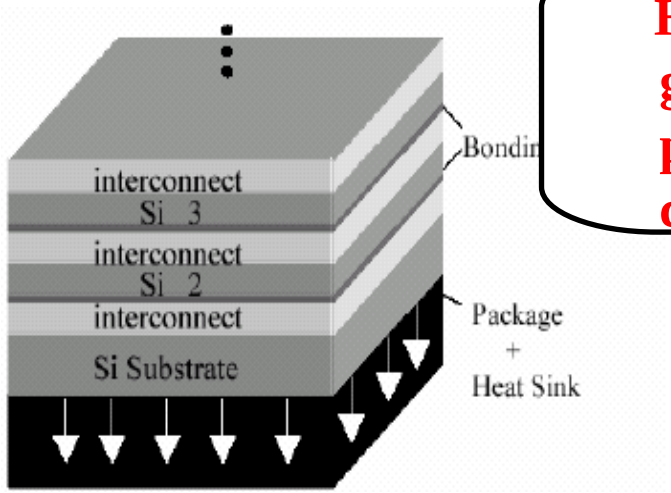
Outline

- Introduction
- Thermal model and leakage power model
- Thermal-driven Via-planning algorithm
- Experimental Results
- Conclusion

Challenges in 3D IC

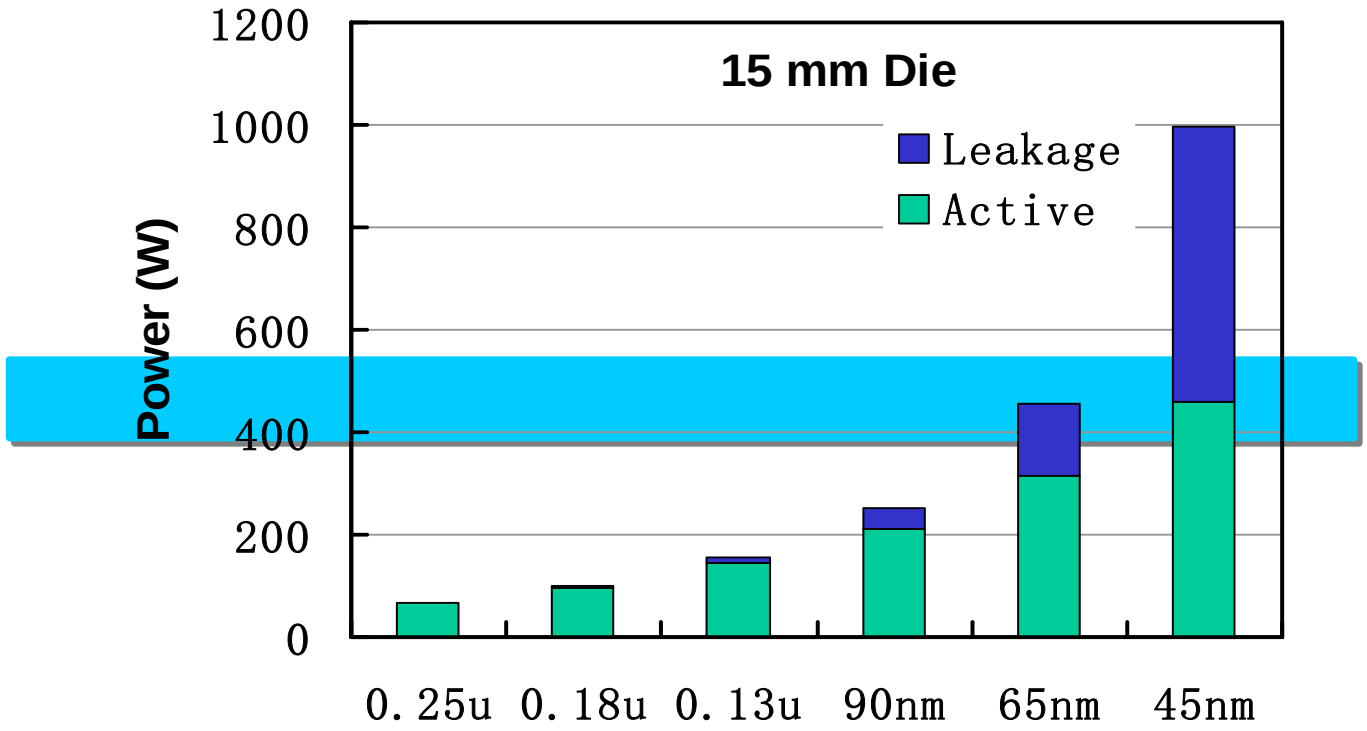
- Three-dimensional (3D) integration
  - More and more popular
  - Decreasing wire delay, increasing integration density and improving performance
  - Faced with heat dissipation and temperature problem due to the increased power density and lower thermal conductivity



High temperature will greatly reduce the performance of circuits.

Power crisis

- leakage power has been more and more and is definitely non-negligible.



Source: Shekhar Borkar, Intel Labs

Leakage Power

- leakage power has been more and more and is definitely non-negligible.
- Leakage power is sensitive to temperature
  - Interacting with each other
  - A chicken-egg problem
  - An iterative computation process is needed to get an accurate value of temperature

Relative works

- Leakage power model
  - Leakage power is relative to temperature [ISLPED'03]
- Thermal optimization
  - Thermal-driven floorplanning or placement [ICCAD04][ISQED06][TCAS-I'07][ICCAD'03] [ASPDAC07][ICCSS08]
  - Thermal-driven routing [ASPDAC'05]
  - But maximum temperature is still too high
- Thermal cooling technology
  - Thermal-through-silicon-vias (TTSVs) [ASPDAC'05][ICCAD'07]

Effectively remove heat

Thermal Via insertion

- Thermal vias bring in additional cost
  - It is expensive to manufacture thermal v
  - Take dead-space, create routing conge lead to longer interconnects and larger delays.
- Thermal via planning methods
  - Nonlinear programming problem[ASPDAC'05], Redistributed dead-space [15,16] and L relaxation method [17]
  - However, most of works didn't taken lea power into account.
- White-space resource constraint
  - [3] proposed that the via space is only 26% of the total white space area instead of fully used

Minimize the total Via number

Lead to estimation error

Contribution in this paper

- An exploration approach for TSV planning
  - Iterative TSV planning considering leakage-delay-temperature dependence
  - Performance aware TSV planning with resource constraints
  - Weighted via planning with power-temperature-timing evaluation

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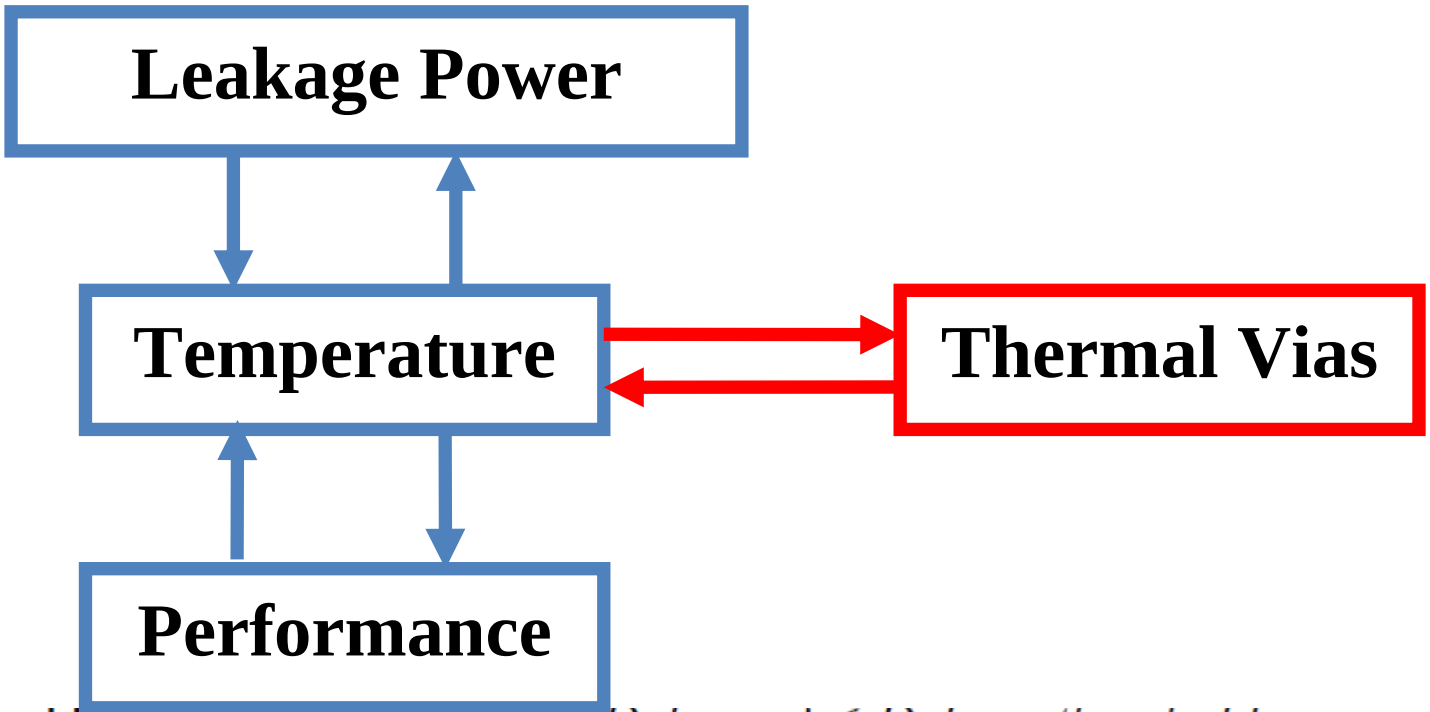
Problem Description

- Thermal model
  - Estimate temperature profile



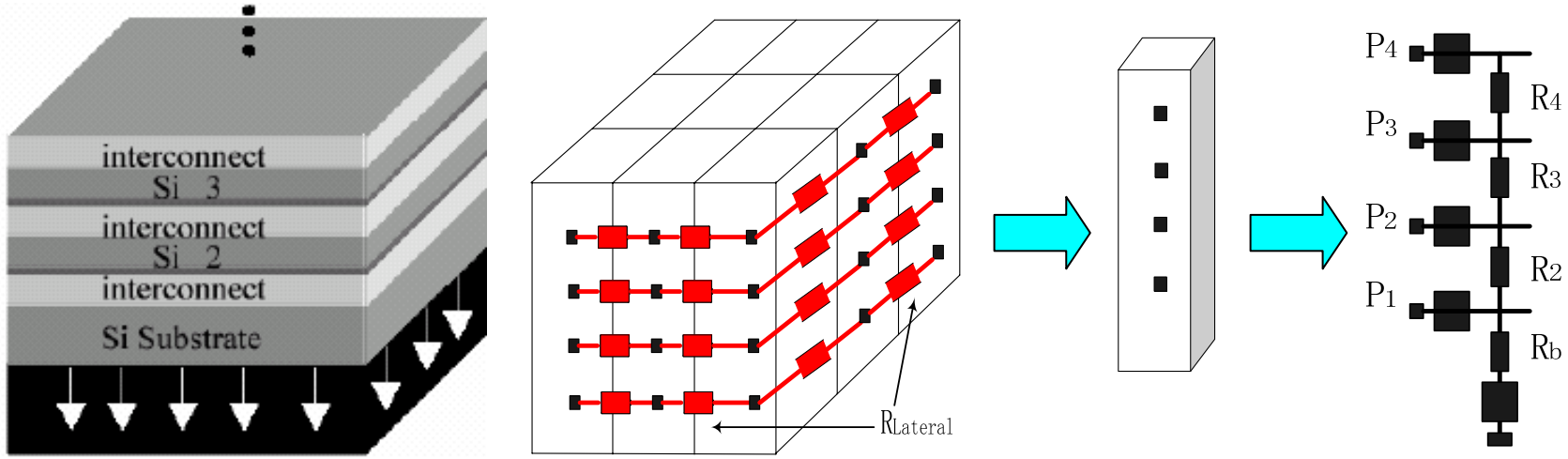
b. Delay constraints: $Max\{Delay_{path}\} \le Delay\_threshold$

c. Dead-space resource constraints:

$$A_{via} \times VN_{i,j,k} \le Area^{ds}_{i,j,k} \times via\_ratio$$

Thermal Model

- The computation of leakage depends on temperature profile, temperatures are calculated by thermal model
- Circuit stack partitioned into tile stacks
- A tile stack is modeled as a resistive network.
  - Determine the thermal profile as a function of power profile

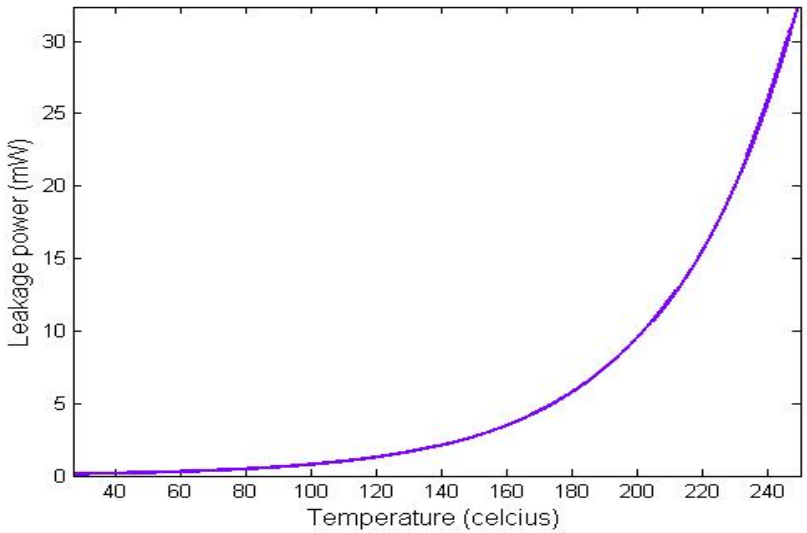


Leakage Power Model

- Temperature-dependent leakage power model
  - The leakage power of a grid cell *i*

$$P_{leakage-i} = A_i \times \alpha \times e^{\beta \times (T_i - T_{base})}$$

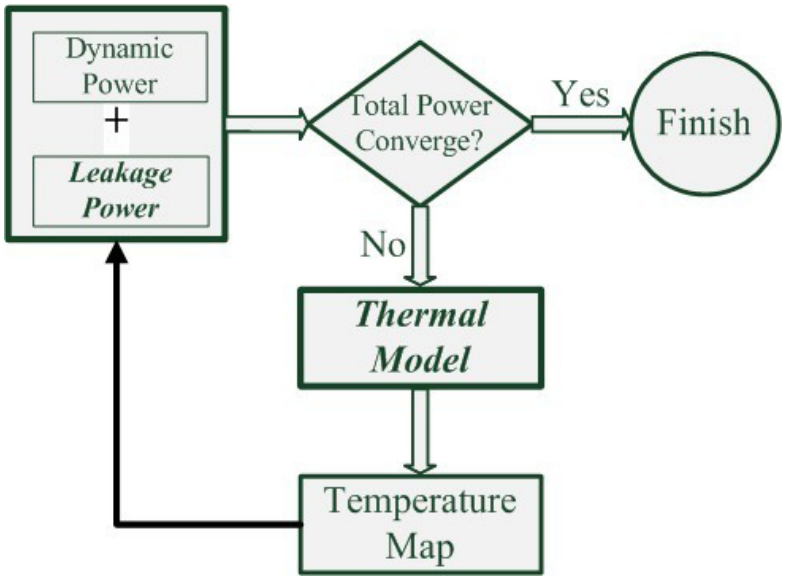
    - *Ai* :area of the cell *Ti* :temperature of the cell
    - α = 100000 W/m^2 and β = 0.025 for 130nm
    - *Tbase* is the reference temperature at which α and β are defined. *Tbase*=110℃.
  - Spice simulation shows the error is within 10%

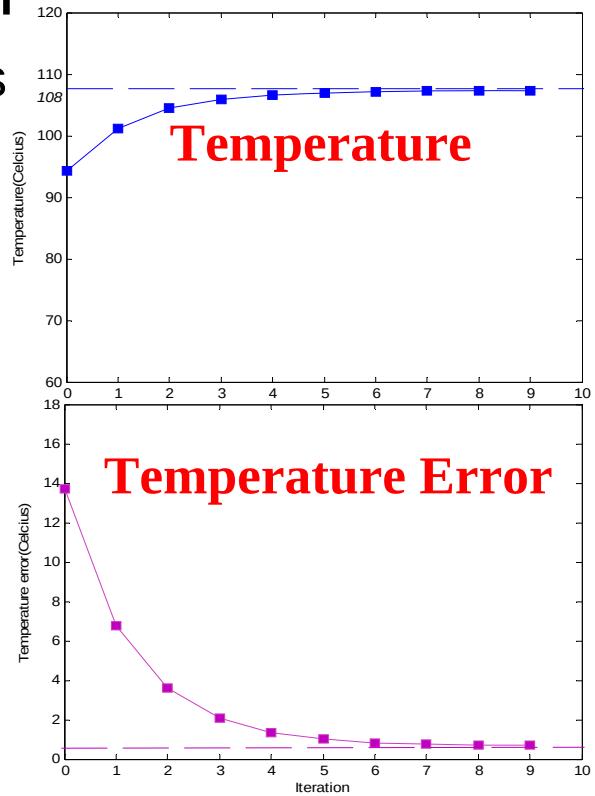


The leakage power increases with the temperature super-linearly.

Iterative thermal analysis

- Leakage power and temperature value are interacting with each other
  - An iterative computation process





Iterative computation loop 2 or 3 iterations are enough to get an accurate estimation.

Delay-Temperature Dependence

- Delay-temperature dependent model:

$$delay(T) = \frac{delay(T_0)(V_{DD} - V_{TH}(T_0))^{\alpha} T^{\beta}}{T_0^{\beta}(V_{DD} - V_{TH}(T_0) + k(T - T_0))^{\alpha}}$$

Where $k = k_0 + \gamma (T - T_0)$

- The values of α, β, γ, k0 are in [DAC'06]:

k_0 (mV/K)	γ (mV/K)	α	β
1.2	0.003	1.3	1.5

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- Thermal model and leakage power model
- Thermal-driven Via-planning algorithm
  - Impact of leakage power on temperature
  - Via Estimation and Iterative Via Planning
  - Weighted TSV insertion algorithm and evaluation method
- Experimental Results
- Conclusion

Thermal Impact of leakage power

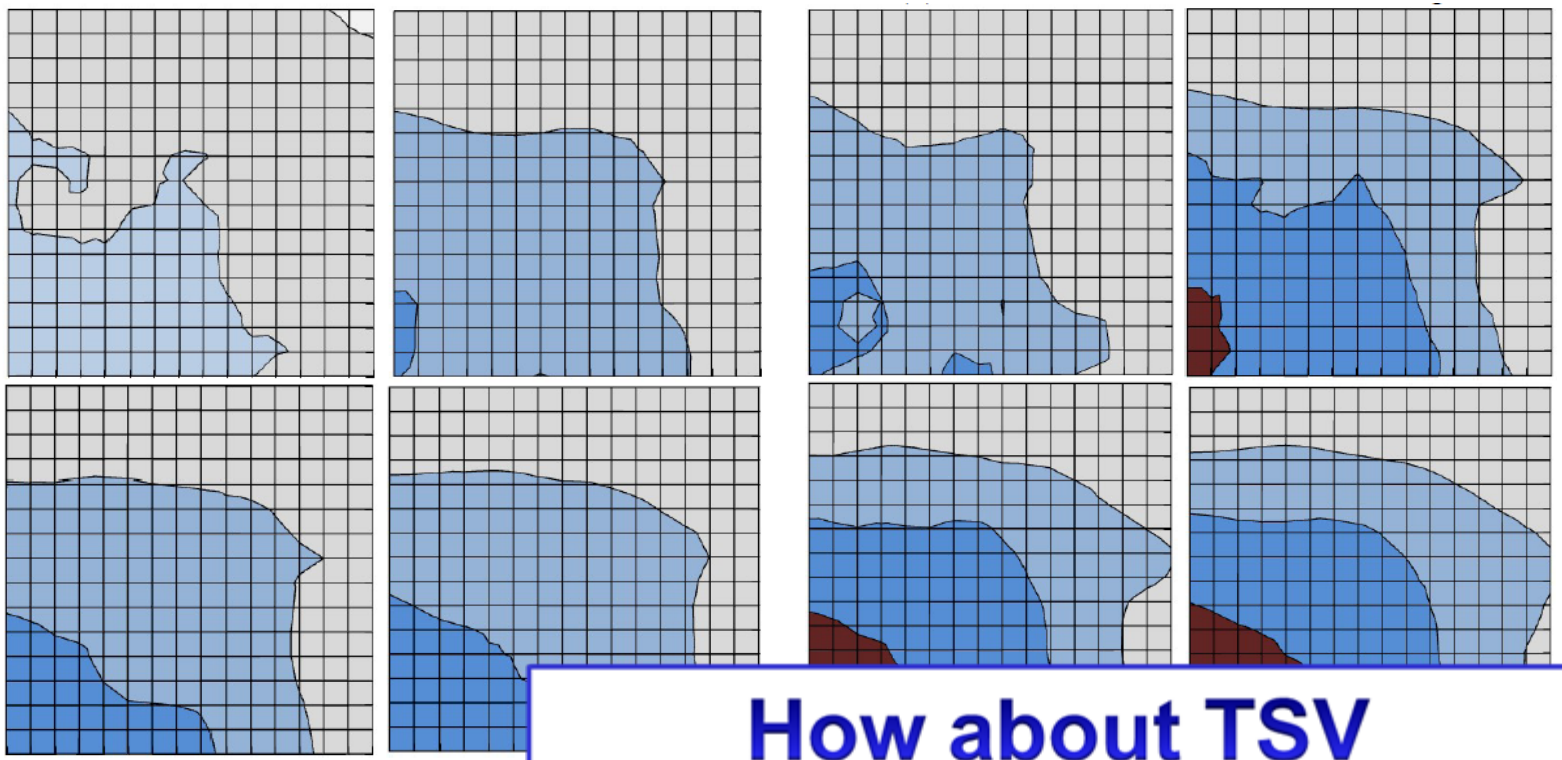
- **Without leakage power considered, temperature estimation can have about 50% error.**

Thermal Impact of leakage power on temperature

Circuit	*Area*	*HPWL*	*Max Temperature*	
			With FLP	**With TDLP**
Ami33	39.2	21.1	136.2	212.2 (+76.0)
Ami49	1392.9	411.2	128.0	204.8 (+76.8)
N100	5.4	90.9	117.3	175.4 (+58.1)
N200	6.1	164.6	123.3	187.9 (+64.6)
N300	8.8	224.6	135.7	198.6 (+62.9)

Temperature distribution with leakage

- **Thermal distribution without leakage and with leakage considered on 4 layers**



(a) Without leakage p
Ther

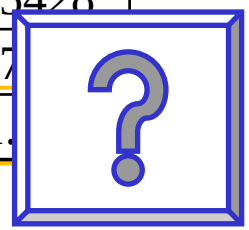
How about TSV Number?

Impact of leakage power on via number

- **Considering leakage power result in increase of the total required number of vias greatly**

Impact of leakage power on temperature and via number

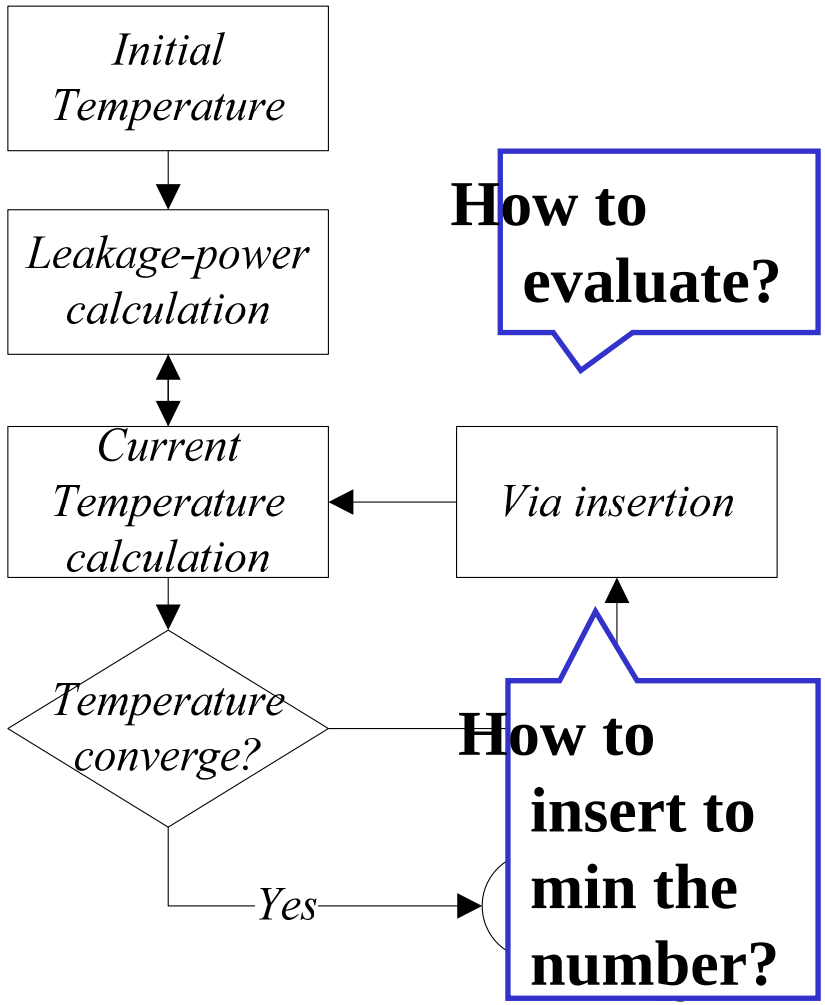
Circuit	*W/O leakage (NLP)*			*With Leakage (CLP)*		
	Initial T (℃)	T with TTSV (℃)	#Via	Initial T (℃)	T with TTSV (℃)	#Via
Ami33	152.9	76.8	562	175	75	642
Ami49	215.4	107	31378	277	118	58042
N100	144	77	4728	177.3	80	5294
N200	185.7	80	7879	212	79	8570
N300	258.7	80.1	13094	293	79	15428
Avg	191.3	84.2	11528	226.9	86.2	17
Ratio	1	1	1	1.186	1.024	1.



To reach the required temperature after TSV Insertion

Iterative Via Planning

- Pre-Estimated
  - Estimate the total number before actual insertion
    - Consider black space for thermal vias
  - Enough, the temperature can directly reach the target temperature
    - calculate the leakage power from the final temperature.
  - Not enough to reach the target temperature;
    - a few iterations are needed to obtain the convergence,



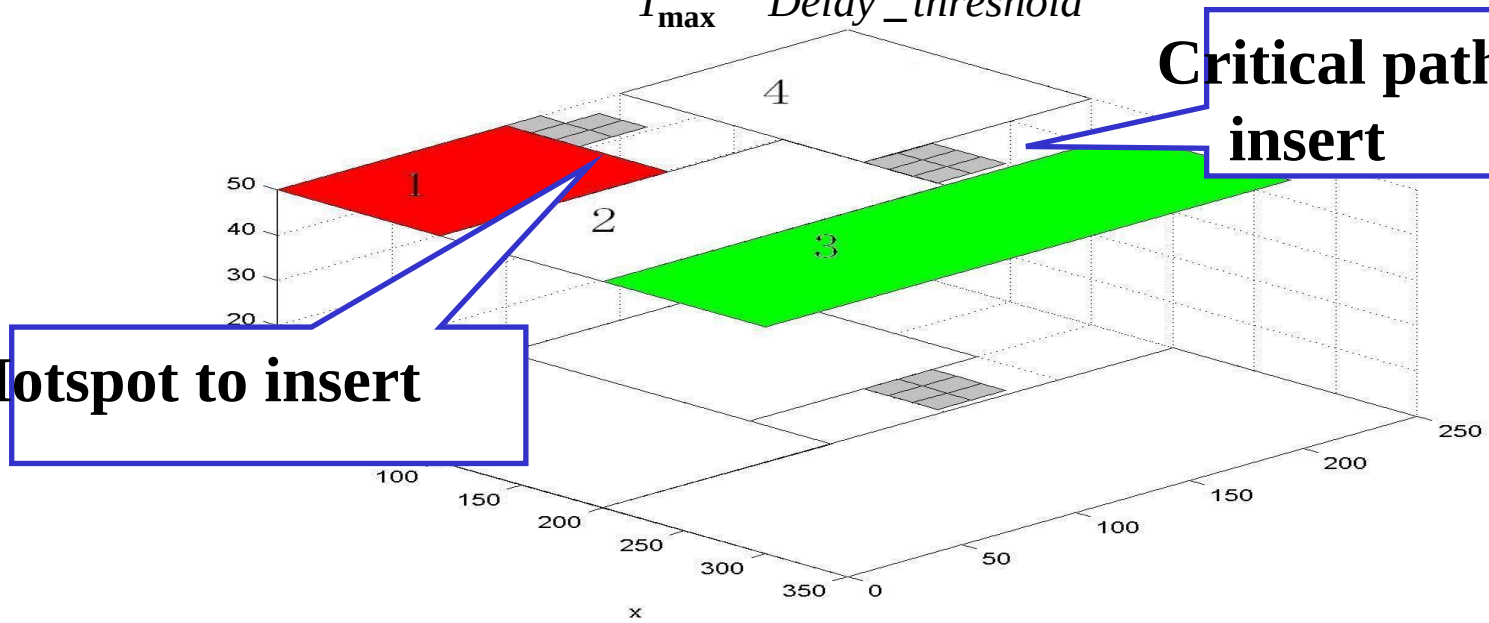
Weighted TSV insertion

- Two kinds of weights:
  - $W_{leakage}$: to evaluate leakage criticality

$$W_{leakage}(b_i) = \alpha \times \frac{T_{bi}}{T_{\max}} \times \frac{P_{bi}}{P_{\max}}$$

  - W_{delay} : to evaluate delay criticality **between (0, 1)**

$$W_{delay}(b_i) = \frac{T_{bi}}{T_{\max}} \times \frac{delay(T_0)}{Delay\_threshold}$$



Evaluation Function

- ***To Evaluate the solution:***
  - *1.Balance Function:*

$$Bal(T,d,n) = \alpha \cdot (T - T_{low}) + \beta \cdot delay + \gamma \cdot via\_num$$

Balance the weight of temperature, delay and via number

  - *2.Punish Function:*

$$M(T,d,n) = \begin{cases} M & T > T_{up} \\ 0 & otherwise \end{cases}$$

Penalty high temperature

  - *3.Cost Function:*

$$Cost(T,d,n) = Bal(T,d,n) + M(T,d,n)$$

Evaluate performance aware TSV insertion solution

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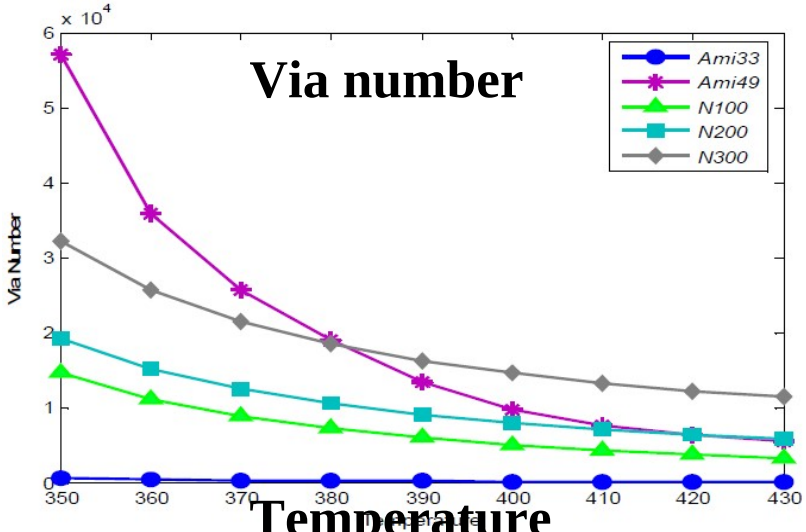
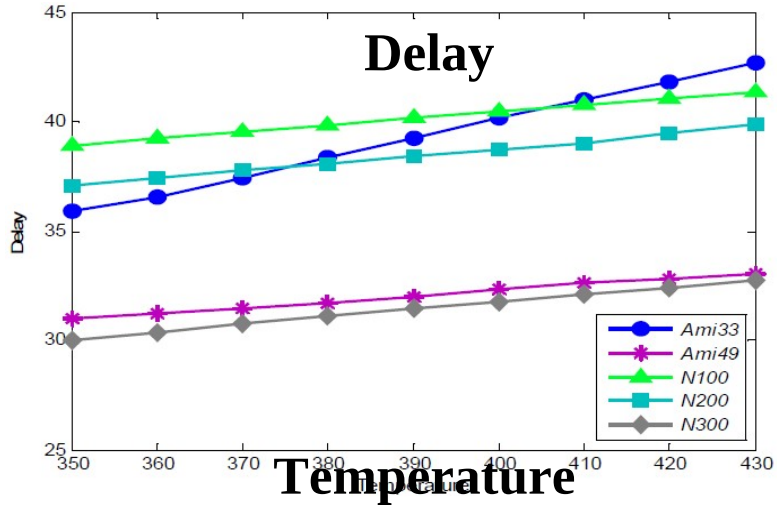
Impacts of T-delay-power dependence

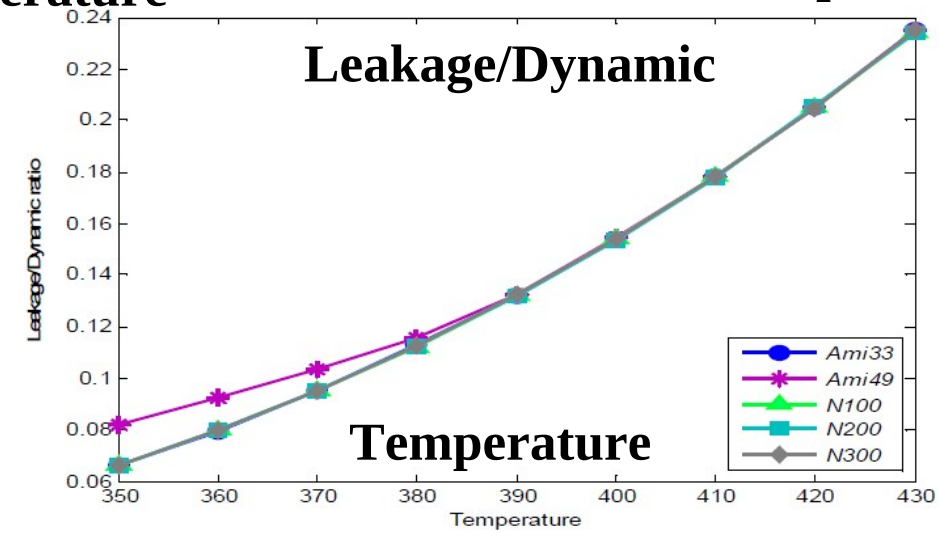
Impact of thermal-driven floorplanning with leakage power

Test cases	*Required T*	*Max T*	*Normalized Delay*	*Via Number*	*Leakage/ Dynamic*	*Run Time* (s)
Ami33	350	350.09	35.90	548	0.0662	7.06
	380	380.14	38.34	243	0.113	7.97
	410	410.00	41.00	126	0.178	8.39
Ami49	350	361.74	31.02	57179	0.0821	4.43
	380	381.60	31.72	18967	0.115	4.70
	410	410.09	32.61	7553	0.178	5.66
N100	350	349.80	38.87	14641	0.0658	12.08
	380	379.85	39.85	7309	0.112	11.4
	410	410.02	40.76	4329	0.178	15.37
N200	350	349.86	37.10	19237	0.0659	16.61
	380	379.95	38.09	10545	0.112	17.72
	410	409.82	39.53	7174	0.178	17.20
N300	350	350.03	30.01	32130	0.0661	16.98
	380	379.94	31.09	18534	0.112	22.08
	410	410.13	32.10	13248	0.178	18.07

Impacts of T-delay-power dependence







Impact of thermal resource to Via Number

- **With thermal resource considered, vias required can be much more, by about 76.0%.**

Impact of *via_ratio* in Ami33

via_ratio	***Required T(K)***	***Max T(K)***	***Delay***	***Via Number***	***Max L/D***	***Runtime (s)***
1	350	349.95	36.84	1328	0.0660	3.55
0.6	350	349.80	36.82	1953	0.0658	3.75
0.2	350	375.44	37.54	1409	0.0769	4.13
1	380	380.05	39.29	633	0.1126	4.63
0.6	380	380.05	39.27	672	0.1121	5.13
0.2	380	380.15	39.26	1114	0.1123	5.41
1	410	409.92	41.54	443	0.1779	4.39
0.6	410	409.92	41.55	436	0.1779	5.23
0.2	410	409.90	41.47	547	0.1782	5.35

Effect of weighted TSV insertion

- **Weighted approach can result in more vias to some extent**

Required T	*Normal Pattern (NP)*			*Weighted Pattern (WP)*		
	Max T	*Delay*	*Via Number*	*Max T*	*Delay*	*Via Number*
350	350.09	36.84	1327	349.95	36.89	1253
370	369.99	38.46	758	369.81	38.68	723
390	389.99	40.07	549	389.89	40.05	536
410	410.00	41.55	436	411.93	41.69	442
430	430.05	42.96	370	430.10	42.94	382
Ratio	1	1	1	1	1.	0.97

- **Weighted approach can improve via number by 5.6% at most and 3.0% on average and the lower *required_T* is the more significant effect is created.**

Best results with different weight

Type	*Weight* (α, β, γ)	*Max T (K)*	*Normalized Delay*	*Via Number*
Ami33	**0,0,1**	430.13	42.67	84
	0,1,0	350.09	35.90	548
	0.5,0.3,0.2	430.13	42.67	84
Ami49	**0,0,1**	430.17	33.03	5464
	0,1,0	361.74	31.02	57179
	0.5,0.3,0.2	430.17	33.03	5464
N100	**0,0,1**	429.91	41.32	3226
	0,1,0	349.80	38.87	14641
	0.5,0.3,0.2	410.02	40.76	4329
N200	**0,0,1**	429.84	39.89	5954
	0,1,0	349.86	37.10	19237
	0.5,0.3,0.2	409.82	39.02	7174
N300	**0,0,1**	430.13	32.72	11436
	0,1,0	350.03	30.01	32130
	0.5,0.3,0.2	430.13	32.72	11436

$$Bal(T,d,n) = \alpha \cdot (T - T_{low}) + \beta \cdot delay + \gamma \cdot via\_num$$

Conclusion

- Temperature sensitivity of leakage power cannot be ignored, especially in 3D designs
- We show the effects of both thermal aware floorplanning and thermal via insertion with leakage power considered
- Experimental results show that it is necessary to control the leakage power with temperature optimized
- With leakage power and resource constraint considered, TSV insertion result can be quite different.
- Weighted via insertion method can reduce total via number without influencing final peak temperature.

Thanks